THE LEADER IN
TECHNOLOGY
PERFORMANCE
AND INNOVATION

GOULD Electronics

Gould Inc.

Design & Test Systems Division

0114-1044-10

FOR PAUL CLEVELAND
NORTH BUILDING
CEC EX 0663

E.S.D. INSTRUMENTATION
C.C. 203 MS 145
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K101/102-D LOGIC ANALYZER
KEYBOARD AND
ASSCOCIATED DISPLAYS

INTRODUCTION:

THE GOULD BIOMATION K101-D AND K102-D PROVIDE A MAJOR ADVANCE IN LOGIC ANALYZER CAPABILITY FOR HARDWARE AND SOFTWARE ENGINEERS. THE FOLLOWING INFORMATION IS COMMON TO BOTH THE 101 AND 102, THE DIFFERENCE BEING THAT THE K101-D HAS 48 DATA CHANNELS AND THE K102-D HAS 32 DATA CHANNELS. THUS, FOR EASE OF COMPOSITION, REFERENCE WILL BE MADE TO THE K101-D.

CONTROLLED BY A 16-BIT 8086 MICROPROCESSOR, THE K101-D'S STANDARD OPERATING SYSTEM USES OVER 80 KBYTES OF ROM AND 64 KBYTES OF RAM. AS TESTING SYSTEMS GROW, SO DOES THE ANALYZER—IT'S OPERATING SYSTEM CAN ACCOMMODATE UP TO 256 KBYTES OF ROM AND 125 KBYTES OF RAM.

FEATURES:

1. TWELVE EXTERNAL CLOCK-INPUTS, COMBINABLE AT RATES UP TO 50 MHZ.
2. MULTIPLE THRESHOLD-LEVEL SELECTION FOR VARIOUS LOGIC.
3. FOUR DIFFERENT INPUT MODES.
4. FORTY-EIGHT DATA INPUTS CAPABLE OF BEING INTERNALLY SAMPLED AT RATES UP TO 100 MHZ.
5. SIXTEEN SELECTIVE TRACE-CONTROL LEVELS.
6. A 515-WORD MEMORY LENGTH WITH FULL TRACE LEVEL TRACKING.
7. FULLY INTEGRATED 4-DIGIT DIGITAL VOLTMETER (DVM).
8. EXTERNAL FREQUENCY COUNTER
9. 24 HOUR REAL TIME CLOCK (ALLOWS THE LOGIC ANALYZER TO LOG THE EXACT TIME AND DATE OF EACH RECORDING).
10. BATTERY BACK UP FEATURE FOR THE CLOCK, ALSO ALLOWS THE USER TO SAVE A COMPLETE SET OF RECORDING PARAMETERS FOR CONVENIENCE.

KEYBOARD
GENERAL DESCRIPTION

THE KEYBOARD OF THE K101-D HAS BEEN DIVIDED INTO THE FOLLOWING AREAS:

SPECIFY

FIELD

DISPLAY

GPIB

ACQUIRE

GENERAL

A. SPECIFY KEYS - ALL DISPLAY MENUS ARE SELECTED USING THESE 6 KEYS. THE DISPLAY MENU TITLE IS LOCATED AT THE TOP OF EACH DISPLAY UNDER THE GPIB INFORMATION.

B. FIELD KEYS - THE FIELD AREA CONTAINS THE K101-D DATA AND PARAMETER SELECTION CURSORS. MOST K101-D ENTRY FIELDS CAN BE PROGRAMMED BY USING THESE KEYS TO STEP THROUGH THE DISPLAY PARAMETERS WHICH WILL BLINK WHEN SELECTED. PARAMETERS CAN BE CHANGED USING THE "NEXT", "CHOICE", AND "PREV" KEYS.

C. DISPLAY KEYS - THESE KEYS SELECT THE DATA, TIMING, OR GRAPH DISPLAYS AS WELL AS "A MEMORY", "B MEMORY", COMPARE, SEARCH, AND A-B FUNCTIONS.

D. GPIB KEYS - THESE KEYS PERFORM THE FRONT PANEL GPIB FUNCTIONS. THE GPIB STATUS IS SHOWN AT THE TOP OF EACH K101-D DISPLAY.

E. ACQUIRE KEYS - ARM ACTUALLY STARTS A RECORDING, ADVANCE WILL CAUSE THE UNIT TO MANUALLY JUMP TO NEXT TRACE CONTROL LEVEL, M-A TRANSFERS HIGH SPEED MEMORY TO DISPLAY MEMORY, AND STOP WILL HALT THE K101-D DURING RECORDING CYCLES.

G. GENERAL KEYS - ALL MISCELLANEOUS DIRECT ENTRY KEY FUNCTIONS FALL INTO THIS CATEGORY.

1. THE "SAVE" AND "RECALL" KEYS IN THE TOP ROW OF KEYS ARE USED FOR STORING AND RETRIEVING A USER SELECT MENU SET-UP; RECALLING THE POWER DOWN MENU STATES USING THE SHIFT AND RECALL KEYS.

2. THE ASCII KEYBOARD AND THE YELLOW LETTERS ROUND OUT THE ASCII CHARACTER SET WHEN USING THE SHIFT KEY, AND ARE USED FOR LABELING CHANNELS IN THE TIMING DISPLAY.

3. THE SELF TEST KEY RESETS THE K101-D AND PERFORMS A MENU ORIENTED DIAGNOSTIC CHECK.

KEYBOARD

DETAILED DESCRIPTION

DISPLAY KEY SECTION

A. PRESS "A" - THIS KEY ALLOWS THE USER TO EXAMINE THE CONTENTS OF THE DISPLAY MEMORY.

B. PRESS "B" - THIS KEY ALLOWS THE USER TO EXAMINE THE CONTENTS OF THE REFERENCE MEMORY.

1. THE "EDIT" KEY MAY BE USED TO ALTER THE CONTENTS OF B MEMORY.

C. PRESS "COMPARE A/B" - THIS KEY ALLOWS THE USER TO AUTOMATICALLY COMPARE THE CONTENTS OF A AND B MEMORY.

1. COMPARISON RESULTS WILL APPEAR AT THE BOTTEM OF THE CRT WITH RESULTS SUCH AS:

   TOTAL ≠ = 20 FIRST ≠ = Ø LAST ≠ = 450

D. PRESS "SEARCH ON/OFF" - THE USER MUST FIRST ENTER THE DATA FORMAT (SPECIFY SECTION) AND ENTER THE WORD TO BE SEARCHED FOR.

1. ONCE THE SEARCH WORD IS ENTERED A SEARCH CAN THEN BE CONDUCTED.
2. COMPARISON RESULTS WILL APPEAR AT THE BOTTOM OF THE CRT WITH RESULTS SUCH AS:

   TOTAL * = 1 FIRST * = 350 LAST * = 350

E. PRESS "GRAPH" - IN THE GRAPH MODE, THE K101-D PLOTS 48 CHANNEL MAGNITUDE (VERTICAL AXIS) VERSUS TIME OR MEMORY CELLS ON THE HORIZONTAL AXIS.

1. HORIZONTAL EXPANSION BY PRESSING THE APPROPRIATE KEYS (H X 1, H X 3, H X 6, H X 12).

1. VERTICAL EXPANSION BY PRESSING "EDIT", AND THEN ENTERING THE UPPER DATA LIMIT. THEN PRESS "GRAPH".

F. PRESS "A-B" - THIS KEY SIMPLY TRANSFERS THE CONTENTS OF A MEMORY TO B MEMORY.

G. PRESS "DATA" - THIS KEY ALLOWS THE USER TO VIEW THE RECORDED DATA IN WHICHEVER RADIX CHOSEN.

H. PRESS "TIMING" - THIS KEY DISPLAYS AN ACTUAL TIMING CHART OF THE RECORDED DATA.

1. EACH TIMING TRAIN MAY BE LABELED BY PRESSING THE EDIT KEY, MOVING THE CURSOR, AND USING ANY OF THE ASCII CHARACTERS AND NUMBERS.
2. VERTICAL EXPANSION / V24, V12, V6.
3. HORIZONTAL EXPANSION / H X 1, H X 3, ETC.
4. SINCE ONLY 24 LINES OF TIMING CAN BE DISPLAYED AT ONE TIME THE PAGE ↑ OR PAGE ↓ CAN BE USED TO VIEW THE OTHER CHANNELS.

SPECIFY KEY SECTION

A. PRESS "INTERFACE" - THIS DISPLAY FIELD ALLOWS THE USER COMPLETE MANIPULATION OF THE GPIB AND RS232 INTERFACE PARAMETERS. THE TIME AND DATE OF THE REAL TIME CLOCK CAN ALSO BE SET.

1. GPIB ENTRY POSSIBILITIES:

LISTEN ONLY	CR/LF	DATA SELECT
ADDRESS =	CR/LF + EOI	TIME SELECT
TALK ONLY	CR	COMMAND = ?
	CR + EOI	

2. RS232 ENTRY POSSIBILITIES:

BAUD RATE = 110 1200 9600
150 1800
300 2400
600 4800

STOP BITS = 1
2

PARITY = ODD
EVEN
NONE

WORD LENGTH = 7 BITS
8 BITS

PROTOCOL = NAK/ACK
CTS/RTS

COMMAND = ?

B. <u>PRESS "CLOCK SELECT"</u> - THE USER NOW HAS THE CHOICE OF SIX MENU SCREENS TO SET UP THE CORRECT CLOCKING ARRANGEMENT FOR A PARTICULAR PROBLEM. THE "NEXT" KEY CAN NOW BE USED TO STEP THROUGH THE VARIOUS CLOCK MENUS.

1. ENTRY POSSIBILITIES:

<u>CLOCK MENUS</u>

INTERNAL
EXTERNAL SINGLE-PHASED
EXTERNAL MULTI-PHASED
MIXED SINGLE-PHASED
MIXED MULTI-PHASED
INTERNAL EXTENDED

<u>INTERNAL CLOCK RANGE</u>

0010 NANOSECONDS TO 1,000 MICROSECONDS

CLOCKS

	CLOCK	ENABLE
A SECTION	J,K	R,S
B SECTION	J,K	R,S
C SECTION	J,K	R,S

INTERNAL A, B, OR C SECTIONS

MASTER CLOCK: CLOCKS INPUT DATA INTO MAIN MEMORY.

C. PRESS "INPUT MODE" - THIS MENU DISPLAY IS USED TO PROGRAM CHANNEL OPERATING MODE.

1. ENTRY POSSIBILITIES:

INPUT MODES

SAMPLE
GLITCH
LATCH
DEMUX (XF - X8 ONLY)

THRESHOLDS

TTL
ECL
VAR A ±9.99 V
VAR B ±9.99 V
(ASSIGNABLE BY PROBE)

ARMING

MANUAL
AUTO
AUTO STOP IF A=B
AUTO STOP IF A<>B
AUTO STOP IF A=B WITHIN LIMITS
AUTO STOP IF A<>B WITHIN LIMITS

D. PRESS "TRACE CONTROL" - SIXTEEN SEPARATE SELECTIVE TRACE-CONTROL LEVELS ARE NOW AVAILABLE, EACH WITH ITS OWN MENU SCREEN TO SIMPLIFY THE USER'S SPECIFICATION TASK (0 - F). EACH LEVEL HAS FOUR CONDITIONAL COMMANDS — STOP, JUMP, ADVANCE, AND SELECTIVE TRACE. THE EXECUTION OF EACH COMMAND WITHIN A CONTROL LEVEL CAN BE MADE CONDITIONAL TO A UNIQUELY DEFINED 48-BIT DATA PATTERN AND DELAY COUNT.

INSTEAD OF SIMPLY FINDING A SPECIFIC SPOT IN A PROGRAM FOR RECORDING, THE K101-D ACTUALLY FOLLOWS THE PROGRAM FLOW. THE INSTRUMENT TRACES THROUGH COMPLEX DATA PATHS, RECORDING NOT JUST ONE, BUT MANY PRECISELY DEFINED PORTIONS OF THE PROGRAM FLOW ALONG THE WAY.

1. ENTRY POSSIBILITIES:

LEVEL

16 LEVELS (0 - F)

DELAY

SPECIFIED EITHER IN DECIMAL OR HEX.

COUNTED AS EITHER OCCURENCES OF MASTER CLOCK CYCLES OR OF THAT LEVEL'S ADVANCE PATTERN.

END LEVEL

(0-F)

STOP CONDITIONS

STOP IF DATA = S AND SAMPLE COUNT >DELAY
STOP IF DATA = S AND SAMPLE COUNT <DELAY
STOP IF DATA = S AND SAMPLE COUNT =DELAY
STOP IF DATA = S AND SAMPLE COUNT>=DELAY
STOP IF DATA = S AND SAMPLE COUNT<=DELAY
STOP IF DATA = S AND SAMPLE COUNT<>DELAY
STOP IF DATA = S
STOP ALWAYS
STOP NEVER

STOP PATTERN

S = XXXX XXXX XXXX XXXX

JUMP TO Ø NEVER

J = XXXX XXXX XXXX XXXX

ADVANCE NEVER

A = XXXX XXXX XXXX XXXX

TRACE ALWAYS

T = XXXX XXXX XXXX XXXX

E. PRESS "LOGIC POLARITY" - THIS KEY SIMPLY ALLOWS THE USER TO SPECIFY NEGATIVE OR POSITIVE CONVENTION LOGIC ON ANY OF THE 48 DATA CHANNELS.

1. ENTRY POSSIBILITIES:

POLARITY

ASSIGNABLE BY CHANNEL FOR ALL 48 INPUTS.

F. PRESS "DATA FORMAT" - THE DATA FORMAT MENU IS USED TO ARRANGE THE CHANNELS OF THE LOGIC ANALYZER TO SUIT THE NEEDS OF THE USER.

AQUIRE KEY SECTION

A. PRESS "ARM" - THIS KEY IS USED TO INITIATE A RECORDING WITH THE K101-D.

B. PRESS "ADVANCE" - THIS KEY CAN BE USED TO AUTOMATICALLY ADVANCE THE TRACE CONTROL LEVEL DURING A RECORDING.

C. PRESS "M→A" - THIS KEY CAN BE USED TO TRANSFER THE CONTENTS OF HIGH SPEED MEMORY TO DISPLAY MEMORY IN THE CASE OF EXTERNAL CLOCK LOSS.

D. PRESS "STOP" - THIS KEY WILL STOP A RECORDING IN PROGRESS.

GPIB SECTION KEYS

A. THESE KEYS ARE USED IN CONJUNCTION WITH THE INTERFACE MENU.

1. SERVICE - THIS KEY SIMPLY PUTS A SERVICE REQUEST ONTO THE GPIB BUS (SRQ).

2. GO TO LOCAL - THIS KEY IS USED TO RETURN THE K101-D TO CONTROL OF THE LOCAL USER.

SELF TEST KEY

A. THIS KEY IS USED TO ACCESS AN EXTENSIVE SERIES OF TESTS TO CHECK SYSTEM CONFIDENCE.(SHIFT KEY MUST BE USED TO ACCESS SELF TEST MODE)

GENERAL KEYS

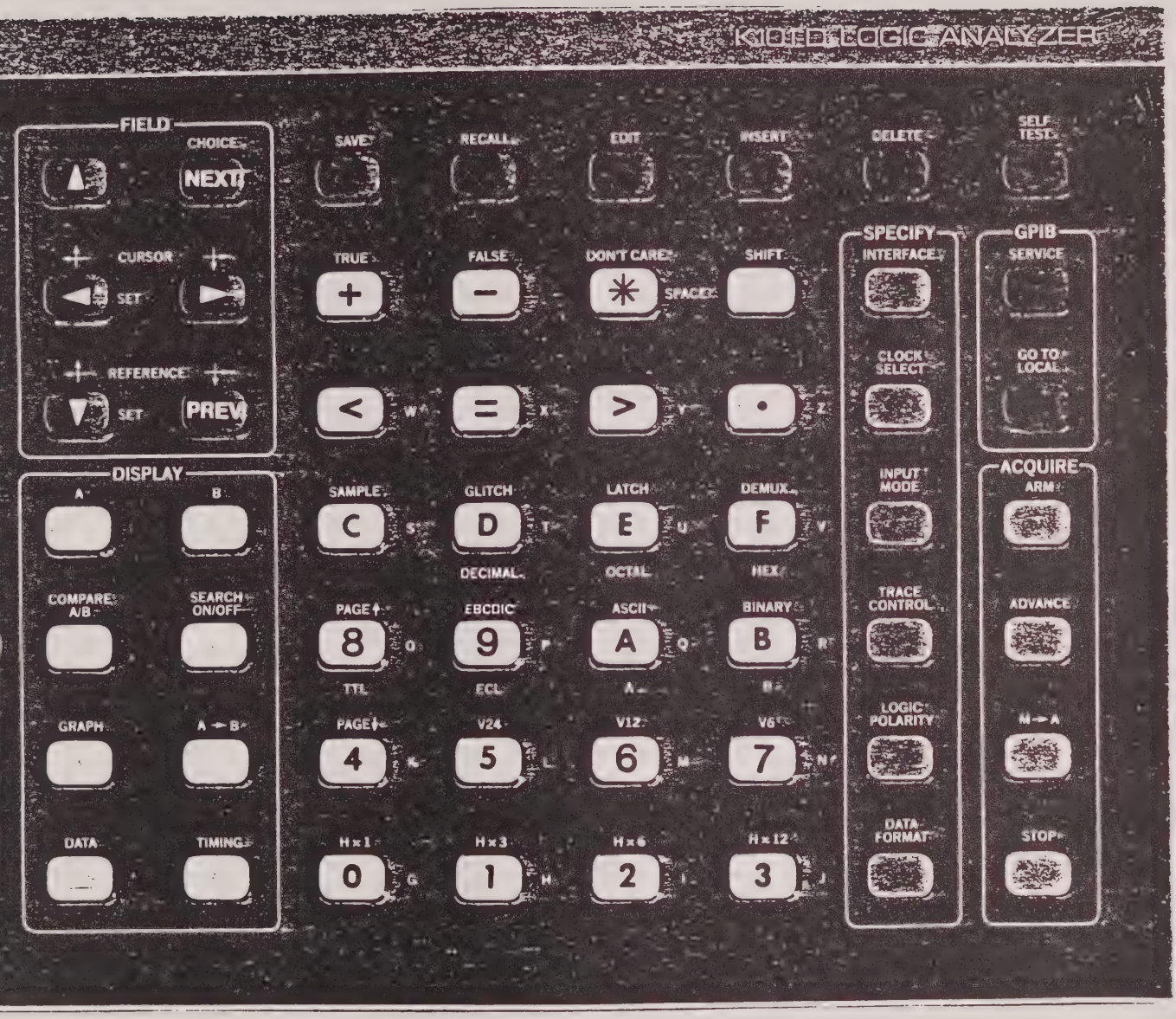
A. THE REMAINING KEYS WHICH ARE NOT DESIGNATED IN ANY CERTAIN SECTION ARE USED IN CONJUNCTION WITH VARIOUS DEDICATED KEYS.

1. "SAVE" - ALLOWS THE USER TO STORE A CERTAIN SET OF PARAMETERS IN THE CMOS RAM CIRCUIT.

2. "RECALL" - USED TO RECALL THE SAVED PARAMETERS.

3. " SHIFT / RECALL" - RESTORES THE DISPLAY MENU TO IT'S ORIGINAL FORMAT.

4. "EDIT" - USED IN CONJUNCTION WITH "B" MEMORY. DATA DISPLAY EDITING IS ACCOMPLISHED.



K101-D FRONT PANEL

SYSTEM

BLOCK DIAGRAM

K101-D LOGIC

ANALYZER

BLOCK DIAGRAM

BIOMATION'S MODEL K101/102-D LOGIC ANALYZER IS AN EXTREMELY POWERFUL AND INNOVATIVE INSTRUMENT DESIGNED ESSENTIALLY AS TWO DIFFERENT, BUT INTERACTIVE DEVICES; A POWERFUL MICRO-COMPUTER (8086 BASED), AND SOPHISTICATED LOGIC ANALYZER.

HUMAN INTERFACE WITH THE FRONT PANEL KEYBOARD OR VIA THE GPIB, ALLOWS THE MICROCOMPUTER TO COMPLETELY CONTROL ALL RECORDING PROCESSES.

A. PROBES

1. THE INPUT PROBES ARE DIVIDED INTO THREE SECTIONS (SECTION A, SECTION B, AND SECTION C)
2. EACH SECTION CONTAINS 2 GROUPS OF 10 INPUTS EACH.
3. 60 TOTAL INPUTS TO THE K101-D.
   - 48 DATA INPUTS
   - 12 CLOCK INPUTS
4. ONE INPUT SECTION CONTAINS THE FOLLOWING:

K101-D ACTIVE PROBE	K101-D ACTIVE PROBE
SECTION A	SECTION A
CLK	EN
A A A A A A A A A A	A A A A A A A A A A
J K F E D C B A 9 8	R S 7 6 5 4 3 2 1 0
∘ ∘ ∘ ∘ ∘ ∘ ∘ ∘ ∘ ∘	∘ ∘ ∘ ∘ ∘ ∘ ∘ ∘ ∘ ∘

5. INPUT IMPEDANCE IS 1MΩ, 15pF, OVER A RANGE OF ±10 V.
6. THRESHOLDS ARE ASSIGNABLE FOR EACH 10 INPUT PROBE ASSEMBLY.
   - TTL (+1.40 V)
   - ECL (-1.30 V)
   - VAR A, VAR B (+9.98 V IN 10 mv STEPS)

B. THRESHOLD BOARD

1. VARIABLE A & B DAC
2. TTL & ECL REFERENCES
3. THRESHOLD MULTIPLEXER
4. GPIB INTERFACE
5. A TO D CONVERTER
6. INTERVAL TIMER
7. RS232 AND RS449 USARTS
8. DVM INPUT BUFFER
9. MPU INTERFACE

C. HIGH SPEED DATA BOARD

1. DATA INPUT BUFFERS
2. GLITCH DETECTION LOGIC
3. DATA LATCHES
4. SAMPLE REGISTERS
5. DATA PIPELINE
6. RECORD (HIGH SPEED) MEMORY
7. MEMORY CONTROL LOGIC
8. MPU INTERFACE

D. CLOCK BOARD

1. INTERNAL CLOCK GENERATION
2. EXTERNAL CLOCK DECODING
3. CLOCK DISTRIBUTION
4. "AND" / "OR" CLOCK SELECTION
5. LEVEL MEMORY
6. MPU INTERFACE

E. CONTROL BOARD

1. WORD RECOGNITION CIRCUITS
2. WORD SELECTION CIRCUITS
3. LEVEL SWITCHING CIRCUITS
4. DELAY COUNTER
5. RECORD CONTROL LOGIC
6. MPU INTERFACE

F. MPU BOARD

1. 8086 MICROPROCESSOR
2. ADDRESS REGISTERS AND DATA TRANSCEIVERS
3. 128 K BYTES OF DYNAMIC RAM
4. 128 K BYTES OF ROM
5. MEMORY CONTROLLER
6. I/O DECODING

G. DISPLAY BOARD

1. CRT CONTROLLER
2. HORIZONTAL AND VERTICAL DEFLECTION
3. HORIZONTAL AND VERTICAL TIMING
4. HIGH VOLTAGE GENERATION
5. KEYBOARD AND FRONT PANEL INTERFACE
6. INTERRUPT PROCESSOR
7. CMOS RAM SAVE CIRCUIT
8. REAL TIME CLOCK
9. BEEPER CIRCUIT

K101/102-D THEORY
OF
OPERATION

PROBE
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0251

DESIGNED AROUND A CUSTOM THICK-FILM HYBRID INTEGRATED CIRCUIT, THE DIGITAL PROBES OF THE K101/102-D LOGIC ANALYZER ARE ESSENTIALLY ZERO-CROSSING CIRCUITS DUPLICATED FIVE TIMES ON EACH CIRCUIT.

A. ALL INPUTS ARE "FETs" WITH A 1-MΩ, 10-pF INPUT IMPEDANCE TO ENSURE MINIMUM LOADING AND DISTORTION OF THE SIGNALS UNDER TEST. (SD5001 AT LOCATION Q1)

B. GLITCHES AS NARROW AS 5 NS (ASYNCHRONOUS NOISE SPIKES) CAN BE CAPTURED ON ALL INPUTS.

C. GROUND ISOLATION IS PROVIDED ON EACH INPUT FOR PROTECTION FROM THE ACCIDENTAL CONNECTION OF THE GROUND LEAD TO SIGNALS OVER A ±15 VDC RANGE.

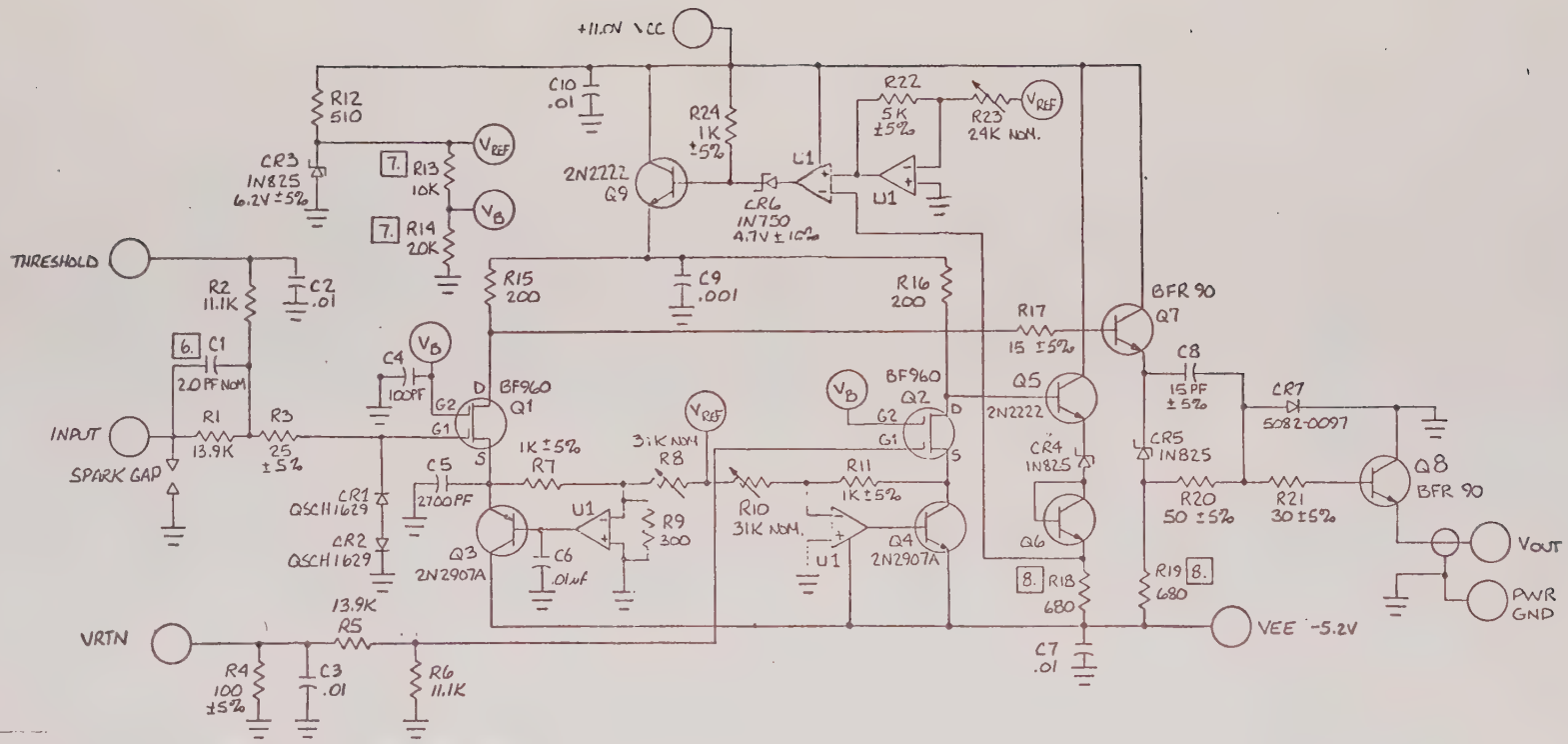
D. OVERVOLTAGE PROTECTION IS ANOTHER PROVISION ON ALL INPUTS, AS ILLUSTRATED BY THE CROSSED DIODES (CR1 & CR2) AND TUNED SPARK GAP.

   1. THE DIODES PROTECT UP TO ABOUT 500 VDC OVER THE ENTIRE FREQUENCY RANGE.

   2. THE SPARK GAPS FUNCTION AT VOLTAGES ABOVE 500 V TO PROTECT THE PROBE INPUTS FROM STATIC CHARGES AS HIGH AS 5 kV DC.

E. TWO IDENTICAL HYBRIDS ARE MOUNTED BACK-TO-BACK ON A SMALL PRINTED-CIRCUIT BOARD WITHIN EACH POD TO ELIMINATE SKEW BY MAINTAINING A CONSTANT PROBING-DISTANCE FOR ALL INPUTS.

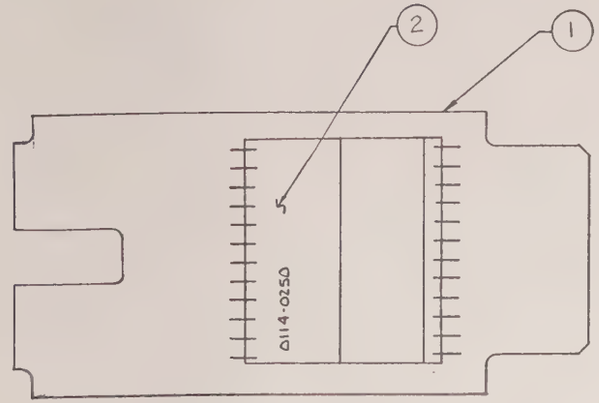
F. TWO CLOCK INPUTS AND EIGHT DATA INPUTS ARE CONTAINED IN EACH PROBE POD.

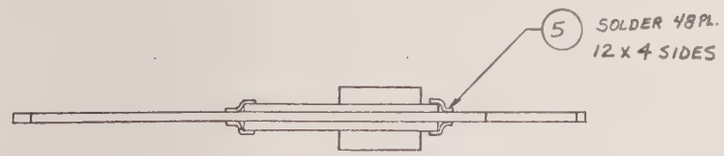


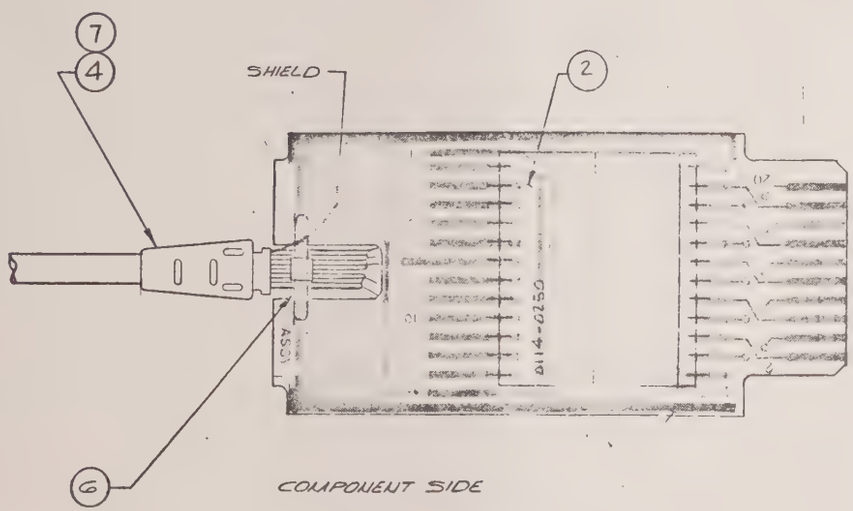
K500 PROBE HYBRID
PART NUMBER 0950-0121

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—		MB		
	B		PILOT REL PER ERN #0102	JKP	RD	
	C	1573	REVISED PER ECO.	MB	RD	3-21-81
	D	1773	REVISED PER ECO	[illegible]	DL	7/27/81
	E	2126	REVISED PER ECO	[illegible]	RD	10-9-81
	E	—	PROD REL PER ERN #0207	MB	RD	1/29/82
	F	2641	REV'D PER ECO	George	JHS	8/31/82

SOLDER SIDE







COMPONENT SIDE

WIRING INSTRUCTIONS		
	CABLE	TO BOARD
TW PR	GRN (30 GA)	16
	LT BRN (30GA)	17
TW PR	YEL (30GA)	18
	LT BRN (30GA)	19
TW PR	ORG (30GA)	20
	LT BRN (30GA)	21
TW PR	RED (30GA)	23
	LT BRN (30GA)	24
TW PR	BRN (30GA)	25
	LT BRN (30GA)	26
	BLK (24GA)	7/22/28
	RED (24GA)	1
TW PR	BLUE (30GA)	4
	LT BRN (30GA)	3
TW PR	VIO (30GA	6
	LT BRN (30GA)	5
TW PR	GRAY (30GA)	9
	LT BRN (30GA)	8
TW PR	WHT (30GA)	11
	LT BRN (30GA)	10
TW PR	BLK (30GA)	13
	LT BRN (30GA)	12
	YEL (24GA)	27
	BLUE (24GA)	15
	SHIELD	14

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0.599 ± .003; 600.999 ± .004; 1.000-1.499 ± .005

DASH NO.	NUMBER	QTY
-10	0114-0254	
	NEXT ASSEMBLY	

		DATE
DRAWN	[illegible]	2-9-81
CHECKED	R. Dean	2/4/82
PROJ. ENG.	Curt	1/18/82
MANUFACTURING	[illegible]	1/7/82
QUALITY ASSUR	[illegible]	1/7/82
ENG. SERV.	R. Gipson	1/7/82

GOULD biomation

TITLE: PROBE PWB ASSY

SCALE	SIZE	PART NUMBER	REV
2/1	C	0114-0240	F

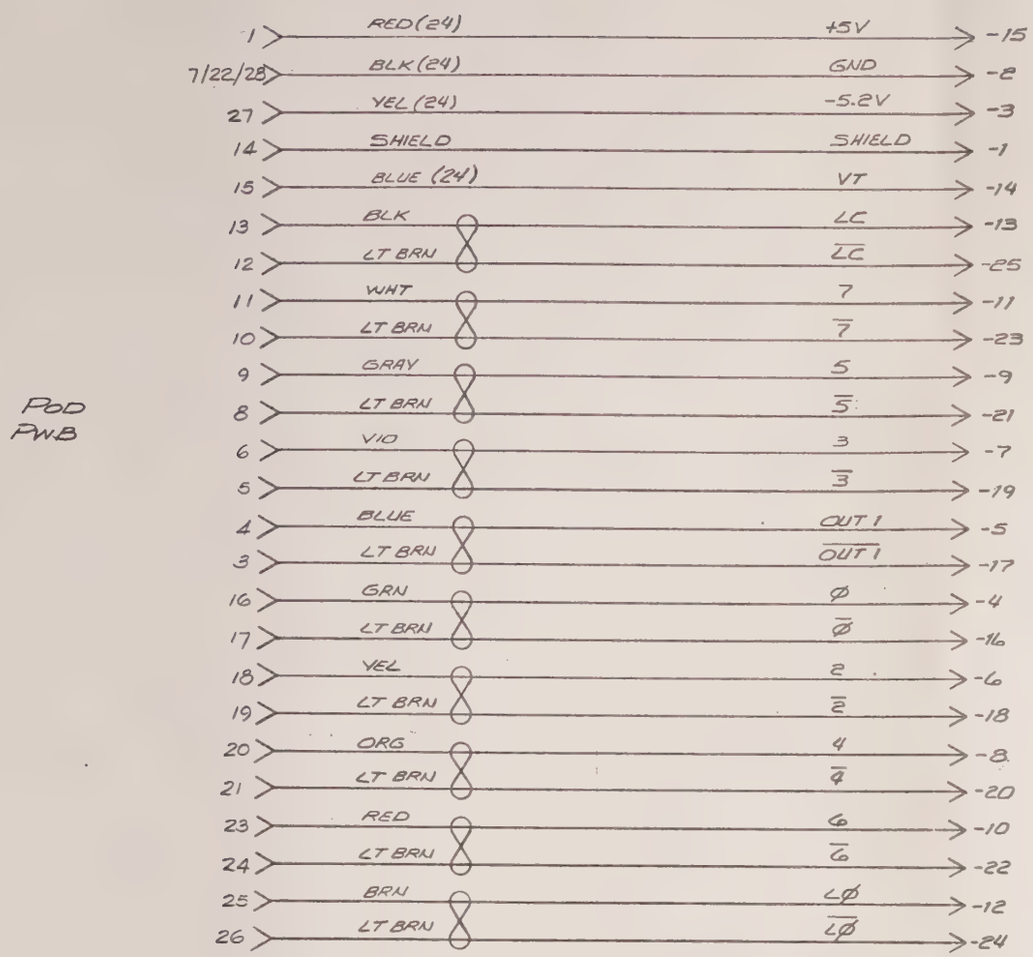
CODE K101 SHEET 1 OF 2

DWG. NO. 0114-0240 SH 1 REV F

MAY 31 1983

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4428

SCHEMATIC



1	RED (24)	+5V	-15	
7/22/28	BLK (24)	GND	-2	
27	YEL (24)	-5.2V	-3	
14	SHIELD	SHIELD	-1	
15	BLUE (24)	VT	-14	
13	BLK	LC	-13	
12	LT BRN	$\overline{LC}$	-25	
11	WHT	7	-11	
10	LT BRN	$\overline{7}$	-23	
9	GRAY	5	-9	
8	LT BRN	$\overline{5}$	-21	
6	VIO	3	-7	
5	LT BRN	$\overline{3}$	-19	
4	BLUE	OUT 1	-5	
3	LT BRN	$\overline{OUT\ 1}$	-17	
16	GRN	Ø	-4	
17	LT BRN	$\overline{Ø}$	-16	
18	YEL	2	-6	
19	LT BRN	$\overline{2}$	-18	
20	ORG	4	-8	
21	LT BRN	$\overline{4}$	-20	
23	RED	6	-10	
24	LT BRN	$\overline{6}$	-22	
25	BRN	LØ	-12	
26	LT BRN	$\overline{LØ}$	-24	

POD PWB

25 PIN "D" CONN.

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DWG. NO. 0114-0240 SH 2 REV F

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: .0-.599 ± .003; .600-.999 ± .004; 1.000-1.499 ± .005

DRAWN [signature] DATE

CHECKED [signature] 2/5/82

PROJ. ENG. [signature] 1782

MANUFACTURING

QUALITY ASSUR. [signature] 1/7/82

GOULD biomation

TITLE PROBE PWB ASSY

SCALE | SIZE C | PART NUMBER 0114-0240 | REV F

CODE K101 | SHEET 2 OF 2

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV. | DATE

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4428

MMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1					1	1	0114-0242	PROBE PWB FAB				
2					2	2	0114-0250	HYBRID				
3												
4					—	1	9000-0072-10	K101 POD-TO UNIT CABLE W/ MOLDING				
5					A/R	A/R	0114-0262	LEAD FRAME				
6					1	1	7200-0008	TY-WRAP				
7					1	—	9000-0072-20	K101 POD-TO UNIT CABLE W/ MOLDING				

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	B	PILOT REL PER ERN #0102	2-11-81	[illegible]	RD	
	C	REVISED PER ECO # 1578	3-21-81	MB	RD	
	D	REVISED PER ECO # 1773	6-8-81	[illegible]	DL	
	E	REVISED PER ECO # 2126	10-5-81	JC	RD	
	E	PROD REL PER ERN #0207	1/29/82	MB	[illegible]	
	F	Rev'D Per ECO # 2641	8-6-82	George	GHS	

-10	0114-0254	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	U. PERGINS	1/21/81
CHECKED	[illegible]	2-5-82
ENGINEER	[illegible]	1-7-82
MANUFACTURING	[illegible]	1/7/82
QUALITY ASSURANCE	[illegible]	1/7/82

LIST OF MATERIAL

PROBE PWB ASSY

MODEL K101

biomation

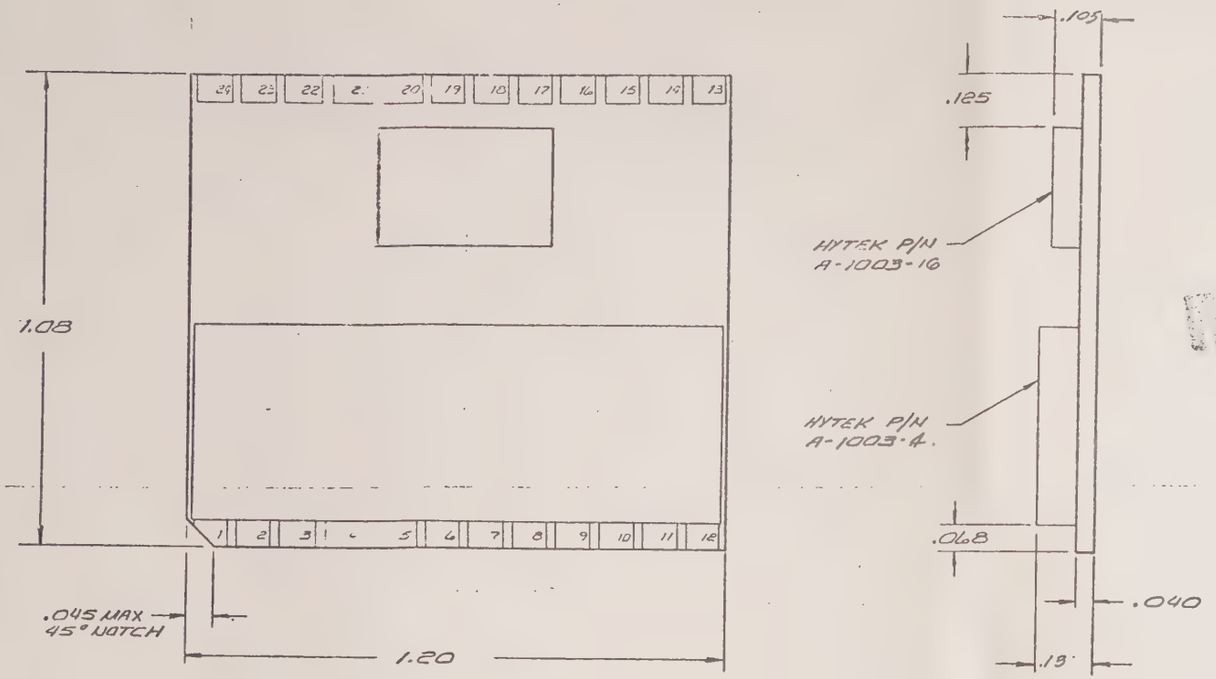
MAY 3 1 1983

B 0114-0240 REV F

CODE

SHEET 1 OF 1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTOTYPE			
	B		PILOT REL PER ERN 116	[illegible]	[illegible]	
	C	2578	REVISED PER ECO No	JWC	JW	7-15-82
	D	2590	REVISED PER ECO No	JWC	JW	7-15-82



APR 1 1 1983

REFERENCE PRINT

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER	QTY
-10	0114-0240	2
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, ANGLES XX ± .020, ± 1°, XXX ± .010

HOLE SIZE: 0.599 ± .003, 600.999 ± .004, 1.000 1.499 ± .0[illegible]

ENG. SERV. | DATE

DRAWN: L. PERGINS | DATE: 1/21/81

CHECKED: [illegible] | 3-17-8[illegible]

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

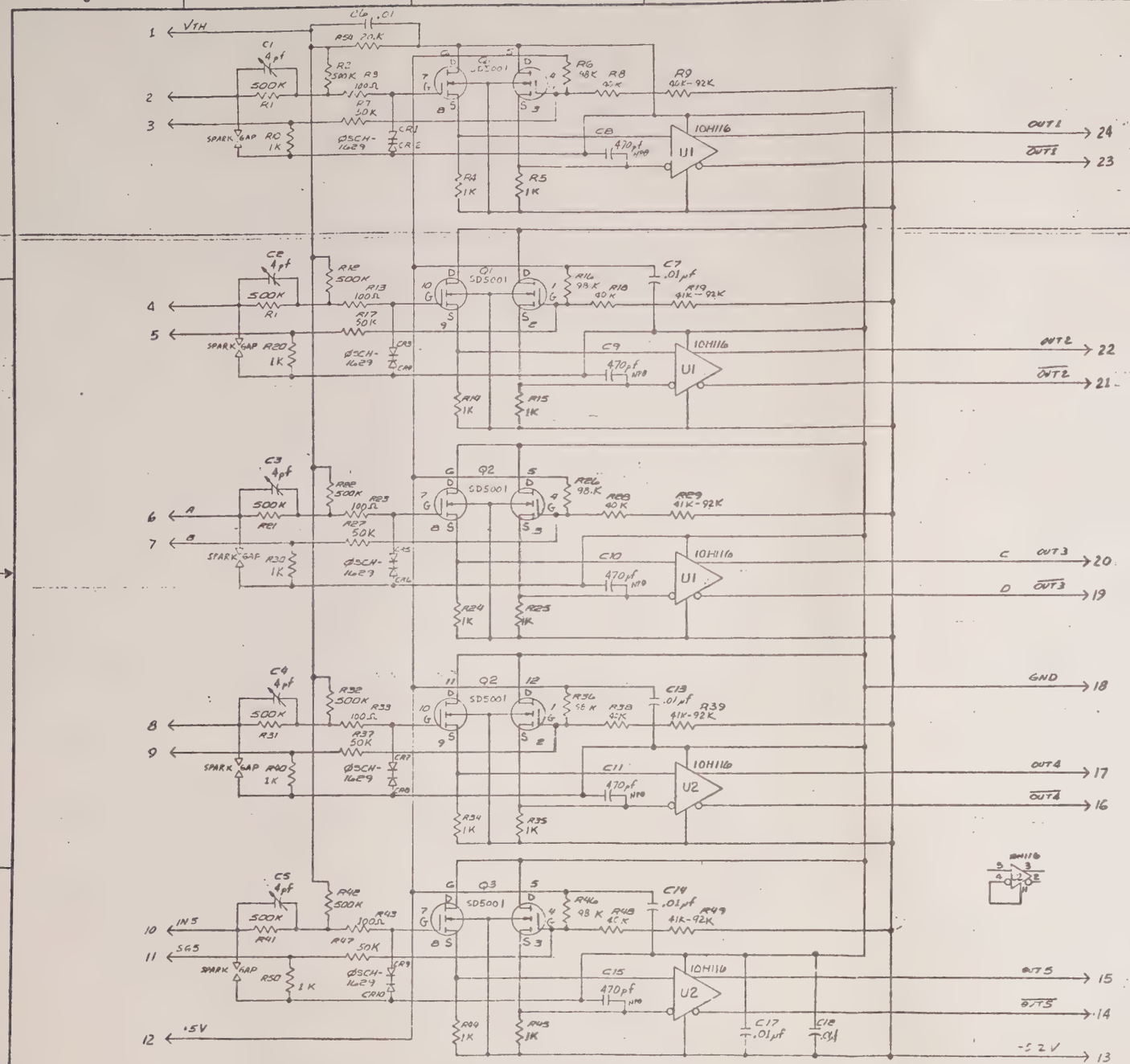
TITLE: ASSEMBLY- K101 PROBE HYBRID

SCALE	SIZE	PART NUMBER	REV
5:1	C	0114 - 0250	D

CODE K101 | SHEET 1 OF 1

DWG. NO. 0114-0250 | SH 1 | REV D

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4428



DWG. NO. 0114-0251 SH 1 REV 1

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A					
	B		added R19 and C6 changed R1 and R7 (5 PLCS) from 100K to 500K			12/12
	C		renumbered resistors and capacitors PILOT REL PER ERN 116			1/26
	D		REVISED PER ECO No 2578			3/14/82
1	E	2590	REVISED PER ECO No			7-15-82

REFERENCE PRINT

APR 11 1983

NOTES

1. ALL RESISTORS ARE ±5% AND CAPACITORS ± 20% UNLESS OTHERWISE SPECIFIED.
2. R9 IS TRIMED TO NULL OFFSET VOLTAGE (SEE NOTE 8)
3. C1 SHOULD BE DETERMINED DURING PROTOTYPE EVALUATION TO COMPENSATE THE EFFECTIVE CAPACITANCE OF THE INPUT MODE TO MEET THE SPECIFICATION IN NOTE 8 (NOM. IS 20% OVERSHOOT)
4. PADS TO BE Pd Ag.
5. OPERATING TEMP. RANGE 0°C TO 70°C
6. TEST CIRCUIT SHOWN ON SHT 2 SHOULD BE USED TO MEASURE OFFSET VOLTAGE.
7. ELECTRICAL SPECIFICATIONS: AT TA = 25°C, VEE = -5.2 V ± 1%
   COMMON MODE REJECTION: 40 db MIN. (± .5V)
   OFFSET VOLTAGE, ± 10 MV MAX. (MEASURED AT INPUT)
   PROPAGATION DELAY, 9.0 n SEC. MAX. (FROM INPUT TO OUT OR $\overline{OUT}$)
   TRANSITION TIMES, 20% TO 80% 3.3 n SEC MAX (OUT & $\overline{OUT}$)
   INPUT COMPENSATION, +15% MIN. TO +25% MAX.
8. COVER SHALL BE THE SIZE TO PROTECT BONDING WIRES AND ACTIVE CIRCUIT COMPONENTS AND SHALL PRECLUDE DAMAGE TO UNIT DURING TEST AND ASSEMBLY.
9. MARK WITH PART No 0114-0251 AND REV. LEVEL ON BACKSIDE.
10. MARK REV LEVEL ON FRONT OF PART.

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

TOLERANCE

CHECKED 3-17-81

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV

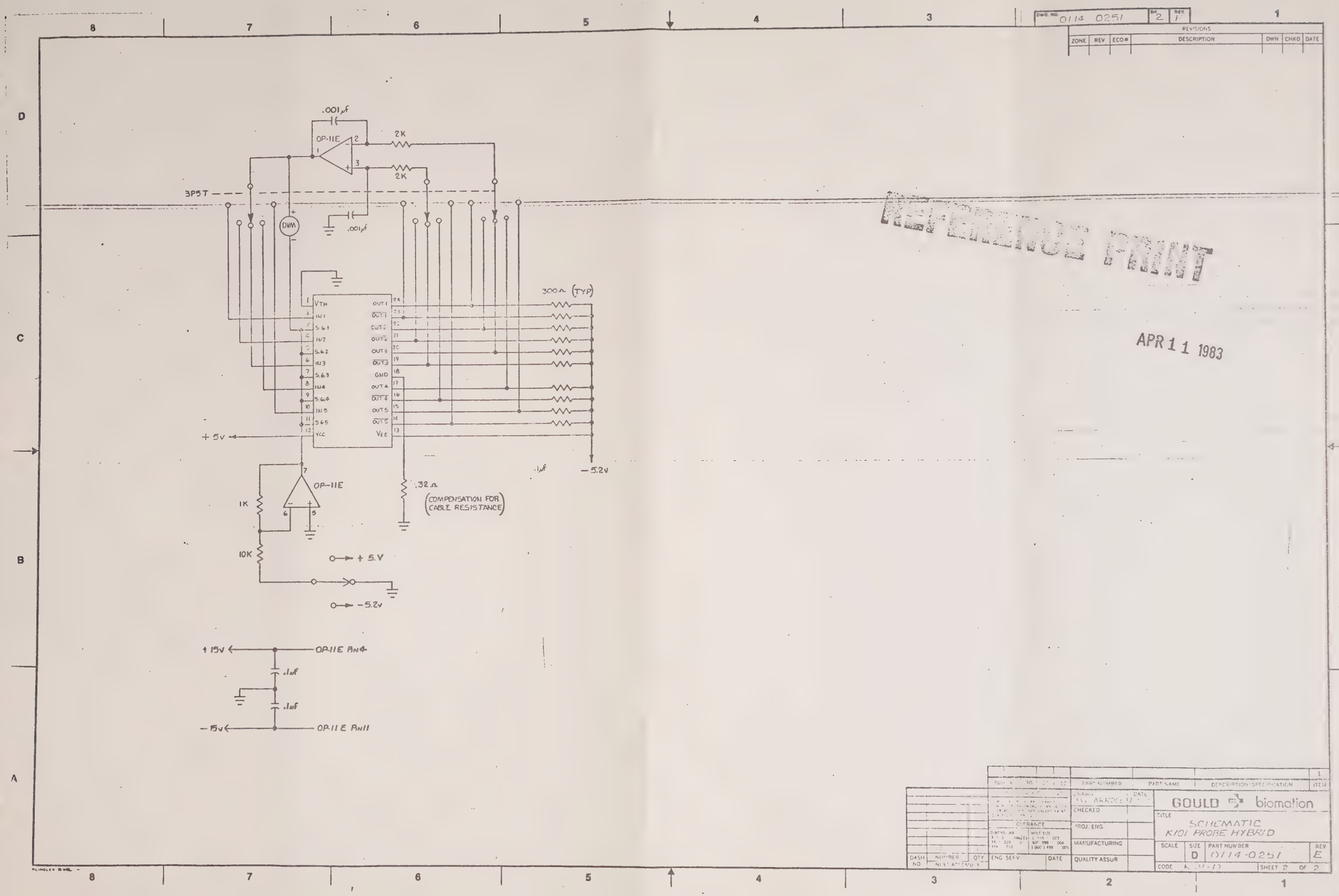
DASH NO | NUMBER | QTY | NEXT ASSEMBLY

GOULD biomation

TITLE SCHEMATIC— K101 PROBE HYBRID

SCALE — | SIZE D | PART NUMBER 0114-0251 | REV E

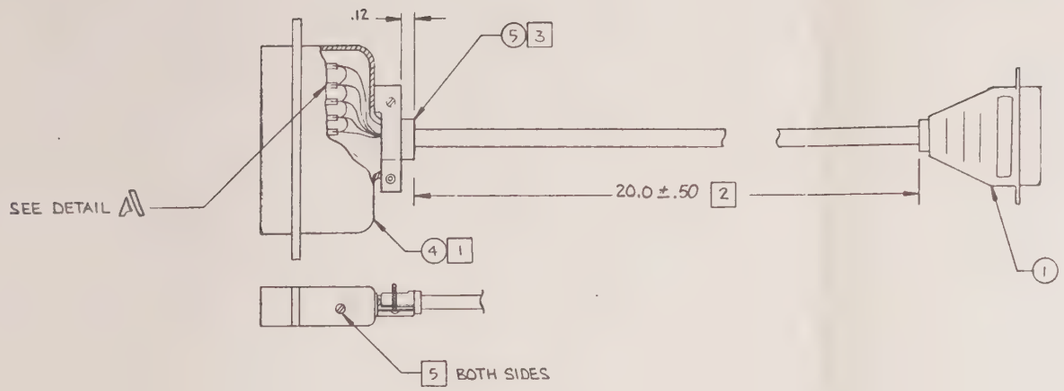
CODE | SHEET 1 OF 2

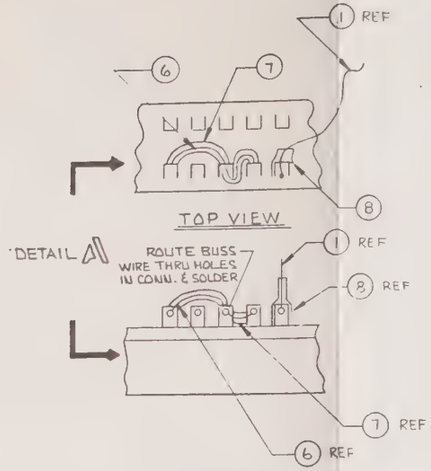


DWG. NO. 0114 0251
SH 2
REV F
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
.001µf
OP-11E
2K
2K
3P5T
DVM
.001µf
VTH
IN1
S.6.1
IN2
S.6.2
IN3
S.6.3
IN4
S.6.4
IN5
S.6.5
VCC
OUT1
OUT2
OUT3
GND
OUT4
OUT5
VEE
300Ω (TYP)
+5V
-5.2V
.1µf
OP-11E
1K
10K
.32Ω
(COMPENSATION FOR CABLE RESISTANCE)
+5.V
-5.2v
+15V
OP-11E PIN4
.1µf
.1µf
-15V
OP-11E PIN11
REFERENCE PRINT
APR 11 1983
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC
K101 PROBE HYBRID
SCALE
SIZE
D
PART NUMBER
0114-0251
REV
E
CODE
SHEET 2 OF 2

DWG NO 0114-0249 SH 1 REV

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
—	A	—	PER PER EPN # 277		[illegible]	[illegible]
	B	2748	REVISED PER ECO	M.W	DGW	5/23
	C	3625	REVISED PER ECO	MW	DGW	4/20





EXAMPLE OF CONNECTIONS
REFERENCE SHEET 2 OF 2.

NOTES:

1. ADD CAPACITOR TO CABLE BEFORE ADDING CONNECTOR.
2. CUT CABLE AT 22" CUT OFF INSULATION AND SHIELD AT 2" FROM END STRIP AND TIN .15 OFF ALL WIRES ADD SHRINK TUBING (ITEM 8) ON EACH WIRE THEN SOLDER TO PIN, REF DETAIL A.
3. CUT HOSE (ITEM 5) .75 LONG AND INSERT IT ON CABLE ITEM 1 PRIOR TO SOLDER OF (ITEM 4).
4. ROUTE (ITEM 6) THRU CONTACTS AS SHOWN ON SHEET 2 AND ADD (ITEM 7) AND SOLDER.
5. SET SCREWS SHOWN ARE SUPPLIED WITH (ITEM 4).
6. ADD SHRINK TUBING (ITEM 7) TO LOOSE END OF RED WIRE (+5V), SHEET 2 OF 2 TO ELIMINATE CONTACT WITH SHIELD.

REFERENCE PRINT
APR 22 1983

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .XX ±.020 ±.010; XX ± .010; HOLE SIZE: 0.599 .003, 600.999 .004, 1.000 1.499 .005

DRAWN [illegible] DATE 4/15/82
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR

GOULD biomation

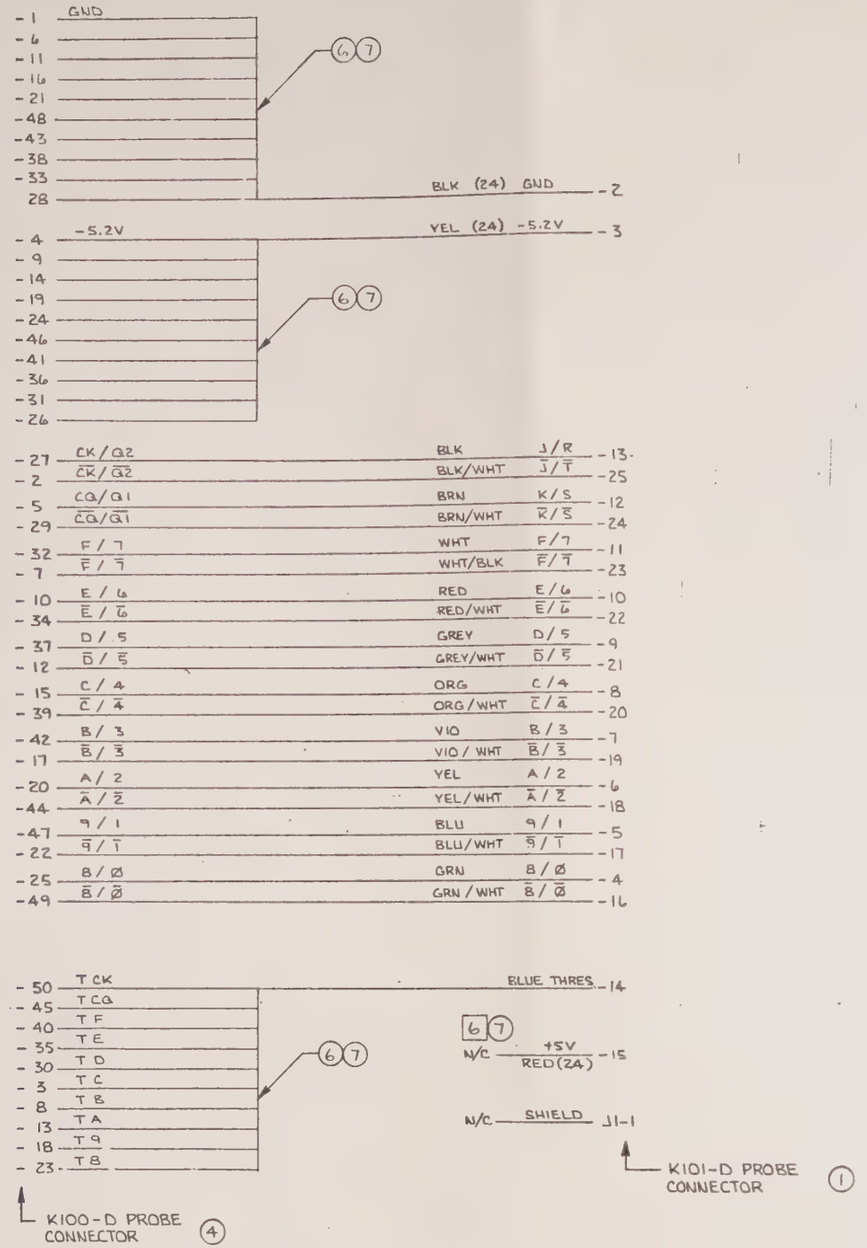
TITLE CABLE ASSEMBLY - K101D
ADAPTER FOR K100 PROBES

SCALE — SIZE D PART NUMBER 0114-0249 REV [illegible]
CODE SHEET 1 OF 2

DASH NO | NUMBER | QTY | NEXT ASSEMBLY | ENG SERV | DATE

DWG NO. 0114-0249 SH 2 REV 1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH. 1			



REFERENCE PRINT
APR 23 1983

DASH NO	NUMBER NEXT ASSEMBLY	QTY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL .X ± .1 ANGLES .XX ± .030 1° .XXX ± .010
FINISH 0-.199 ± .001 .XX .199 ± .004 .XXX ± .199 ± .001

ENG SERV		DATE

DRAWN		DATE 4-19-81
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		

GOULD biomation

TITLE SCHEMATIC, K101-D ADAPTER FOR K100 PROBES

SCALE	SIZE	PART NUMBER	REV
---	D	0114-0249	1

CODE SHEET 2 OF 2

ITEM	-90	-80			-50	-40	-30	-20	-10	PART NUMBER	PART DESCRIPTION	REFERENCE DESIGNAT	LTM
1									1	9000-0072	ROD TO UNIT CABLE & MOLDING		
2													
3													
4									1	6000 0009-10	CONN. PLUG	50 PIN	
5									1	7200-0096	GROMET/HOSE		
6									AR	7100-0141-10	BUS WIRE, 24 AWG		
7									AR	7200-0151-10	SLEEVING, 24 AWG		
8									AR	7200-0050-11	SHRINK TUBING, 1/16		
9													
10													

REFERENCE PRINT
APR 22 1983

REV	DESCRIPTION	DATE	DWN	CKD
A	REVISED PER ECO # 277	[illegible]	[illegible]	[illegible]
B	REVISED PER ECO 2708	2/28/83	MW	DGW
C	REV'D PER ECO 3525	4/19/83	MW	DGW

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

		DATE
DWN	B. S	[illegible]
CHK		
ENGR		
MFG.		
Q.A.		

LIST OF MATERIAL

CABLE ASSEMBLY
K10 D
ADAPTER FOR K100 PROBES

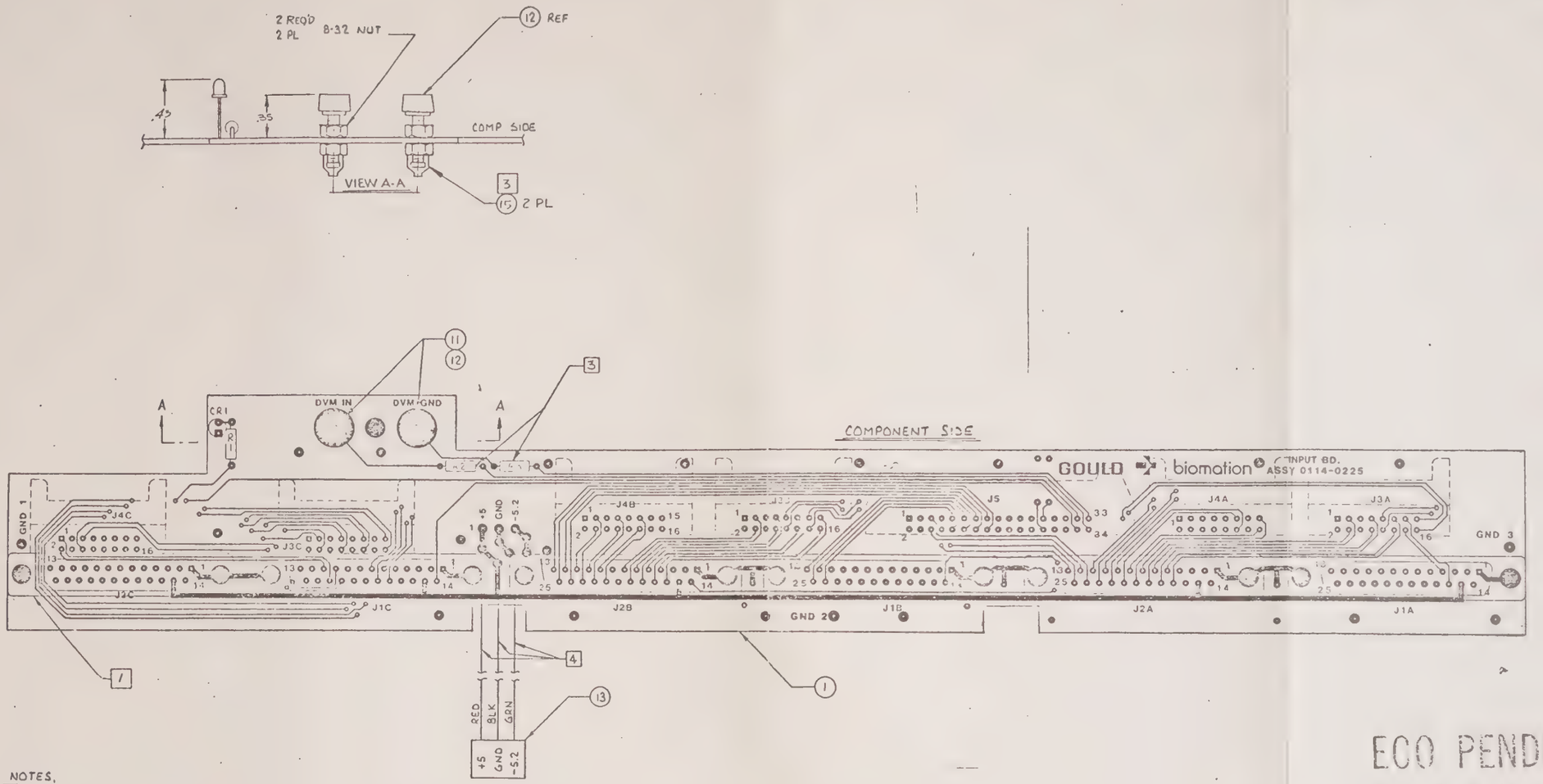
GOULD biomation

B 0114-0249 REV C

MODEL K10 | SHEET 1 OF 1

KLINGLER K-VEL H-10

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	~	PILOT REL PER ERN#0161	[illegible]	[illegible]	[illegible]
	B	[illegible]	REVISED PER ECO No	[illegible]	[illegible]	[illegible]
	C	[illegible]	REVISED PER ECO No	[illegible]		
	D	3602	REVISED PER ECO No	[illegible]	[illegible]	[illegible]



NOTES,

1. J1C, J2C, J3C, & J4C ARE TO BE ASSEMBLED ON -10 ONLY.
2. J3A, J4A, J3B, J4B, J3C, J4C, & J5 ARE MOUNTED ON THE SOLDER SIDE.

3. PLACE TUBING OVER END OF CONNECTOR SO THAT IT IS FLUSH WITH NUT, THEN SHRINK AND SQUEEZE LOWER END TOGETHER.

ECO PENDING
No. 3820
DATE MAY 31 1983

DASH NO	NUMBER	QTY
-20	0114-1000	1
-10	0114-[illegible]	1

NEXT ASSEMBLY

-50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV | DATE

DRAWN | DATE

CHECKED | 7/20/81

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY, INPUT BD.

SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0225	D

CODE | SHEET 1 OF 1

COMM		COST	COST
[1] -10 ONLY			

	60	-50	-40	-30	-20	-10	NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	[illegible]ION	TYPE
1					1	1	0114-0227	P.C.B.				
2												
3												
4					1	1	3000-1500	RESISTOR	R1		150Ω, 1/4W, 5%	
5					2	2	2950-1006	RESISTOR	R2,3		10Ω, 1/8W, 5%	
6					1	1	6400-0041	LED	CR1		GRN	
7					4	6	6000-0406	HEADER	J3A, J3B, J4A, J4B [1] J3C, J4C		16 PIN, RT ANGLE	
8					1	1	6000-0405	HEADER	J5		34 PIN, RT ANGLE	
9					4	6	6000-0404	"D" CONN	J1A J1B J2A J2B [1] J1C, J2C		25 PIN	
10					A/R	A/R	7200-0025	MOUSE TAIL				
11												
12					2	2	6000-0041	CONN	DVM IN, DVM GND		8-32 TIP PLUG	
13					1	1	0114-0055	CABLE ASSY				LM
14												
15					A/R	A/R	7200-0050-14	SHRINK TUBING, 3/16"			DVM IN, DVM GND	
16												
17												
18												

ASSEMBLY TIME | COMPONENT NG

APR 14 1983

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN #0161	6-30-81	SR	DC	
B	REVISED PER ECO# 2225	1-19-83	[illegible]	MG	1/1/82
C	REVISED PER ECO #3503 A	3-2-83	MW	DGW	3-15-83
D	REVISED PER ECO #3602	4-12-83	MW	DGW	4/13/83

DASH NO.	NUMBER	QTY
-20	0114-1008	1
-10	0114-0008	1

NEXT ASSEMBLY

		DATE
DRAWN	S. RODELL	6-30-81
CHECKED	D LeVARDI	7-20-81
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
ASSEMBLY,
INPUT BD.

biomation

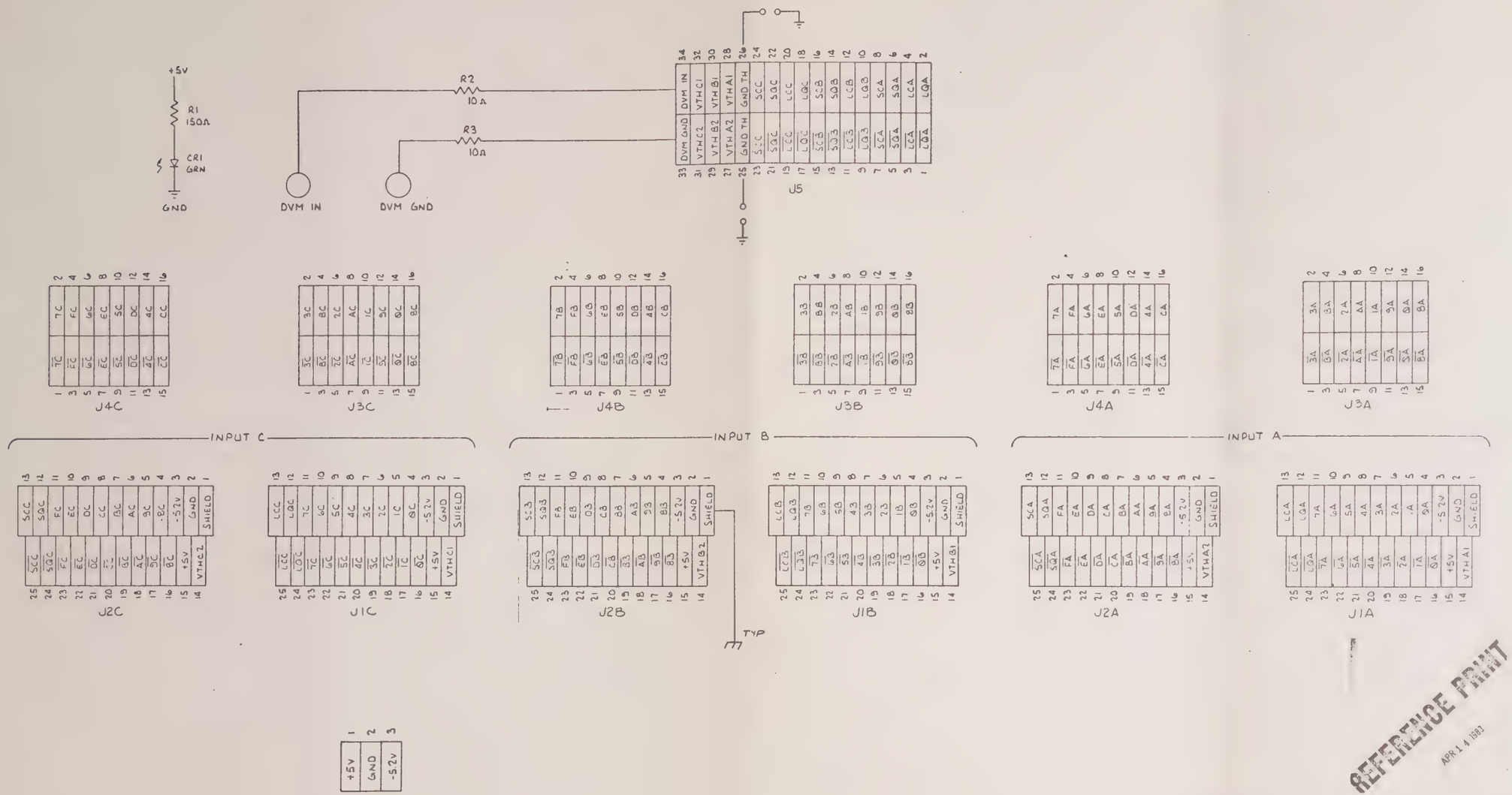
B | 0114-0225 | REV D

MODEL K101/2 | CODE | SHEET 1 OF 1

DWG NO	SH	REV
0114-0226	1	

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	[illegible]	PILOT REL PER ECN # 0161	[illegible]	DL	[illegible]
	B	[illegible]	REVISED PER ECO [illegible]	[illegible]	[illegible]	[illegible]
	C	3538	REVISED PER ECO [illegible]	[illegible]	[illegible]	[illegible]
	D	3602	REVISED PER ECO [illegible]	[illegible]	[illegible]	[illegible]



REFERENCE PRINT
APR 14 1983

DASH NO	NUMBER	QTY
-10	0114-0225	REF
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV | DATE

PART NUMBER | PART NAME | DESCRIPTION SPECIFICATION | ITEM

DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR

GOULD biomation

TITLE: SCHEMATIC, INPUT BD

SCALE	SIZE	PART NUMBER	REV
	D	0114-0226	D

CODE | SHEET | OF

DATA DISPLAY BOARD
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0191

A. CRT CONTROLLER- (SHEET 3 OF SCHEMATIC)- THE DESIRED CRT DISPLAY PATTERN IS COMPUTED BY THE MICROPROCESSOR AND STORED IN THE RAM AS A COMPLETE DOT MAP; EVERY DOT LOCATION OF THE CRT IS REPRESENTED BY A BIT IN THE RAM ("1" = WHITE, "0" = BLACK).

B. TYPICAL PROCEDURE:
   1. THE CRT DISPLAY ADDRESSES ARE ALL SET TO ZERO (BLANKING THE CRT).
   2. THE MICROPROCESSOR CONVERTS EACH DISPLAYED CHARACTER INTO A PATTERN OF "1's" AND "0's" AND STORES THEM IN THE PROPER LOCATIONS IN RAM.
   3. THE CRT CONTROLLER CONTINUOUSLY CYCLES THROUGH THE RAM AND TRANSLATES THE INFORMATION TO THE CRT. A 16 BIT WORD IS READ FROM THE RAM EVERY 2 us AND CONVERTED INTO A STRING OF 16 DOTS ON THE CRT.

C. THE CRT CONTROLLER GENERATES A STANDARD RASTER SCAN DISPLAY FORMAT WITH DATA BEING PRESENTED AS A SERIES OF HORIZONTALLY SCANNED LINES.
   1. EACH LINE STARTS AT THE LEFT AND GOES TO THE RIGHT.
   2. FIRST LINE IS AT THE TOP AND THE LAST IS AT THE BOTTOM.
   3. STANDARD SYNC AND BLANKING SIGNALS ARE GENERATED.

D. HORIZONTAL TIMING- EACH HORIZONTAL SCAN LINE IS 64us LONG AND PRESENTS 52us OF VIDEO WITH 12 us BLANKED AND A 6 ns SYNC PULSE DURING THE BLANK TIME.
   1. THE HORIZONTAL COUNTER (LS161 LOCATION 9A AND 10A) RUNS CONTINOUSLY AT A 500 kHz RATE GENERATING THE FIVE ADDRESS LINES FOR THE HORIZONTAL ROM (10B)

2. THE HORIZONTAL ROM (10B) DECODES THE ADDRESS TO PRODUCE THE BLANKING, SYNC, AND TOP COUNT (END OF LINE) PULSES. (74LS175 LOCATION 9B)

3. HORIZONTAL BLANKING INTERVAL OCCURS FOR THE FIRST 12 us AFTER THE COUNTER ROLLS OVER, STATES 0 THROUGH 5 (9B PIN 7).

4. THE SYNC PULSE (9B-3) STARTS 2us AFTER THE BLANKING AND LASTS 6 us.

5. IN ADDITION TO ADDRESSING THE ROM, THE FIFTH ADDRESS LINE IS USED BY THE HORIZONTAL DRIVE FOR THE DEFLECTION. (LOCATION 10C-10)

E. VERTICAL TIMING - THE VERTICAL TIMING CYCLE STARTS WITH COUNTERS PRESET TO 7200 (HEX).

1. AFTER COUNTING 290 LINES THE HORIZONTAL AND VERTICAL PROMS DECODE TOP COUNT AND RESET THE COUNTER TO 7200 (HEX).

2. SIMULTANEOUS WITH VERTICAL TOP COUNT, THE VERTICAL PROM GENERATES "PRESET ADDRESS COUNTER" WHICH SYNCHRONIZES THE TRACKING ADDRESS COUNTER ON THE MPU BOARD.

3. VERTICAL SYNC PULSE IS DECODED TO OCCUR AT LINE 35 (HEX).

4. THE K101-D OPERATES AT A 50 HZ SCAN RATE AT ALL TIMES!

F. HORIZONTAL DEFLECTION AND HIGH VOLTAGE - (SHEET 1 OF SCHEMATIC)

THE HORIZONTAL DRIVE SIGNAL FROM THE CRT CONTROLLER SYNCHRONIZES THE HORIZONTAL SCANNING WITH THE RETRACE BLANKING BY CONTROLLING THE HORIZONTAL DRIVE TRANSISTOR (Q5).

1. THE HORIZONTAL DRIVE TRANSISTOR (Q5) SERVES TWO PURPOSES; IT PROVIDES ENERGY TO THE FLYBACK TRANSFORMER, AND IT DRAWS CURRENT FROM THE HORIZONTAL DEFLECTION COIL TO GENERATE THE SCAN FROM LEFT TO RIGHT.

2. THE FLYBACK TRANSFORMER (T2) PROVIDES THE ENERGY FOR THE RAPID RETRACE FROM RIGHT TO LEFT AND IT SERVES AS A DC TO DC CONVERTER FOR GENERATING THE OPERATING VOLTAGES FOR THE CRT.

   VOLTAGES SUPPLIED TO THE CRT:

+10 KV	CRT ANODE
+200 V	FOCUS
+30 V	CATHODE
-40 V	CRT GRID

3. FOCUS ADJUSTMENT (R29) AND BRIGHTNESS ADJUSTMENT (R32) ARE LOCATED ON THIS BOARD.

4. HORIZONTAL WIDTH (L1) AND LINEARITY (L2) ARE ALSO PRESENT.

G. VERTICAL DEFLECTION- (SHEET 2 OF SCHEMATIC)- THE VERTICAL PROCESSOR GENERATES AND SYNCHRONIZES THE VERTICAL SCANNING.

1. THE VERTICAL PROCESSOR DRIVES THE VERTICAL DEFLECTION DEFLECTION COIL DIRECTLY, AND SENSES THE CURRENT THROUGH THE COIL THROUGH A SENSE RESISTOR.

2. THE TDA 1270 PROCESSOR (11B) CONTAINS AN OSCILLATOR THAT IS SYNCHRONIZED TO THE VERTICAL SYNC PULSE, AN ADJUSTABLE CONSTANT CURRENT SOURCE RAMP GENERATOR, AN EMITTER FOLLOWER AND A POWER AMPLIFIER TO DRIVE THE COIL.

3. THE VERTICAL PROCESSOR CIRCUITRY ALLOWS ADJUSTMENT OF VERTICAL HOLD (R21), VERTICAL HEIGHT (R20), AND VERTICAL LINEARITY (R47).

H. VIDEO - CONTROLLING THE BRIGHTNESS ON THE CRT IS DONE BY COMBINING THE DIGITAL DATA WITH THE HORIZONTAL AND VERTICAL BLANKING SIGNALS AND SWITCHING THE CATHODE VOLTAGE BETWEEN OV (WHITE) AND +30 V (BLACK).

1. TO PROVIDE A SHARPER DISPLAY PRESENTATION THE VIDEO IS MODULATED BY AN 8 MHZ CLOCK SIGNAL.

2. A COMPOSITE VIDEO SIGNAL IS ALSO GENERATED AND IS AVAILABLE AT THE REAR PANEL FOR USE WITH ANOTHER VIDEO MONITOR.

I. KEYBOARD AND FRONT PANEL INTERFACE - (SHEET 4) - THE KEYBOARD AND THE FRONT PANEL ARE ADDRESSED BY THE MICRO-PROCESSOR AT THE SAME TIME.

1. THE INTERFACE CIRCUITRY DECODES EIGHT ADDRESSES OUT OF THE I/O MAP.

2. EACH ROW IS READ AS A BYTE AT A 60 HZ RATE (OR 50 HZ DEPENDING ON THE VERTICAL RATE SELECTED), ANY KEY CONTACT THAT IS CLOSED WILL BE STORED AS A ZERO WITHIN THAT BYTE.

3. EACH BIT OF THE BYTE CORRESPONDS TO A COLUMN ON THE KEYBOARD.

J. INTERRUPT PROCESSOR - (SHEET 4) - THE INTERRUPT STRUCTURE OF THE K101-D HAS BEEN DESIGNED TO HANDLE UP TO EIGHT LEVELS OF INTERRUPTS USING A 8295A INTERRUPT PROCESSOR (IC 2E). (CURRENTLY ONLY 6 LEVELS ARE REQUIRED)

INTERRUPT LEVELS ARE AS FOLLOWS:

LEVEL	ASSIGNMENT
7	----------
6	1 SECOND (TIME OF DAY CLOCK)
5	----------
4	TIMER #Ø
3	RS449 (USART #2)(RxRDY+TxRDY)
2	RS232 (USART #1)(RxRDY+TxRDY)
1	GPIB
Ø	50 HZ (CRT INTERRUPT)

K. CMOS RAM SAVE CIRCUIT - (SHEET 5) - CIRCUITRY IS PROVIDED TO ALLOW THE OPERATOR TO STORE A COMPLETE SET OF RECORDING PARAMETERS FOR USE AFTER POWER DOWN.

IF THE UNIT IS ACCIDENTALLY POWERED DOWN THE SAVE CIRCUIT WILL AUTOMATICALLY STORE THE PARAMETERS LAST DISPLAYED ON THE SCREEN.

1. A 2.9 V BATTERY PROVIDES POWER TO THE TWO CMOS RAMS (LOCATIONS 1B AND 3B) ONCE THE UNIT IS POWERED DOWN.
2. DATA TO AND FROM THE 6116 RAMS IS OVER A BI-DIRECTIONAL DATA BUS VIA THE TWO BUFFERS AT 3C AND 4C.

L. REAL TIME CLOCK - (SHEET 6) - THE HEART OF THE CLOCK CIRCUIT IS A MSM5832 MONOLITHIC, METAL GATE CMOS INTEGRATED CIRCUIT THAT FUNCTIONS AS A REAL TIME CLOCK.

M. BEEPER CIRCUIT - (SHEET 4) - THIS CIRCUIT PROVIDES A LOW LEVEL BEEP WHEN IMPROPER KEYBOARD ENTRIES ARE ATTEMPTED.

1. BEEP LENGTH IS PROGRAMMABLE.

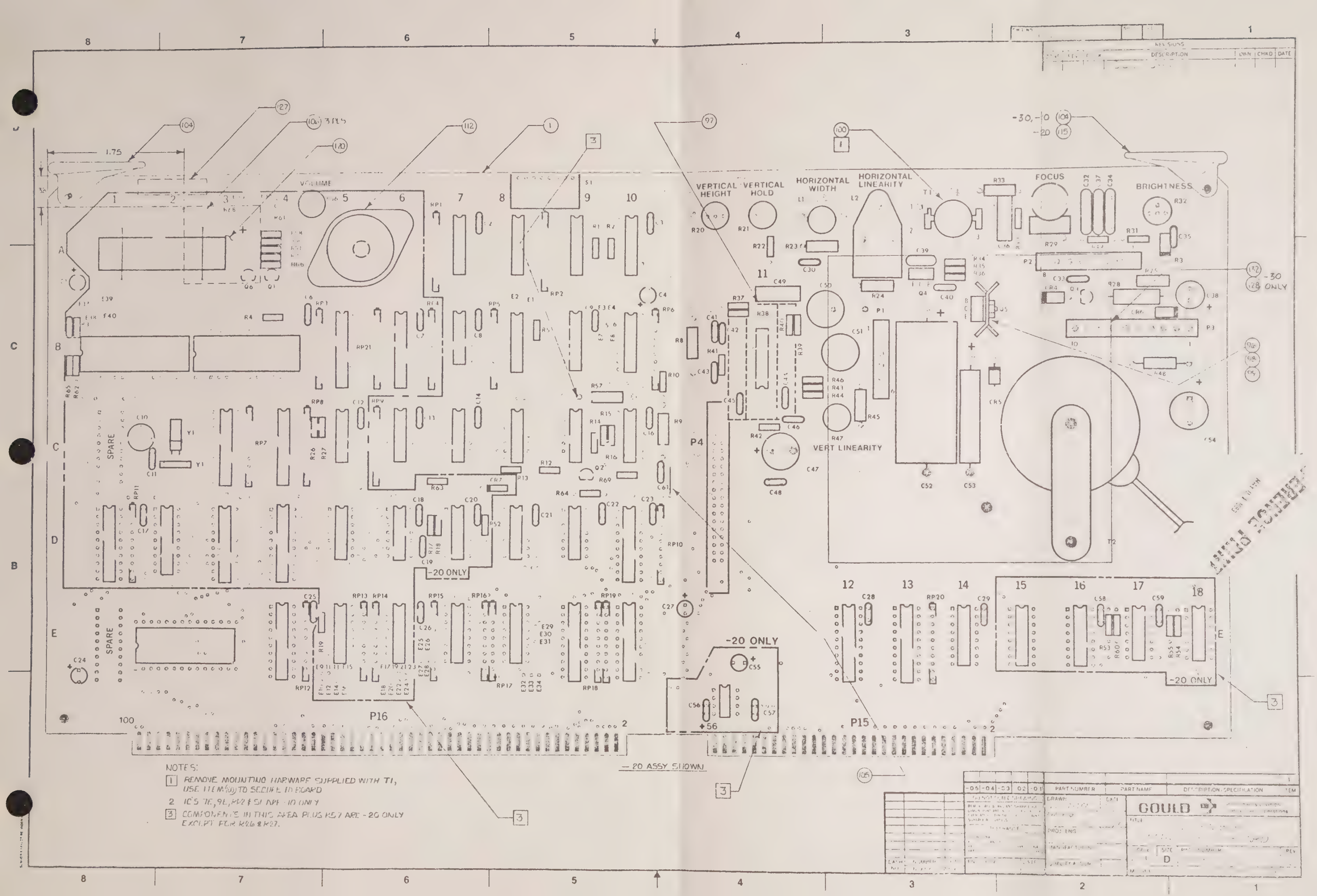
JUMPER	AS ETCHED	-20 K101/K102	-10 / -30 K500/K105	DESCRIPTION
E1 TO E2	OUT		JUMPER FOR 50HZ ONLY	CRT SCAN RATE IN-50HZ. OUT-60HZ
E3 TO E4	OUT			NOT USED
E5 TO E6	OUT			NOT USED
E7 TO E8	OUT		JUMPER	IN K500 HORIZ. SCAN OUT-K101
E9 TO E10	OUT			A18
E11 TO E12	IN			A17
E13 TO E14	IN			A16
E15 TO E16	IN			A15 — K101 CMOS RAM
E17 TO E18	IN			A14 — ADDRESS SELECTION
E19 TO E20	IN			A13
E21 TO E22	IN			A12
E23 TO E24	IN			A19
E25 TO E26	IN			A8 — K500 MEM MAPPED I/O
E27 TO E28	IN			A7 — ADDRESS DECODE
E29 TO E30	IN		CUT	IN SELECTS I/O MAPPED I/O (K101)
E30 TO E31	OUT		JUMPER	IN SELECTS MEM MAPPED I/O (K500)
E32 TO E33	IN		CUT	IN FOR K101
E33 TO E34	OUT		JUMPER	IN FOR K500

GOULD biomation

TITLE: ASSEMBLY DATA DISPLAY BD

SCALE 2/1 | SIZE D | PART NUMBER 0014-2013 | REV C

SHEET 1 OF 2


VOLUME
VERTICAL HEIGHT
VERTICAL HOLD
HORIZONTAL WIDTH
HORIZONTAL LINEARITY
FOCUS
BRIGHTNESS
VERT LINEARITY
SPARE
SPARE
-20 ONLY
-20 ONLY
-20 ONLY
-30 ONLY
-20 ASSY SHOWN
P4
P15
P16
NOTES:
1 REMOVE MOUNTING HARWARE SUPPLIED WITH T1, USE ITEM (100) TO SECURE TO BOARD
2 IC'S 7E, 9E, RP2 & SI ARE -10 ONLY
3 COMPONENTS IN THIS AREA PLUS R57 ARE -20 ONLY EXCEPT FOR R26 & R27.
GOULD
D

1				1	1	1	0114-2012	PWB					
2				2	3	2	3000-2000	RESISTOR	R35, 36 [1] R64		200Ω, 1/4W, 5%		
3				1	1	1	3000-3307	RESISTOR	R38		3.3Ω, 1/4W, 5%		
4				2	2	2	3050-4700		R8, 9		470Ω, 1/2W, 5%		
5				1	1	1	3000-8206		R12		82Ω, 1/4W, 5%		
6				2	2	2	-4700		R5, 34		470Ω		
7				2	12	2	-2201		[3] R1, 2 [1] R19, 1, 2, 53-55, 58, 3, 4, 60, 62, 65		2.2K		
8				—	4	—	-1002		R17, 18, 52, 63		10K		
9				1	1	1	-5601		R46		5.6K		
10				2	2	2	-8201		R39, 40		8.2K		
11				2	2	2	-4702		R43, 44		47K		
12				1	1	1	-1203		R22		120K		
13				1	2	1	-2203		R41 [1] R37		220K		
14				1	1	1	-2703		[3] R37 [1] R42		270K		
15				1	1	1	-5103		R31		510K		
16				1	—	1	-6803		R42		680K		
17				2	2	2	3000-1004	RESISTOR	R30, 49		1M[illegible] 5%		
18				1	1	1	3050-2200	RESISTOR	R24		22Ω, 1/2W, 5%		

[1] USED ON -20 ONLY

[2] USED ON -10 ONLY

-10 K500

-20 K101/K102

-30 K105

[3] -10, -30

ASSEMBLY TIME	COMPONENT LEAD SPACING
	1/4W RES -.40 1/8W RES -.40 1/2W RES -.50 1W RES -.70

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROD. REL PER ERN # 295	12/[illegible]	M.W.	[illegible]	
B	" " " " # 302	[illegible]			
C	REVISED PER ECO # 3684A	5/2/83	MW	DW	5/4/[illegible]

DASH NO.	NUMBER	QTY
-20	0114-1002	1
-30	0117-0003	1
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

		DATE
DRAWN	M.W	11/82
CHECKED	[illegible]	12/6/82
ENGINEER	[illegible]	1/26/83
MANUFACTURING	[illegible]	1/27/83
QUALITY ASSURANCE	[illegible]	1/27/83

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

MODEL K101/K500

biomation

B | 0114-2010 | REV C

CODE | SHEET | OF 8

19				1	1	1	3050-1007	RESISTOR	R45		1.0 Ω, 1/2W, 5%	
20				1	2	1	3050-3906		R25 [1] R57		39 Ω, 1/2W, 5%	
21				1	1	1	3050-1000		R33		100Ω, 1/2W, 5%	
22				1	1	1	SELECTED AT TEST		R23		S.A.T.	
23				—	2	—	3000-2202		R67,68		22K, 1/4W, 5%	
24				1	1	1	3200-0008		R48		1.0 Ω, 1W, 3%	
25				1	1	1	3070-1501		R28		1.5 KΩ, 1W, 5%	
26				1	1	1	3100-7500		R13		75 Ω, 1/8W, 1%	
27				1	1	1	3100-6040		R14		604	
28				1	1	1	3100-8250		R15		825	
29				1	1	1	3100-9090	RESISTOR	R16		909 Ω, 1/8W, 1%	
30				1	1	1	3300-0084	RES. VAR.	R47		70K	
31				3	3	3	3300-0085		R20,21,32		100K	
32				1	1	1	3300-0088	RES. VAR.	R29		1MEG	
33				1	1	1	4100-0024	CAPACITOR	C43		68 PF, 500V MICA	
34				1	1	1	4100-0002		C39		470PF, 500V MICA	
35				6	8	6	4000-0009		C33,35,42,44-46 [1] C5,6, C1,C4,C24,C27		0.1UF, 100V	
36				4	5	4	4400-0043	CAPACITOR	[1] C19		47 UF, 6V	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	M. WOLFE	DATE 11/22/82
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

MODEL K101/K500

biomation

B 0114-2010

CODE

SHEET 2 OF 5

37				2	2	2	4000-0042	CAPACITOR	C36,49		.15µF, 100V	
38				1	—	1	4400-0039		C50		10 uf / 16V	
39				3	3	3	4000-0043		C32,34,37		.01µF, 500V	
40				17	26	17	4010-0103		C40,41,2,3,8,9,13,14,16,21-23,25,26,28,29,48 [1] C7,12,17,18,20,56,57,58,59		.01µF, 50v	
41				—	1	—	4010-0100		C11		10pf, 100v	
42				1	1	1	4400-0036		C51		1000µF, 16V	
43				2	2	2	4400-0037		C47,54		470µF, 25V	
44				—	1	—	4400-0047		C50		220µF, 35v	
45				1	1	1	4200-0036-10	CAPACITOR	C52		6µF, 200V	
46				1	1	1	4400-0038	CAPACITOR	C38		10µf, 100V	
47				—	1	—	7000-0451	BATTERY	B1	POWER CONV INC.	2.4V NICD	
48				1	1	1	1200-0033	DIODE	CR5	3SF4		
49				3	3	3	1200-0031	DIODE	CR3,4,6	IN4937		
50				1	1	1	4300-0041	CAPACITOR	C53		.056µf, 400V	
51				—	1	—	3000-3900	RESISTOR	R66		390Ω, 1/4W, 5%	
52				1	3	1	6100-0151	SOCKET	X2E / [1] X1B, X3B		28 PIN	
53				1	1	1	SELECTED AT TEST	CAPACITOR	C30		S.A.T.	
54				—	1	—	4600-0010	CAP, VAR	C10		7-40 Pf	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. WOLFE DATE 11/22/82

CHECKED

ENGINEER

MANUFACTURING

QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

MODEL K101/K500

biomation

B 0114-2010 REV C

CODE

SHEET 3 OF 8

55				1	2	1	1300-0028	TRANSISTOR	Q2, [1] Q6	2N3904					
56				1	1	—	1400-0019		Q1	2N3906					
57				1	1	1	1300-0049		Q5	BV407					
58				1	1	1	1300-0048	TRANSISTOR	Q4	2N4921					
59				2	2	3	6100-0120	SOCKET	XS1 [2] X8B, X10B		16 PIN				
60				—	1	1	3000-6800	RESISTOR	R51		680Ω, 1/4W, 5%				
61				—	—	1	0950-0195	IC	10B		PROM, HORIZ				
62				7	8	8	3700-0083	RESISTOR PACK	RP1,5,6,9,12,15,20, [2] RP2 [1] RP14		2.2KΩ, 10 PIN SIP				
63				—	5	—	3700-0085		RP 3,7,8,11,21		22KΩ 10 PIN SIP				
64				5	7	5	3700-0049	RESISTOR PACK	RP10,16-19 [1] RP4,13		3K/6.2KΩ 10PIN SIP				
65				1	1	1	1500-0018	TRANSISTOR	Q3		VN10KM				
66				1	1	1	1800-0105	I.C.	7C	74LS00					
67				1	1	1	1800-0123		6C	74LS14					
68				1	2	1	-0110		9D [1] 5D	74LS10					
69				1	1	1	-0111		8D	74LS20					
70				1	2	1	-0115		7B [1] 17E	74LS74					
71				—	2	1	-0254		[2] 7E [1] 5E,6E	74LS85					
72				1	1	1	1800-0404	I. C.	9C	74LS136					

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME

COMPONENT LEAD SPACING

DRAWN M. WOLFE	DATE 11/22/82	
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

DASH NO. | NUMBER | QTY
NEXT ASSEMBLY

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

MODEL K101/K500

B | 0114-2010 | REV 1.0

CODE | SHEET 4 OF 8

73				1	1	1	1800-0301	I.C.	14E	74LS156		
74				4	6	4	-0125		7A-10A; 1 15E,16E	74LS161		
75				1	1	1	-0121		9B	74LS175		
76				2	3	2	-0267		10D, 4E; 1 6B	74LS240		
77				1	3	2	-0240		13E, 2 9E; 1 5B, 1 1D	74LS244		
78				1	3	1	-0268		10E; 1 3C,4C	74LS245		
79				1	3	1	-0231		12E; 1 3D 4D	74LS273		
80				1	1	1	-0193		8E	74LS138		
81				1	2	1	-0097		10C; 1 18E	7406		
82				1	1	1	1800-0038		3C	74S20		
83				—	1	—	0114-0064		8B		PROM, VERTICAL	
84				—	2	—	1820-0080		1B,3B		IC/ST RAM CMOS	
85				1	1	1	1800-0319		2E	8259-A		
86				—	1	—	0114-0065		10B		PROM, HORIZONTAL	
87				1	1	1	1700-0082		11B	TDA-1270	VERTICAL PROCESSOR	
88				—	1	—	1800-0341		2D	MSM5832		
89				—	1	—	1800-0311	I.C.	7D	7438		
90				—	-	1	0950-0194	I.C.	8B		PROM, VERT	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN M. WOLFE	DATE 11/22/82	
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B 0114-2010 REV C

MODEL K101/K500 CODE SHEET 5 OF 8

	-60	-50	-40	-30	-20	-10			REF DESIGNATION	VENDOR NO.		
91				1	1	1	9000-0049	COIL ASSY, WTH	L1		5-30 µH	
92				1	1	1	0113-0011	COIL ASSY, LIN	L2			
93				—	1	—	5100-0018	CRYSTAL	Y1		32.768 KHZ	
94				1	1	1	0113-0014	TRANSFORMER	T1			
95				1	1	1	9000-0082	TRANSFORMER	T2		FLYBACK	
96				1	1	1	7000-0365	HEATSINK	@ Q5			
97				1	1	1	7000-0366	HEATSINK	@ 11B			
98				1	1	1	7000-0221	INS. WASH	@ Q5			
99				1	1	1	7200-0017	INSULATOR	@ Q5			
100				1	1	1	2400-0004	MTG BRACKET	@ T1			
101				1	1	1	6000-0359-6	HEADER	P1		6PIN	
102				1	1	1	6000-0359-8	↕	P2		8PIN	
103				1	1	1	6000-0359-10	HEADER	P3		10PIN	
104				2	1	2	7000-0120	EJECTOR				
105				1	1	1	9000-0054	GND WIRE				
106				—	3	—	7200-0032	MOUSE TAIL			.115 DIA, 4"	
107				—	—	1	6600-0037	DIP SWITCH	S1			
108				2	2	2	3000-1001	RESISTOR	R10, 69		1K, 1/4W, 5%	

		COST	COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN M. WOLFE	DATE 11/22/82	
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B	0114-2010	REV C
CODE		SHEET 6 OF 8

MODEL K101/K500

109				1	1	1	3000-2200	RESISTOR	R26			220Ω, 1/4W, 5%	
110				1	1	1	3000-3300	RESISTOR	R27			330Ω, 1/4W, 5%	
111				—	1	—	3300-0096	RES., VAR.	R56			1K, 1 TURN	
112				—	1	—	7400-0002	BEEPER					
113				—	1	—	1700-0071	I.C.	11C			LF356	
114				—	1	—	4400-0045	CAPACITOR	C55			33µf, 25v	
115				—	1	—	0112-0228-08	EJECTOR, STAMPED				"A8"	
116				—	1	—	1800-0351	I.C.	5C			74LS12	
117				—	1	—	1800-0352	I.C.	6D			74LS22	
118				—	1	—	3000-5106	RESISTOR	R61			51Ω, 1/4W, 5%	X
119				—	1	—	1000-0002	DIODE	CR7			1N4152	X
120				—	A/R	—	8300-0027	INSULATION	3M4108			1"x 1" x 1/8" THK	
121				—	1	—	4000-0011	CAPACITOR	C61			2.2 uf	
122				—	1	—	6000-0389	HEADER	P4			34 PIN - FLOPPY	
123				—	1	—	6100-0146	SOCKET	2D			18 PIN	
124													
125				—	1	—	3000-2700	RESISTOR	R7			270Ω, 1/4W, 5%	
126				—	1	—	3000-3301	RESISTOR	R50			3.3K, 1/4W, 5%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN M. WOLFE	DATE 11/22/82	
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV C

MODEL K101/K500 | CODE | SHEET 7 OF 8

ITEM	-90	-80	-70	-60	-50	-40	-30	-20	-10				
127							–	1	–	0114-0432	LABEL, CAUTION NICD ONLY!		1
128							2	–	–		SCREW		X
129							1	–	–	0117-0149-10	PROM, VERT, K105	8B	
130							1	–	–	0117-0150-10	PROM, HORIZ, K105	10B	
131													
132							1	–	–	0117-0139-10	SHIELD, DEFLECTION		X
133													X
134													X

NOTES

LIST OF MATERIAL

DATA DISPLAY PWA ASSY

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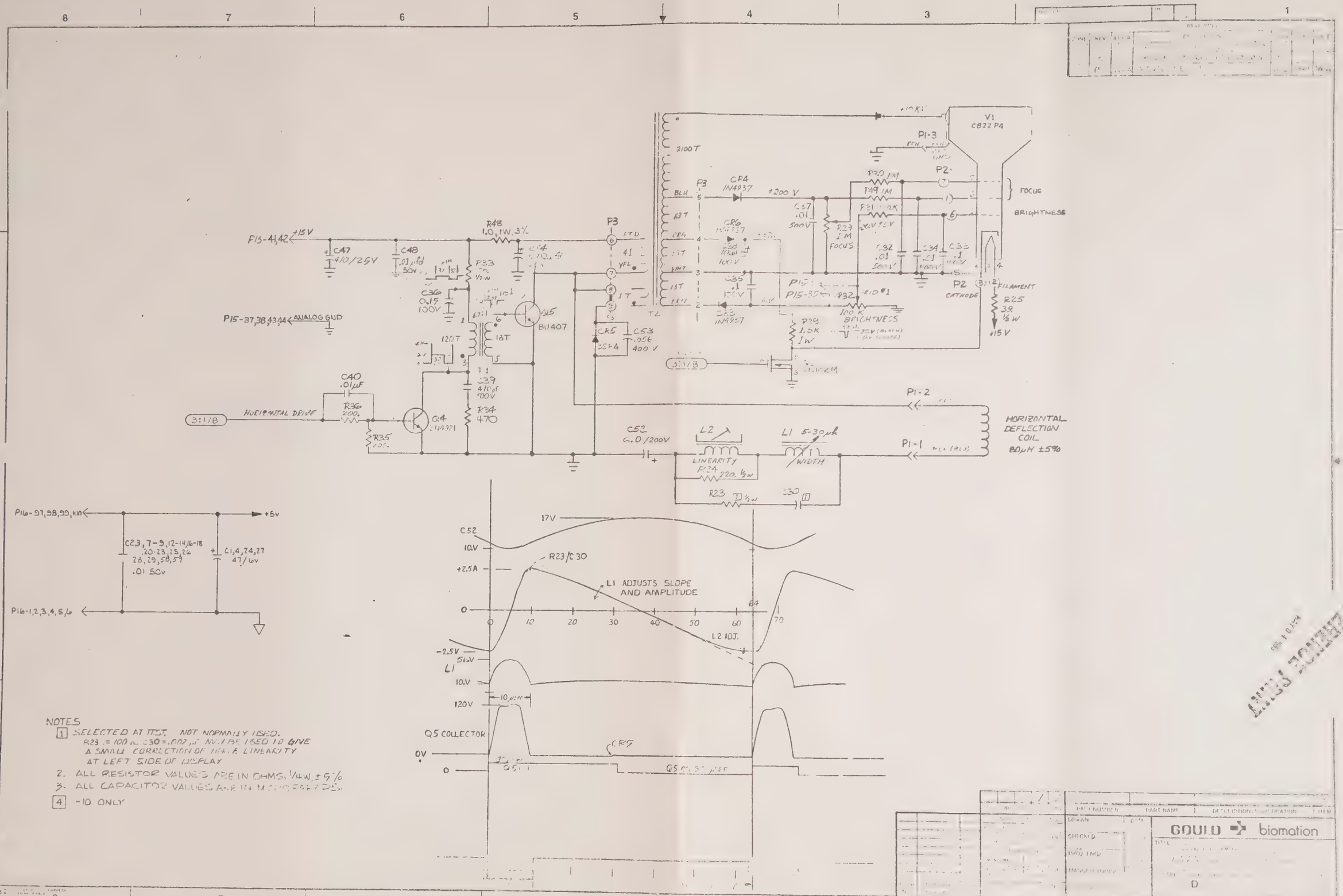
B 0114-2010 REV C

MODEL K101/K500 SHEET 8 OF 8

KLINGLER K-VEL H-10



NOTES

1. SELECTED AT TEST. NOT NORMALLY USED. R23 = 100 Ω C30 = .002 µf MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ LINEARITY AT LEFT SIDE OF DISPLAY
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. -10 ONLY

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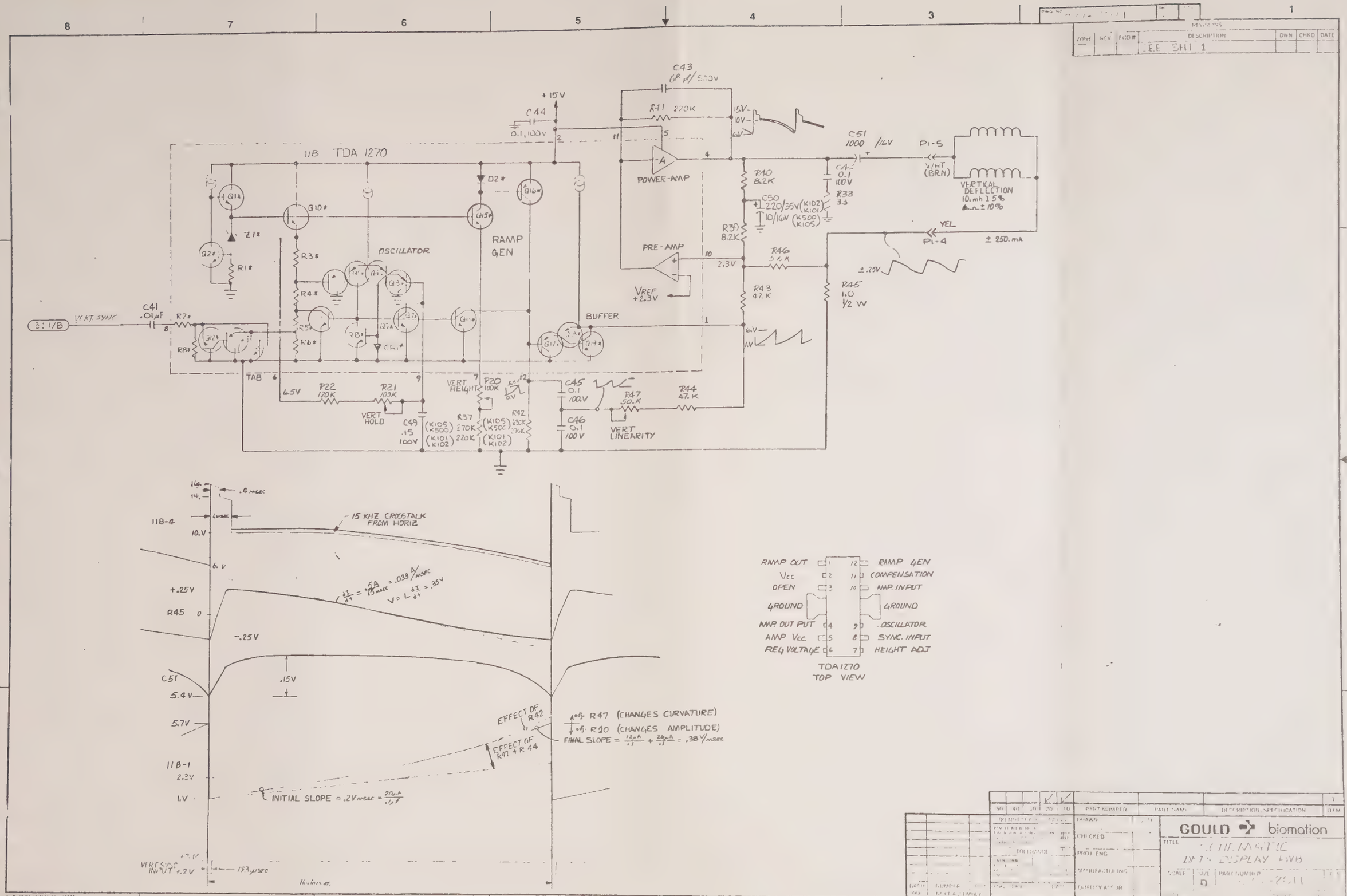
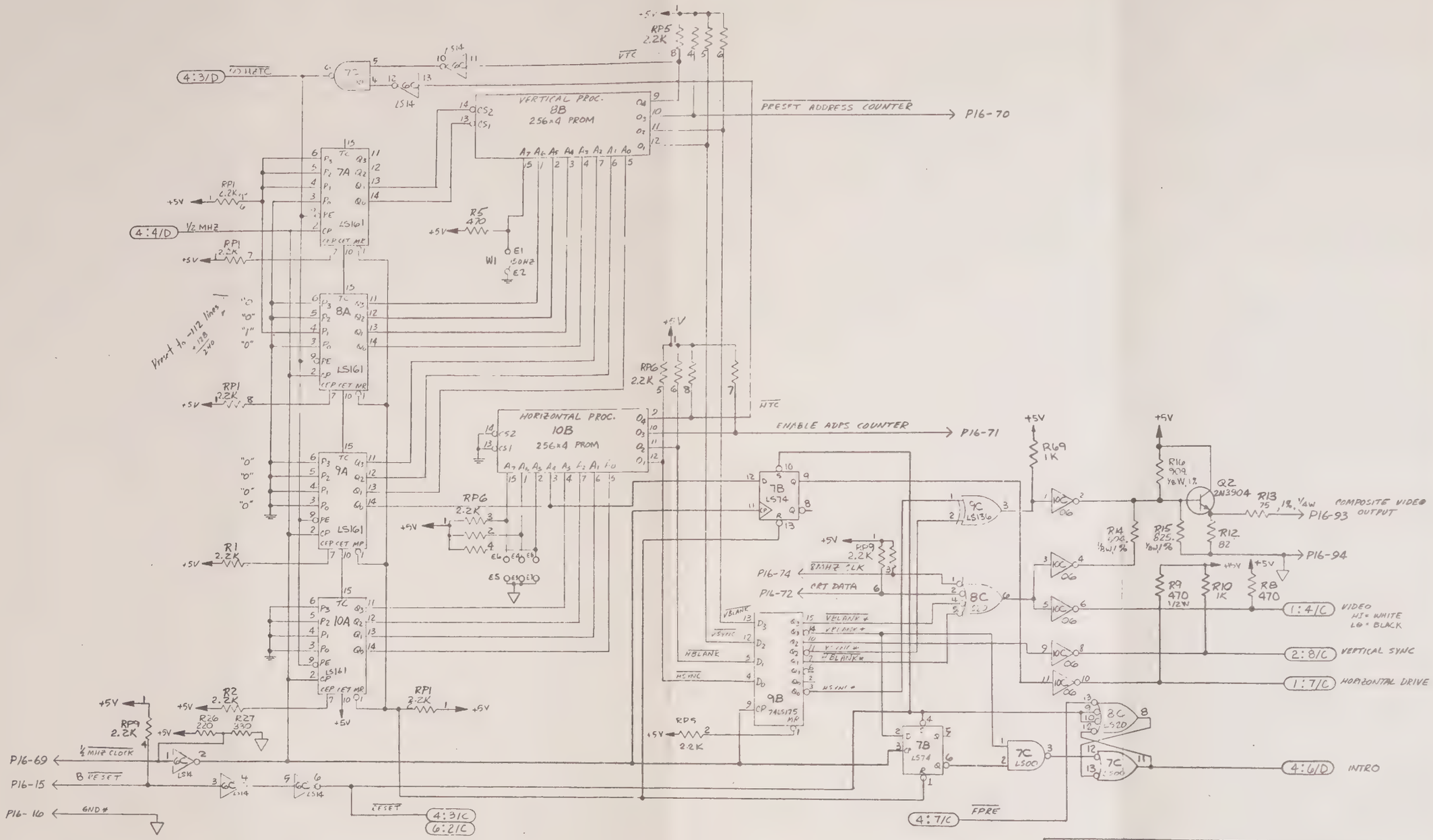


11B TDA 1270
OSCILLATOR
RAMP GEN
BUFFER
POWER-AMP
PRE-AMP
VREF +2.3V
VERT. SYNC
C41 .01µF
R7*
R8*
R1*
R3*
R4*
R5*
R6*
Q1*
Q2*
Q10*
Q15*
Q16*
Q17*
Q13*
Z1*
D2*
TAB
6.5V
R22 120K
R21 100K
VERT HOLD
C49 .15 100V
VERT HEIGHT
R20 100K
R37 270K 220K
R42 630K 270K
C45 0.1 100V
C46 0.1 100V
R47 50.K
VERT LINEARITY
R44 47.K
C44 0.1, 100V
+15V
C43 68 pf/500V
R41 220K
15V
10V
6V
R40 8.2K
C50 220/35V (K102 K101) 10/16V (K500 K105)
R39 8.2K
R46 5.6K
R43 47.K
R45 1.0 1/2 W
C51 1000 /16V
C42 0.1 100V
R33 3.3
P1-5
WHT (BRN)
VERTICAL DEFLECTION 10.mh ± 5% 6.Ω ± 10%
YEL
P1-4
± 250. mA
±.25V
11B-4
10.V
6.V
.4 msec
15 KHZ CROSSTALK FROM HORIZ
+.25V
R45 0
-.25V
dI/dt = .5A/15 msec = .033 A/msec
V = L dI/dt = .35V
C51
5.4V
5.7V
.15V
11B-1
2.3V
1.V
EFFECT OF R42
EFFECT OF R47 + R44
adj. R47 (CHANGES CURVATURE)
adj. R20 (CHANGES AMPLITUDE)
FINAL SLOPE = 12µA/.1 + 26µA/.1 = .38 V/msec
INITIAL SLOPE = .2V msec = 20µA/.1µF
VERT SYNC INPUT +.2V
193 µsec
RAMP OUT
Vcc
OPEN
GROUND
AMP OUT PUT
AMP Vcc
REG VOLTAGE
RAMP GEN
COMPENSATION
AMP. INPUT
GROUND
OSCILLATOR
SYNC. INPUT
HEIGHT ADJ
TDA 1270
TOP VIEW
GOULD biomation
TITLE
SCHEMATIC
DATA DISPLAY PWB
SCALE
SIZE D
PART NUMBER
DESCRIPTION, SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
TOLERANCE

DWG NO	SH	REV
[illegible]		C

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



DASH NO	NUMBER NEXT ASSEMBLY	QTY

-50	-40	30	20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING

TOLERANCE

ENG SERV | DATE

DRAWN | DATE

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

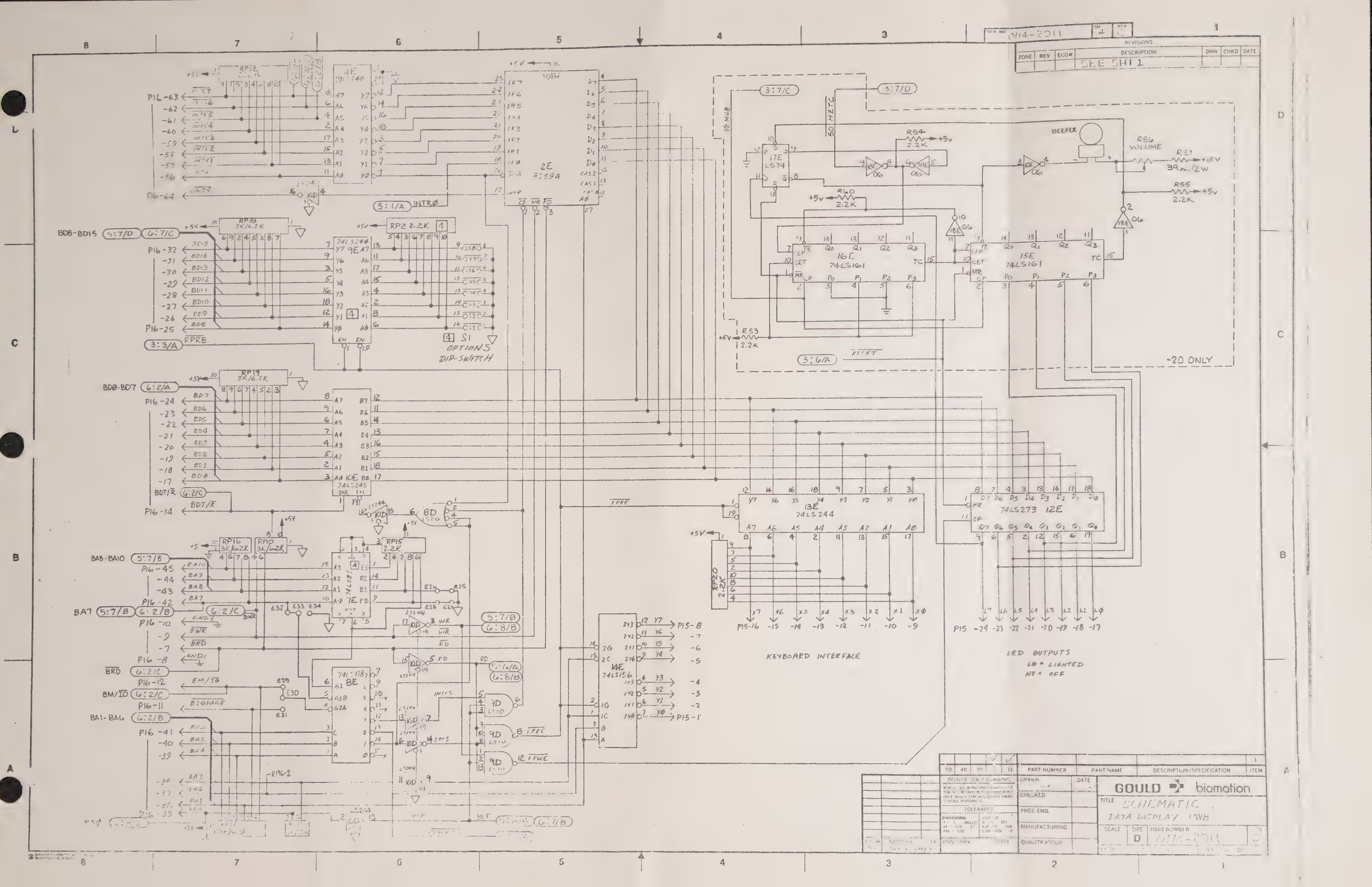
GOULD biomation

TITLE [illegible]

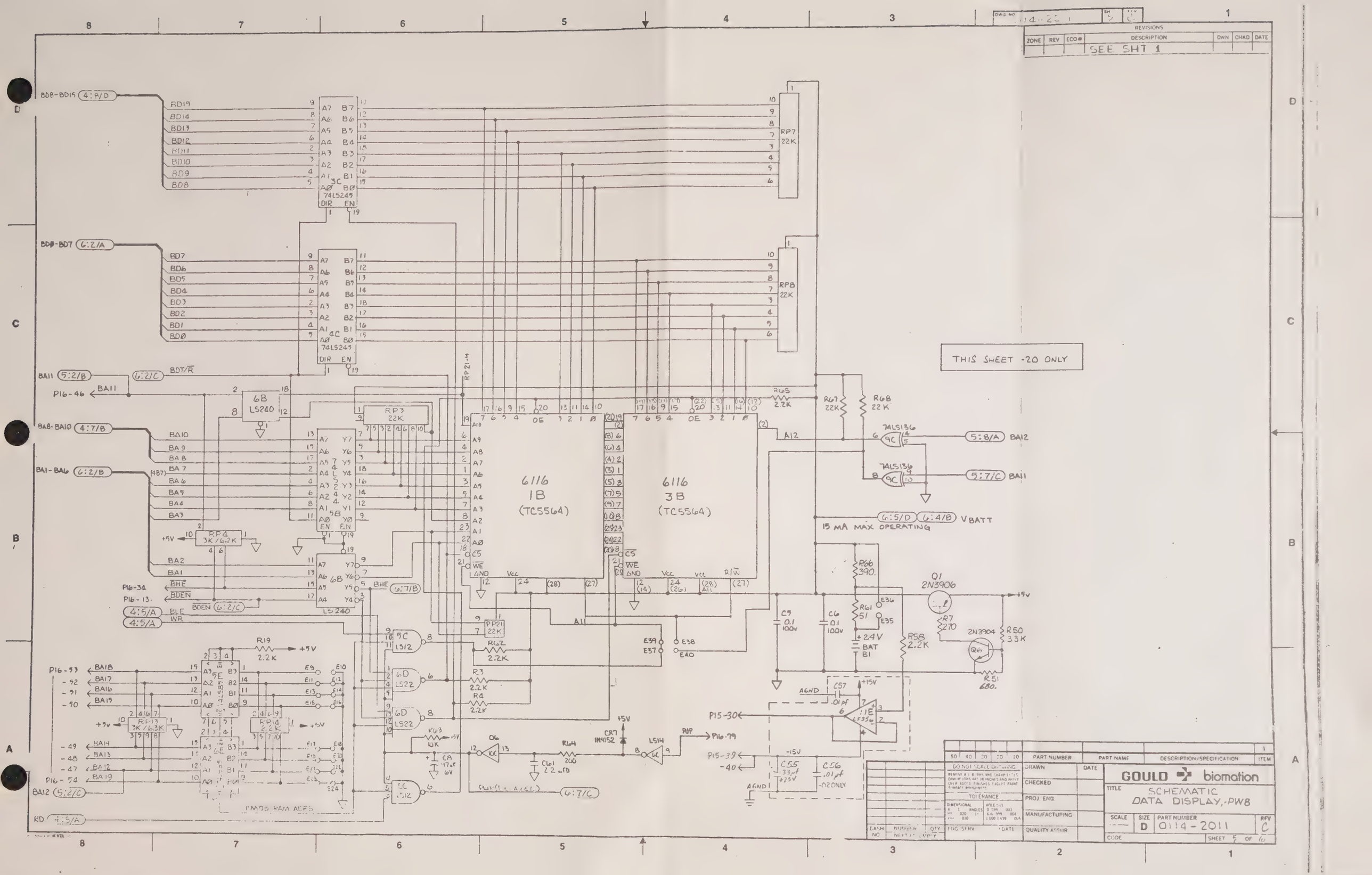
SCALE | SIZE D | PART NUMBER [illegible] | REV C

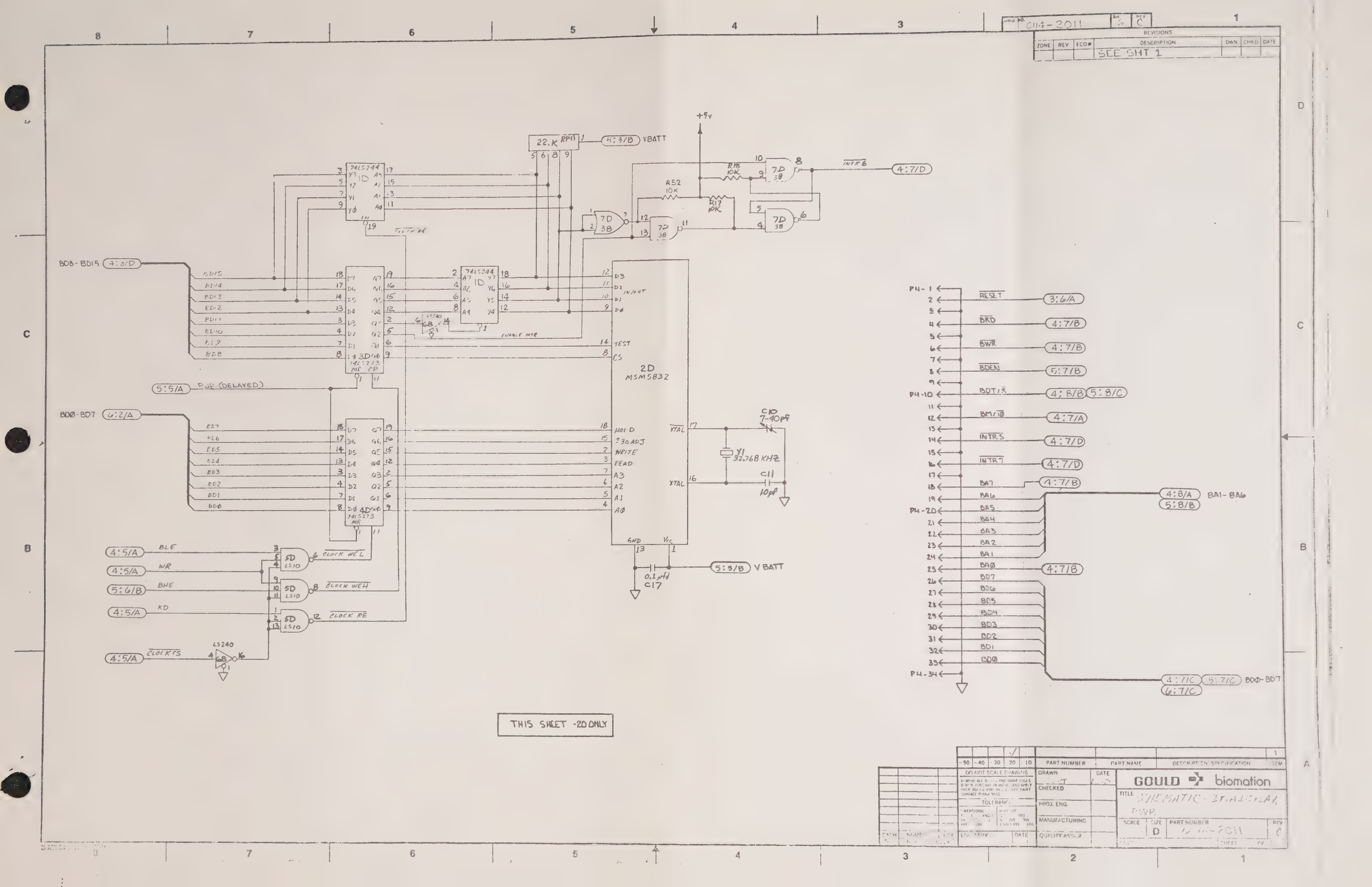
CODE | SHEET [illegible] OF [illegible]

BISHOP GRAPHICS/VARGUPRESS REORDER NO A4475



0114-2011
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
2E 8259A
4E 74LS240
RP12
RP18 3K/6.2K
RP19 3K/6.2K
RP16 3K/6.2K
RP10 3K/6.2K
RP15 2.2K
RP2 2.2K
74LS244 9E
10E 74LS245
8D LS20
7E 74LS85
8E 74LS138
14E 74LS156
9D LS10
S1 OPTIONS DIP-SWITCH
17E LS74
16E 74LS161
15E 74LS161
13E 74LS244
74LS273 12E
RP20 2.2K
BEEPER
R56 VOLUME
R57 39Ω, 1/2W
R54 2.2K
R55 2.2K
R60 2.2K
R53 2.2K
-20 ONLY
KEYBOARD INTERFACE
LED OUTPUTS
LO = LIGHTED
HI = OFF
P16-63
P16-64
P16-32
P16-25
P16-24
P16-14
P16-45
P16-42
P16-10
P16-8
P16-12
P16-11
P16-41
P16-35
BD8-BD15
BD0-BD7
BA8-BA10
BA7
BM/IO
BA1-BA6
BDT/R
INTR0
FPRE
RESET
50 HZTC
1/2 MHZ
P15-16 -15 -14 -13 -12 -11 -10 -9
P15 -24 -23 -22 -21 -20 -19 -18 -17
P15-8
P15-1
GOULD biomation
TITLE SCHEMATIC
DATA DISPLAY PWB
SCALE SIZE D PART NUMBER 0114-2011
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DO NOT SCALE DRAWING
TOLERANCE


DWG NO 0114-2011
SH 5
REV C
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
BD8-BD15 (4:A/D)
BD0-BD7 (6:2/A)
BA11 (5:2/B)
BA8-BA10 (4:7/B)
BA1-BA6 (6:2/B)
P16-46
BDT/R
(6:2/C)
74LS245
3C
4C
5B
6B
6E
LS240
LS245
6B LS240
RP7 22K
RP8 22K
RP21-4
RP3 22K
RP4 3K/6.2K
RP13 3K/6.3K
RP14 2.2K
RP21 22K
R19 2.2K
R62 2.2K
R3 2.2K
R4 2.2K
R63 10K
C4 47pf 6V
C61 2.2 uFD
R64 200
CR7 1N4152
LS14
P16-79
P15-30
P15-39
-40
P16-34
P16-13
BHE
BDEN
(6:7/B)
(6:2/C)
4:5/A BLE
4:5/A WR
P16-53
-52
-51
-50
-49
-48
-47
P16-54
BA18
BA17
BA16
BA15
BA14
BA13
BA12
BA19
(5:2/C)
KD (4:5/A)
CMOS RAM ADRS
5C LS12
6D LS22
6D LS22
5C LS12
6C
6116 1B (TC5564)
6116 3B (TC5564)
OE
CS
WE
GND
Vcc
R/W
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
A12
R65 2.2K
R67 22K
R68 22K
74LS136 9C
(5:8/A) BA12
(5:7/C) BA11
(6:5/D) (6:4/B) VBATT
15 MA MAX OPERATING
R66 390.
R61 51
E36
E35
+2.4V
BAT B1
C9 0.1 100V
C6 0.1 100V
R58 2.2K
Q1 2N3906
R7 270
2N3904 Q6
R50 3.3K
R51 680.
+5V
AGND
C57 .01pf
+15V
1E LF356
-15V
C55 33pf +25V
C56 .01pf -02 ONLY
THIS SHEET -20 ONLY
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC
DATA DISPLAY, PW8
SCALE
SIZE D
PART NUMBER 0114-2011
REV C
CODE
SHEET 5 OF 6



C114-2011
SEE SHT 1
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
+5V
22.K RP11
5:3/B VBATT
74LS244 1D
74LS273 3D
74LS273 4D
74LS244 1D
R52 10K
R18 10K
R17 10K
7D 38
INTR6
4:7/D
BD8-BD15 4:0/D
BD0-BD7 6:2/A
5:5/A PUP (DELAYED)
2D MSM5832
TEST
CS
HOLD
±30 ADJ
WRITE
READ
A3
A2
A1
A0
XTAL
GND
Vcc
C10 7-40pf
Y1 32.768 KHZ
C11 10pf
0.1 µfd C17
5:3/B V BATT
4:5/A BLE
4:5/A WR
5:6/B BHE
4:5/A KD
4:5/A CLOCK CS
LS240
5D LS10
CLOCK WEL
CLOCK WEH
CLOCK RE
P4-1 RESET 3:6/A
BRD 4:7/B
BWR 4:7/B
BDEN 5:7/B
P4-10 BDT/R 4:8/B 5:8/C
BM/IO 4:7/A
INTR5 4:7/D
INTR7 4:7/D
BA7 4:7/B
BA6
BA5
BA4
BA3
BA2
BA1
BA0 4:7/B
P4-20
4:8/A BA1-BA6
5:8/B
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
P4-34
4:7/C 5:7/C BD0-BD7
6:7/C
THIS SHEET -20 ONLY
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
GOULD biomation
TITLE SCHEMATIC - DIAGONAL PWR
SCALE
SIZE D
PART NUMBER
REV C

MPU BOARD
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0186

A. MICROPROCESSOR- (SHEET 1) - THE OPERATION OF THE K101-D IS CONTROLLED BY AN 8086 MICROPROCESSOR RUNNING AT A 4 MHZ CLOCK RATE IN THE MINIMUM MODE CONFIGURATION.

1. 16 BIT MICROPROCESSOR (LOCATION 10L), AND THE K101-D HAS BEEN DESIGNED FOR EITHER BYTE OR WORD TRANSFERS.
2. A0 AND BHE (BYTE HI ENABLE) ARE USED FOR BYTE OR WORD TRANSFERS.
3. A0 IS ASSERTED WHEN A LOW (EVEN) BYTE IS ACCESSED.
4. BHE IS ASSERTED WHEN A HIGH (ODD) BYTE IS ACCESSED.
5. FOR WORD OPERATION BOTH A0 AND BHE ARE USED.

B. ADDRESS REGISTERS AND DATA TRANSCEIVERS - THE 8086 USES A MULTIPLEXED BUS FOR ADDRESS AND DATA TRANSFERS. THE MICROPROCESSOR BOARD DEMULTIPLEXES THE 8086 BUS INTO TWO BUSES.

1. ONE BUS CONTROLS ALL COMMUNICATION TO THE RAM AND THE ROM WHICH IS CONTAINED ON THE BOARD.
2. THE OTHER BUS INTERFACES WITH THE OTHER BOARDS IN THE K101-D.
3. EACH BUS CONTAINS SIXTEEN TRANSCEIVERS FOR THE DATA LINES, D0 THROUGH D15 (74LS245's).
4. EACH BUS ALSO CONTAINS A REGISTER WHICH HANDLES THE 21 ADDRESS LINES, A0 THROUGH A19 AND BHE.
5. THE 8086 LOADS AN ADDRESS INTO THE REGISTER USING ADDRESS LATCH ENABLE (ALE) AND THEN TRANSMITS (WR) THE DATA, TO OR RECEIVES (RD) THE DATA FROM, THE ADDRESS IN THE REGISTER.

C. MEMORY - (SHEET 2, RAM) (SHEET 5, ROM) - THE 8086 MEMORY SPACE IS ORGANIZED INTO SIXTEEN SEGMENTS OF 64 K BYTES EACH.

THE K101-D IS CONFIGURED AS A MINIMUM SYSTEM USING ONLY FOUR SEGMENTS.

1. SEGMENTS E AND F (HEX) ARE THE 128 K OF ROM WHICH CONTAINS THE OPERATING SOFTWARE.
2. SEGMENTS 0 AND 1 (HEX) CONTAINS THE 128 K BYTES OF DYNAMIC RAM.
3. THE ROM SEGMENT (SHEET 5) USES SIXTEEN 8K X 8 MEMORIES ARRANGED INTO EIGHT SECTIONS OF 8K WORDS EACH.
4. THE RAM (SHEET 2) IS MADE UP OF SIXTEEN 64K X 1 DYNAMIC MEMORIES PROVIDING 64K WORDS (128K BYTES).

D. MEMORY CONTROLLER - (SHEET 3) (SHEET 6, TIMING) THE DYNAMIC RAM IN THE K101-D IS ORGANIZED AS A TWO PORT MEMORY.

THE 8086 READS AND WRITES THROUGH ONE PORT, AND THE CRT DATA IS READ OUT THROUGH THE OTHER.

1. (SHEET 3) - THE MEMORY TIMING AND THE CLOCK FOR THE 8086 ARE DERIVED FROM A 24 MHZ OSCILLATOR (Y1).
2. THIS ALSO PROVIDES AN 8 MHZ CLOCK TO THE CRT.
3. (SHEET 6) - TIMING RELATIONSHIPS FOR THE VARIOUS MEMORY SIGNALS IS SHOWN ON THIS PAGE.
4. THE MEMORY CYCLE TIME IS 390 NS, 9 CLOCKS AT 24 MHZ (9 X 43.3 NS = 389.9 NS).
5. THE CRT PORT OF THE MEMORY REQUESTS A WORD FROM MEMORY EVERY 2 US. THE WORD IS WRITTEN INTO A BUFFER REGISTER AND THEN SHIFTED OUT TO THE DATA DISPLAY BOARD.
6. THE REST OF THE TIME (2000 NS - 390 NS = 1610 NS) IS AVAILABLE TO THE 8086 FOR ITS NEEDS.

7. IF THE 8086 REQUESTS A MEMORY CYCLE DURING THE CRT CYCLE, THE CONTROLLER USES THE READY LINE ON THE MICROPROCESSOR TO PRODUCE WAIT STATES UNTIL THE CRT CYCLE IS FINISHED AND THE MEMORY CAN COMPLETE THE REQUESTED 8086 CYCLE.

8. THE CRT READ CYCLE OF ONE WORD EVERY 2 us ALSO PROVIDES SEQUENTIAL OPERATION REQUIRED FOR REFRESHING THE RAM.

E. <u>I/O DECODING</u> - (SHEET 4) - THE MPU ADDRESSES THE OTHER BOARDS IN THE SYSTEM AS I/O.

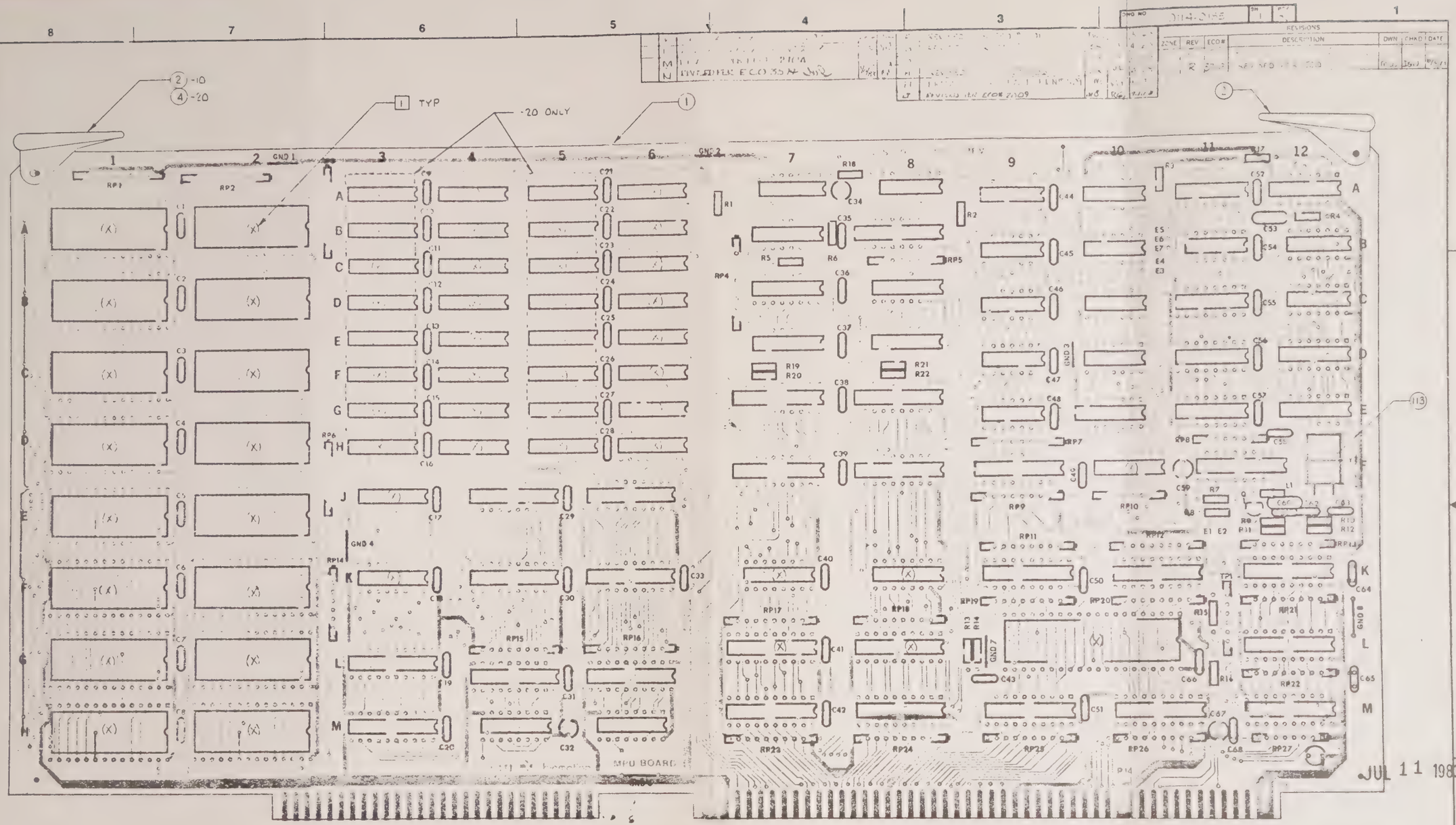
1. WHEN I/O IS ADDRESSED, M/$\overline{IO}$ GOES LOW——DISABLING MAP PROM 10F CAUSING IT'S OUTPUTS TO BE HIGH.

2. $\overline{DEN}$ BECOMES ACTIVE.

3. $\overline{SA\ EN}$ IS NORMALLY HIGH.

4. THE ABOVE CONDITIONS CAUSE "$\overline{ENABLE\ OFF\ BOARD\ DATA}$" TO GO LOW PLACING DATA ON THE BUS.

5. M/$\overline{IO}$ GOES LOW AND ENABLES ADDRESS COMPARATORS ON OTHER BOARDS.



COMPONENT SIDE

NOTES:
1. THIS SYMBOL (X) INDICATES WHERE I.C. SOCKETS ARE REQUIRED (FOR REF ONLY)

JUL 11 1983

ECO PENDING # 3899p

DO NOT SCALE DRAWING	DRAWN	DATE	GOULD biomation
TOLERANCE	CHECKED		TITLE ASSEMBLY, K101, K500 MPU BD.
	PROJ. ENG.		
	MANUFACTURING		SCALE 2:1 · SIZE D · PART NUMBER 0114-0185 · REV R
ENG SERV. · DATE	QUALITY ASSUR		CODE · SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				1	1	1	1	1	—	1	1	0114-0187	P.C. BOARD				
				2	2	2	1	1	—	1	2	7000-0120	EJECTOR				
				3													
				4	—	—	1	1	—	1	—	0112-0228-07	EJECTOR, STAMPED	A7			
				5													
				6													
				7	—	—	—	—	—	—	1	0950-0191	I.C.	10F		ROM, ADD. MAP	
-10: K500				8	—	—	—	—	—	—	1	0950-0193		3J		ROM, CHIP SEL	
-20: K101				9	—	—	—	—	—	—	1	0950-0192		3K		ROM, CHIP SEL	
-30: K102				10													
-40: K101 WITH STORAGE				11	—	—	1	1	—	1	—	0114-0066		10F		ROM, ADD. MAP	
-50: K102 WITH STORAGE				12	—	—	1	1	—	1	—	0114-0067		3J		ROM, CHIP SEL	
				13	—	—	1	1	—	1	—	0114-0069		3K		ROM, CHIP SEL	
				14													
				15	1	1	—	—	—	1	1	1800-0321	I.C.	10L		8086	
				16	1	1	—	—	—	—	—	0117-0017-01	I.C., ROM ADD MAP	10F			
				17	1	1	—	—	—	—	—	0117-0018-01	I.C., ROM CHIP SEL	3J			
				18	1	1	—	—	—	—	—	0117-0019-01	I.C., ROM CHIP SEL	3K			

JUL 11 1983

ASSEMBLY TIME

COMPONENT LEAD SPACING

ECO PENDING # 3899 P

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
B	PROTOTYPE UPDATES	9-30-80	CURT		
C					
D	RELEASE TO PILOT RUN, ERN# 086	11-8-80	N.G.		
E	REVISED PER ECO #1484	3-3-81	J.C.	RD	
F	REVISED PER ECO # 1601	3-26-81	J.C.	RD	
G	REVISED PER ECO # 1662	4-20-81	SR	JL	
H	REVISED PER ECO # 1706	4-22-81	SR	JL	

DASH NO.	NUMBER	QTY
-50	0114-0002	1
-40	0114-0002	1
-30	0114-0073	1
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

		DATE
DRAWN	[illegible]	12-19-80
CHECKED	RG	5/29/81
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
ASSEMBLY, MPU PWB

MODEL K101, K102 K500

biomation

B | 0114-0185 | REV R

CODE | SHEET 1 OF 9

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				19													
				20	—	—	—	—	—	—	1	0950-0150-01	I.C.	2H		READ ONLY MEM	
				21	—	—	—	—	—	—	1	-02		1H			
				22	—	—	—	—	—	—	1	-03		2G			
				23	—	—	—	—	—	—	1	-04		1G			
				24	—	—	—	—	—	—	1	-05		2F			
				25	—	—	—	—	—	—	1	-06		1F			
				26	—	—	—	—	—	—	1	-07		2E			
-10: K500				27	—	—	—	—	—	—	1	-08		1E			
-20: K101				28	—	—	—	—	—	—	1	-09		2D			
-30: K102				29	—	—	—	—	—	—	1	-10		1D			
-40: K101 WITH STORAGE				30	—	—	—	—	—	—	1	-11		2C			
-50: K102 WITH STORAGE				31	—	—	—	—	—	—	1	-12		1C			
				32	—	—	—	—	—	—	1	-13		2B			
				33	—	—	—	—	—	—	1	0950-0150-14	I.C.	1B		READ ONLY MEM	
				34	—	—	—	—	—	—	1	0950-0150-15	I.C.	2A			
				35	—	—	—	—	—	—	1	0950-0150-16	I.C.	1A		READ ONLY MEM.	
				36													

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	PROD REL PER EFN # 0129	5-28-81		RG	
J	REVISED PER ECO # 2009	9-14-81	MG	RG	
K	REVISED PER ECO NO 2297	2-2-82		TJ	
L	REVISED PER ECO 2367	2-2-82		TJ	
M	REVISED PER ECO 2704	10-15-82			
N	REVISED PER ECO # 3574	3/17/83			
P	REVISED PER ECO # 3529	5/16/83	MW	DW	5/27/83

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY
MPU PWB

MODEL

biomation

B | 0114-0185 | REV R

CODE | SHEET 2 OF 9

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				37													
				38	—	—	—	1	—	1	—	0114-2020-01	I.C.	2H		CODE ROM K101	
				39	—	—	—	1	—	1	—	-02		1H			
				40	—	—	—	1	—	1	—	-03		2G			
				41	—	—	—	1	—	1	—	-04		1G			
				42	—	—	—	1	—	1	—	-05		2F			
				43	—	—	—	1	—	1	—	-06		1F			
				44	—	—	—	1	—	1	—	-07		2E			
-20: K101				45	—	—	—	1	—	1	—	-08		1E			
-40: K101 WITH STORAGE				46	—	—	—	1	—	1	—	-09		2D			
-50: K102 WITH STORAGE				47	—	—	—	1	—	1	—	-10		1D			
				48	—	—	—	1	—	1	—	-11		2C			
				49	—	—	—	1	—	1	—	-12		1C			
				50	—	—	—	1	—	1	—	-13		2B			
				51	—	—	—	1	—	1	—	-14		1B			
				52	—	—	—	1	—	1	—	-15		2A			
				53	—	—	—	1	—	1	—	0114-2020-16	I. C.	1A		CODE ROM K101	
				54													

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	R	REVISED PER ECO 3763	6/1/83	MW	DGW	6/4/83

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

biomation

B	0114-0185	REV R
MODEL	CODE	SHEET 3 OF 9

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				55			32	32	—	—	—	1800-0353	IC	3A-3H, 5A-5H 4A-4H, 6A-6H		4164, 64K RAM	
				56			37	37	37	37	—	6100-0120	SOCKET	X3J, X3K, X7K, X8K X10F, X3A-X3H,		16 PIN DIP, LP	
				57										X4A-X4H, X5A-X5H, X6A-X6H			
				58	1	1	1	1	1	1	1	1400-0019	TRANSISTOR	Q1	2N3906		
				59													
				60	3	3	3	3	3	3	3	1800-0031	IC	9B, 10B, 12B	74S00		
				61	1	1	1	1	1	1	1	1800-0038		9C	74S20		
				62	8	8	8	8	8	8	8	1800-0039		10E, 11A, 11C, 11D, 11E 12A, 12D, 12E	74S112		
-10: K500				63	4	4	4	4	4	4	4	1800-0060		7A, 8A, 9D, 12C	74S10		
-20: K101				64	1	1	1	1	1	1	1	1800-0092		10A	74S04		
-30: K102				65	1	1	1	1	1	1	1	1800-0107		9E	74LS04		
-40: K101 WITH STORAGE				66	4	4	4	4	4	4	4	1800-0125		7C, 7D, 8C, 8D	74LS161		
-50: K102 WITH STORAGE				67	1	1	1	1	1	1	1	1800-0133		10C	74S11		
				68	1	1	1	1	1	1	1	1800-0136		10D	74S51		
				69	1	1	1	1	1	1	1	1800-0208		7B	74S161		
				70	9	9	9	9	9	9	9	1800-0240		3L, 3M, 4J, 6J, 7E 7F, 8E, 8F, 9F	74LS244		
				71	2	2	2	2	2	2	2	1800-0243		9A, 11B	74S08		
				72	3	3	3	3	3	3	3	1800-0261	IC	8B, 11F, 11M	74S240		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY - MPU PWB

MODEL

biomation

B	0114-0185	REV R
CODE	SHEET 4 OF 9	

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				73	2	2	2	2	2	2	2	1800-0268	IC	7M, 8M	74LS245		
				74	10	10	10	10	10	10	10	1800-0298	IC	4K,4L,6K,6L,9K,9M 10K,10M,11K,11L	74LS373		
				75	—	—	—	—	—	—	16	1800-0320	IC	4A-4H, 6A-6H		2118 RAM	
				76	2	2	2	2	2	2	2	1800-0335	IC	4M, 6M	74LS166		
				77	32	16	—	—	16	16	—	1800-0353	IC	4A-4H, 6A-6H		64K RAM	
				78	1	1	1	1	1	1	1	2100-0009	INDUCTOR	L1		1.5 μH	
				79													
				80	1	1	1	1	1	1	1	3000-1000	RESISTOR	R11		100Ω, 1/4W, 5%	
-10: K500				81	1	1	1	1	1	1	1	3000-1300		R9		130Ω	
-20: K101				82	2	2	2	2	2	2	2	3000-1601		R6,10		1.6K	
-30: K102				83	1	1	1	1	1	1	1	3000-2006		R4		20Ω	
-40: K101 WITH STORAGE				84	3	3	3	3	3	3	3	3000-2200		R7, 19, 21		220Ω	
-50: K102 WITH STORAGE				85	7	7	7	7	7	7	7	3000-2201		R1-3,5,15,17,18		2.2K	
				86	1	1	1	1	1	1	1	3000-2700		R13		270Ω	
				87	3	3	3	3	3	3	3	3000-3300		R8,20,22		330Ω	
				88	1	1	1	1	1	1	1	3000-3301		R12		3.3K	
				89	1	1	1	1	1	1	1	3000-5100		R16		510Ω	
				90	1	1	1	1	1	1	1	3000-9106	RESISTOR	R14		91Ω, 1/4W, 5%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	Gena M. Hilli	12-19-80
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

ASSEMBLY – MPU PWB

MODEL

biomation

B	0114-0185	REV R
CODE	SHEET 5 OF 9	

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				91	5	5	5	5	5	5	5	3700-0065	RESISTOR PAK	RP3,4,11-13		220/330 (10 PIN SIP)	
				92	13	13	13	13	13	13	13	3700-0049	↓	RP1,2,7,9,15-18, 22-26		3K/6.[illegible]K (10 PIN SIP)	
				93	6	6	6	6	6	6	6	3700-0057	↓	RP5,6,8,10,14, 27		2.2K [illegible] PIN SIP)	
				94	3	3	3	3	3	3	3	3700-0066	RESISTOR PAK	RP19-21		10K (10 PIN SIP)	
				95													
				96	1	1	1	1	1	1	1	4000-0040	CAPACITOR	C43		470pf	
				97	61	61	61	61	61	61	61	4000-0044	CAPACITOR	C1-31,33,35-42,54-58,61-66,68, 44-52		.01µf, 100V, ±20%	
				98													
-10: K500				99	1	1	1	1	1	1	1	4100-0019	CAPACITOR	C53		50pf	
-20: K101				100	1	1	1	1	1	1	1	4100-0029	CAPACITOR	C60		30pf	
-30: K102				101													
-40: K101 WITH STORAGE				102	5	5	5	5	5	5	5	4400-0043	CAPACITOR	C32,34,59,67,69		47µf, 6V, ±10%	
-50: K102 WITH STORAGE				103													
				104	1	1	1	1	1	1	1	5100-0016	CRYSTAL	Y1		24 MHZ	
				105													
				106	1	1	1	1	1	1	1	6000-0190	HEADER	TP1		8 PIN CONN.	
				107													
				108	37	37	—	—	21	21	21	6100-0120	SOCKET	X3J, X3K, X7K, X8K, X10F, X4A-X4H, X6A-X6H,		16 PIN	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	Jena M. Grilli	12-19-80
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

ASSEMBLY - MPU PWB

MODEL

biomation

B	0114-0185	REV R
CODE		SHEET 6 OF 9

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				109	2	2	2	2	2	2	2	6100-0121	SOCKET	X7L, X8L		20 PIN	
				110	1	1	1	1	1	1	1	6100-0123	SOCKET	X10L		40 PIN	
				111	16	16	16	16	16	16	16	6100-0151	SOCKET	X1A-X1H X2A-X2H		28 PIN	
				112													
				113	A/R	A/R	A/R	A/R	A/R	A/R	A/R	7100-0017	WIRE	@Y1 (CRYSTAL STRAP)		#22 AWG	
				114													
				115	8	8	8	8	8	8	8	9000-0054	WIRE, FORMED	GND1-GND8		16 PIN	
				116													
				117													
-10: K500				118													
-20: K101				119													
-30: K102				120													
-40: K101 WITH STORAGE				121													
-50: K102 WITH STORAGE				122													
				123													
				124													
				125													
				126													

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN Gina M. Grilli	DATE 12-19-80	
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL

ASSEMBLY – MPU PWB

MODEL

biomation

B	0114-0185	REV R.
CODE	SHEET 7 OF 9	

COMMENTS		TOTAL COST	UNIT COST	ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
				127													
				128	—	—	1	—	1	—	—	0114-2021-01	IC	2H		CODE ROM K102	
				129	—	—	1	—	1	—	—	-02	↑	1H		"	
				130	—	—	1	—	1	—	—	-03		2G		"	
				131	—	—	1	—	1	—	—	-04		1G		"	
-10; K500				132	—	—	1	—	1	—	—	-05		2F		"	
-20; K101				133	—	—	1	—	1	—	—	-06		1F		"	
-30: K102				134	—	—	1	—	1	—	—	-07		2E		"	
-40; K101 WITH STORAGE				135	—	—	1	—	1	—	—	-08		1E		"	
-50; K102 WITH STORAGE				136	—	—	1	—	1	—	—	-09		2D		"	
				137	—	—	1	—	1	—	—	-10		1D		"	
				138	—	—	1	—	1	—	—	-11		2C		"	
				139	—	—	1	—	1	—	—	-12		1C		"	
				140	—	—	1	—	1	—	—	-13		2B		"	
				141	—	—	1	—	1	—	—	-14		1B		"	
				142	—	—	1	—	1	—	—	-15	↓	2A		1	
				143	—	—	1	—	1	—	—	0114-2021-16	IC	1A		CODE ROM K102	
				144													

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

		DATE
DRAWN		
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

ASSEMBLY
MPU PWB

MODEL

biomation

B | 0114-0185 | REV R

CODE | SHEET 8 OF 9

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
145													
146			1	1	—	—	—	—	—	0117-0020-01	CODE ROM K105	2H	
147			1	1	—	—	—	—	—	-02		1H	
148			1	1	—	—	—	—	—	-03		2G	
149			1	1	—	—	—	—	—	-04		1G	
150			1	1	—	—	—	—	—	-05		2F	
151			1	1	—	—	—	—	—	-06		1F	
152			1	1	—	—	—	—	—	-07		2E	
153			1	1	—	—	—	—	—	-08		1E	
154			1	1	—	—	—	—	—	-09		2D	
155			1	1	—	—	—	—	—	-10		1D	
156			1	1	—	—	—	—	—	-11		2C	
157			1	1	—	—	—	—	—	-12		1C	
158			1	1	—	—	—	—	—	-13		2B	
159			1	1	—	—	—	—	—	-14		1B	
160			1	1	—	—	—	—	—	-15		2A	
161			1	1	—	—	—	—	—	0117-0020-16	CODE ROM K105	1A	
162													
163													
164													
165													
166													
167													
168													
169													
170													
171													
172													
173													
174													

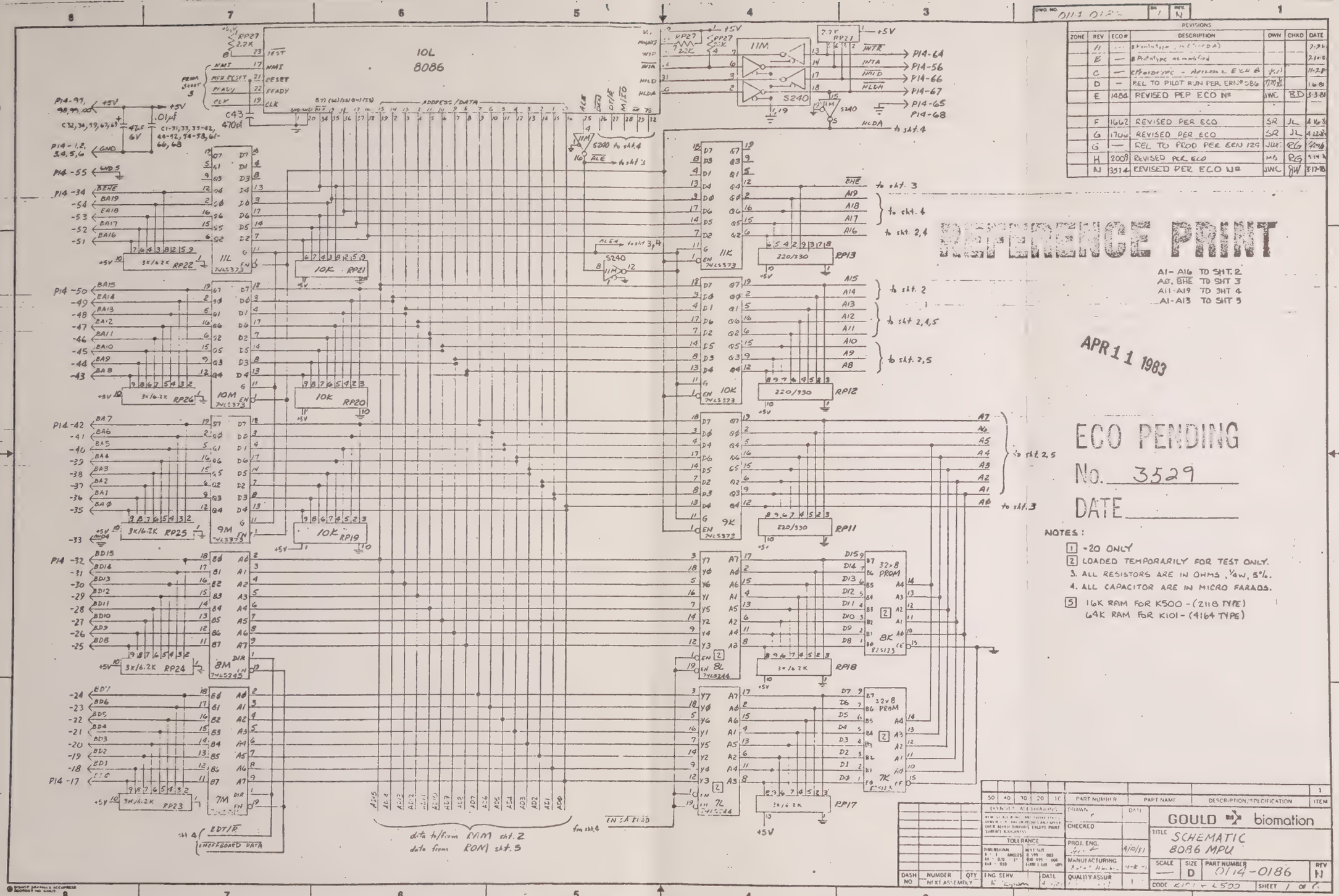
NOTES

LIST OF MATERIAL
ASSEMBLY,
MPU PWB

GOULD biomation

B 0114-0185 REV R

MODEL K101, K102, K500 SHEET 9 OF 9



DWG. NO.	SH.	REV.
0114-0186	1	N

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A1	---	Prototype (ECO DA)			7-31-81
	B	—	Prototype assembled			2-26-82
	C	—	Prototype - Add Rev. E ECN B	JK.11		11-2-82
	D	—	REL TO PILOT RUN PER ERN#0086	TMM		1-6-83
	E	1484	REVISED PER ECO Nº	JWC	BD	5-3-83
	F	1662	REVISED PER ECO	SR	JL	4-16-83
	G	1706	REVISED PER ECO	SR	JL	4-22-83
	G	—	REL TO PROD PER ERN 129	JWC	RG	5-26-83
	H	2009	REVISED PER ECO	MS	RG	9-14-83
	N	3514	REVISED PER ECO Nº	JWC	GW	3-17-88

REFERENCE PRINT

A1- A16 TO SHT. 2
A0, BHE TO SHT 3
A11-A19 TO SHT 4
A1-A13 TO SHT 5

APR 11 1983

ECO PENDING
No. 3529
DATE

NOTES:

1. -20 ONLY
2. LOADED TEMPORARILY FOR TEST ONLY.
3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
4. ALL CAPACITOR ARE IN MICRO FARADS.
5. 16K RAM FOR K500 - (2118 TYPE)
   64K RAM FOR K101 - (4164 TYPE)

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV.		DATE

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

TOLERANCE

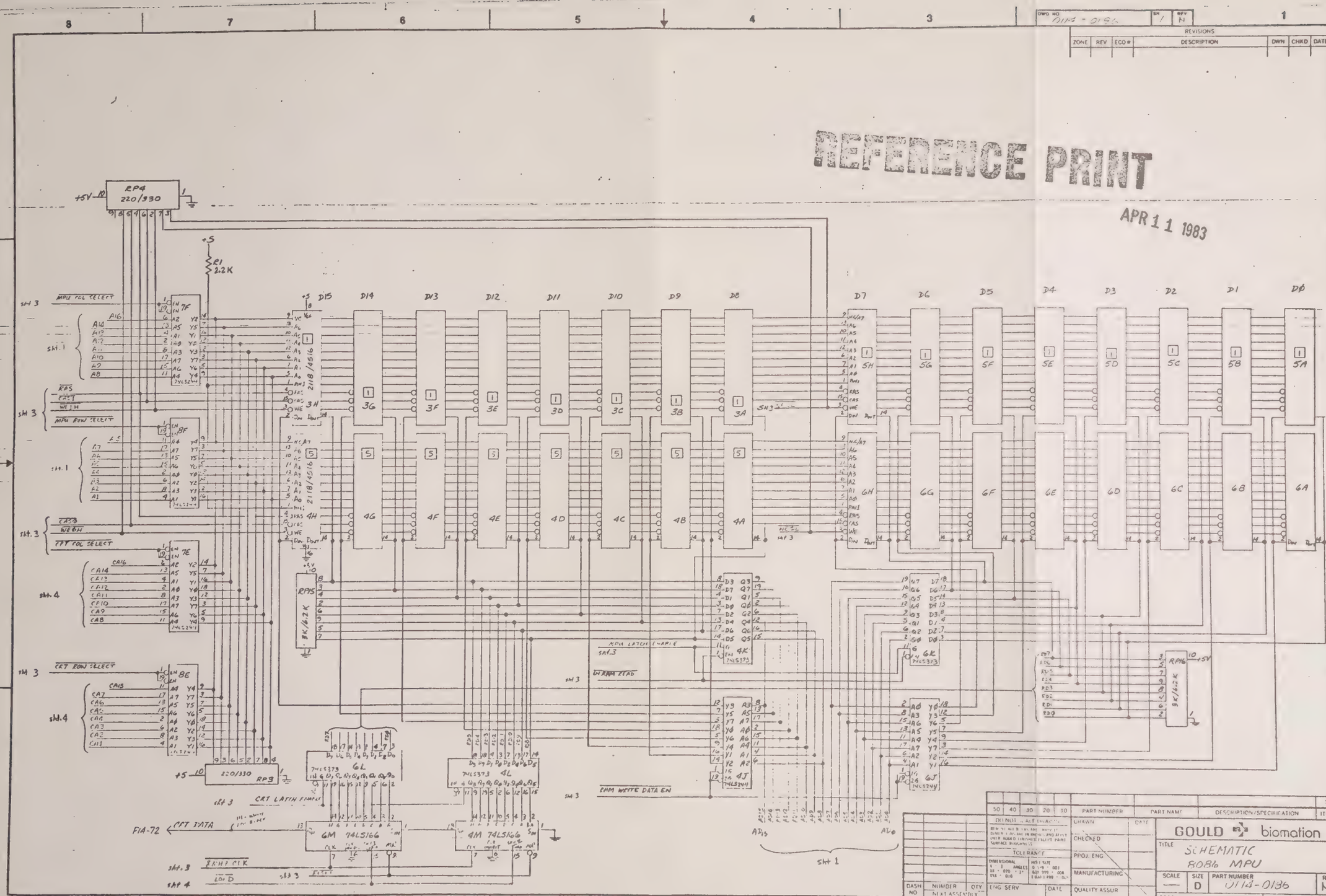
DRAWN		DATE
CHECKED		
PROJ. ENG.		4/10/81
MANUFACTURING		
QUALITY ASSUR		

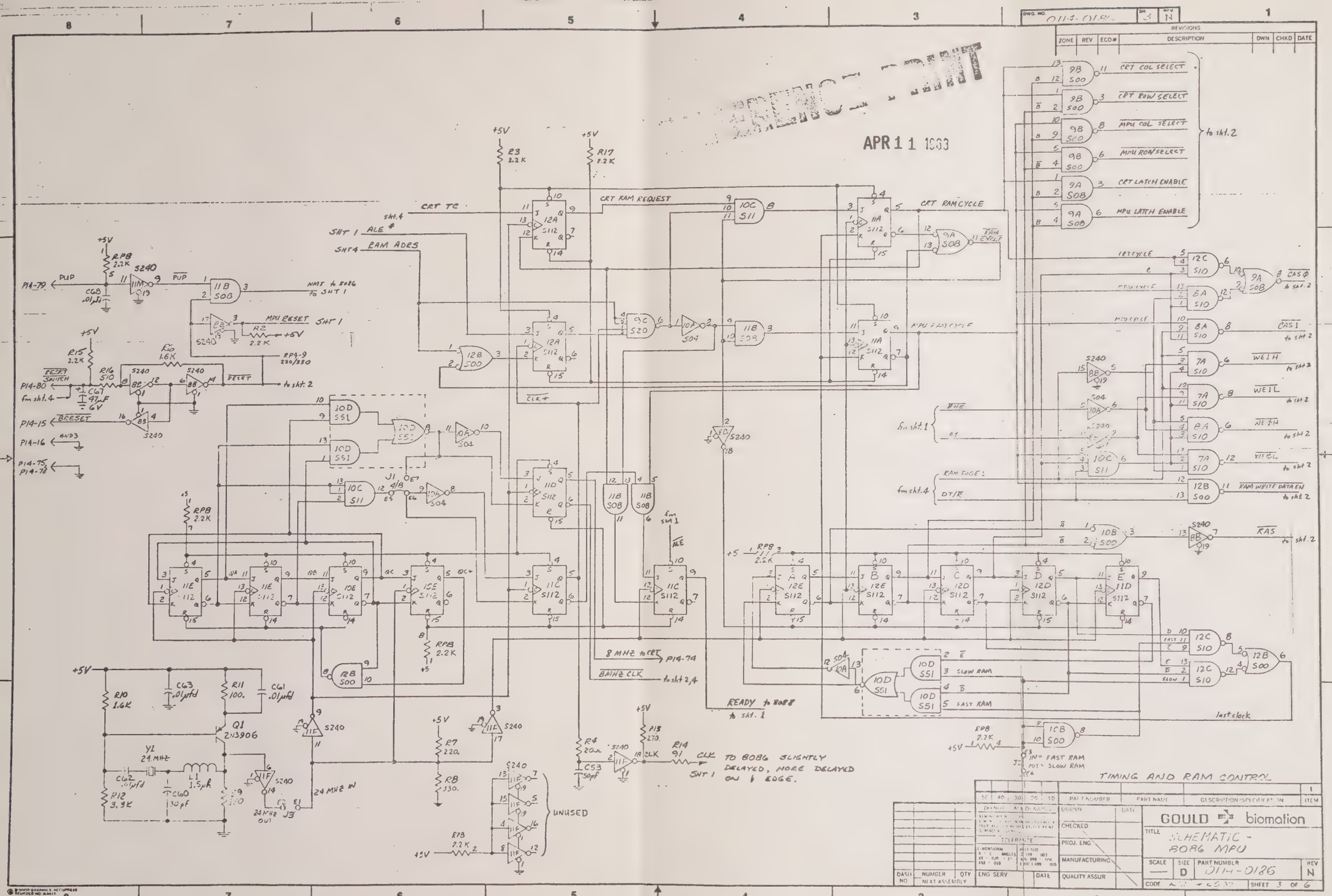
GOULD biomation

TITLE SCHEMATIC 8086 MPU

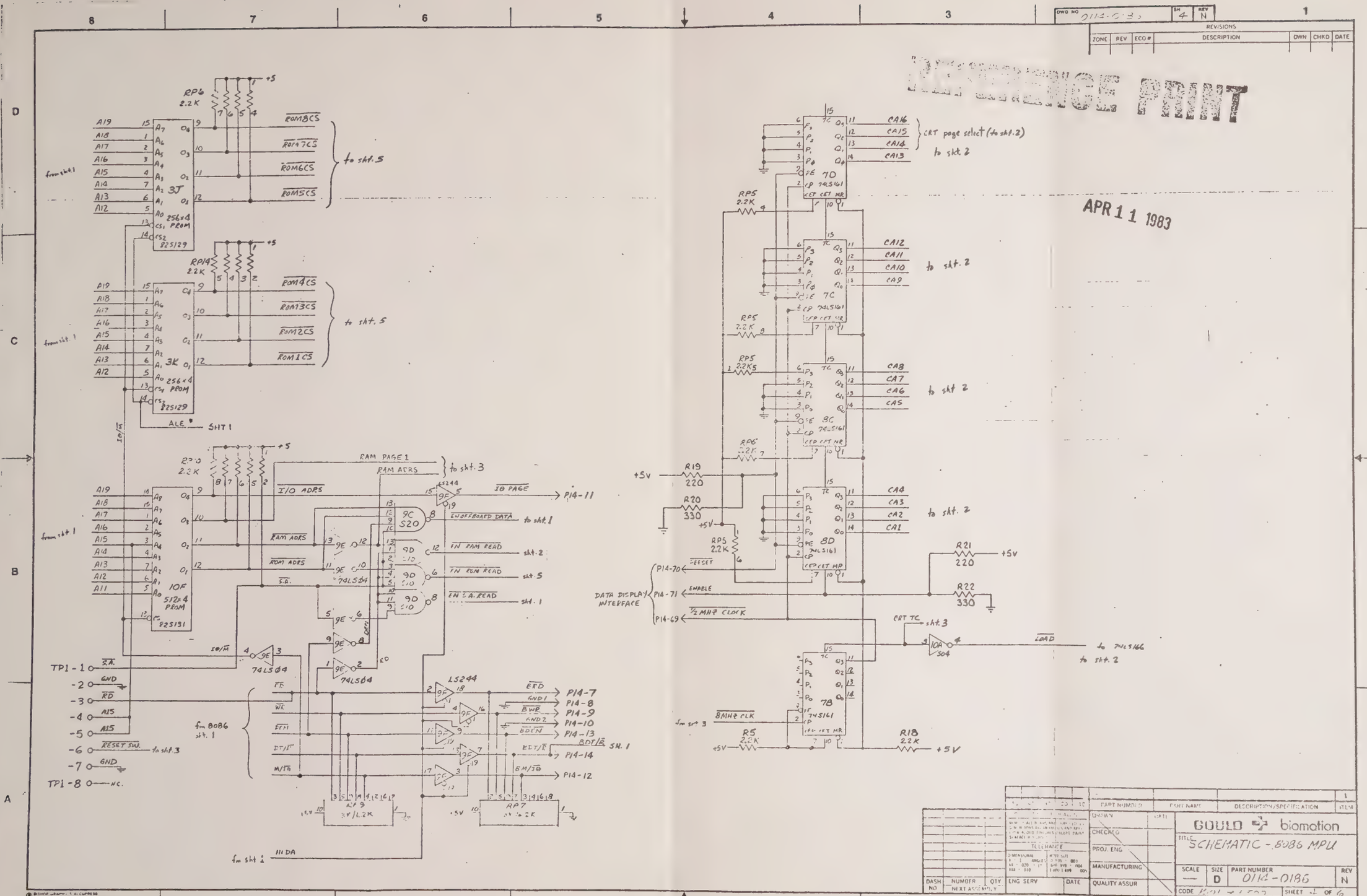
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0186	N

CODE K101 + K500 SHEET 1 OF 6

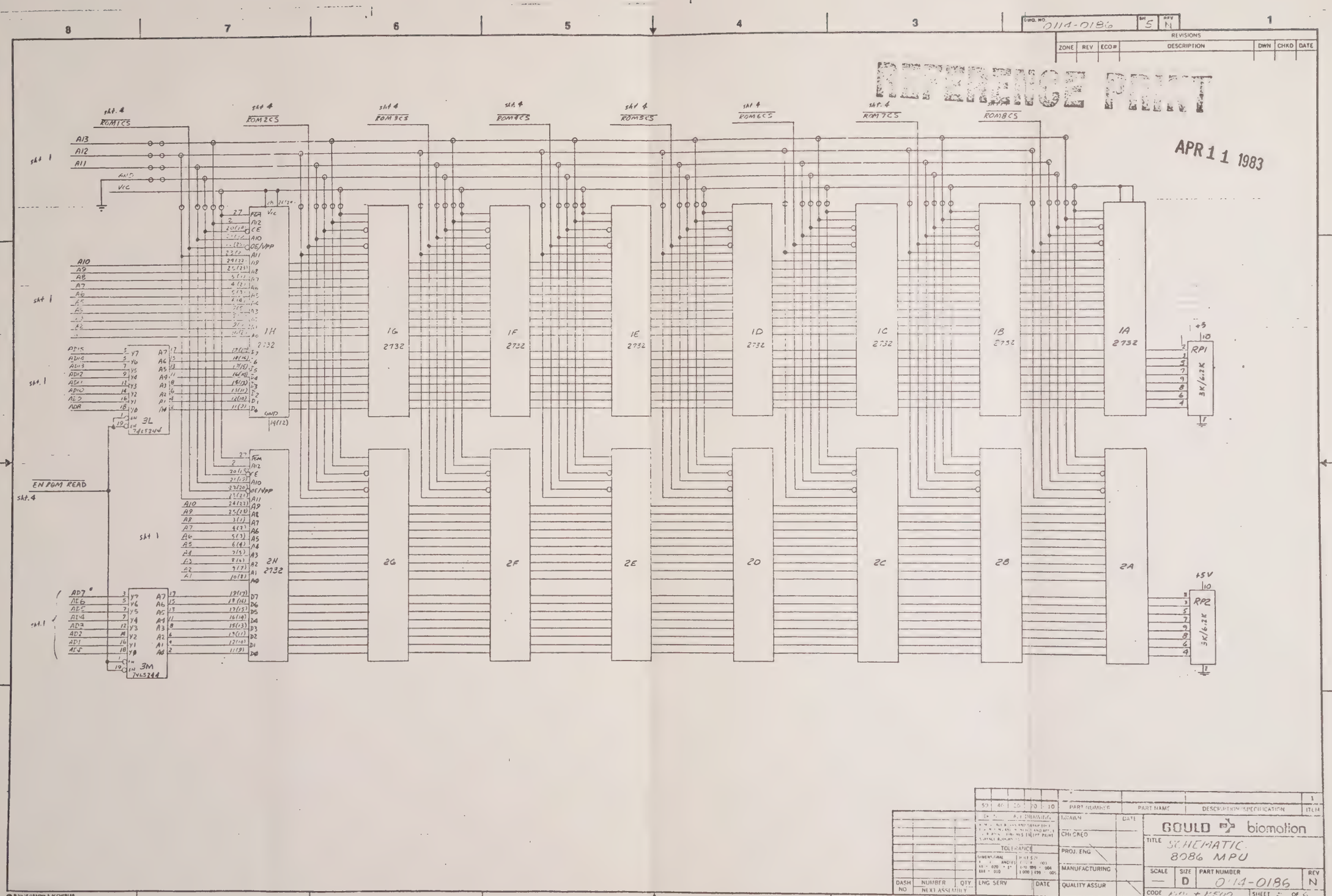

REFERENCE PRINT
APR 11 1983
DWG NO 0114-0186
SH 1
REV N
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
RP4 220/330
+5V
R1 2.2K
MPU COL SELECT
MPU ROW SELECT
CPT COL SELECT
CRT ROW SELECT
CRT LATCH ENABLE
CRT DATA
RAM WRITE DATA EN
MPU LATCH ENABLE
IN RAM READ
RP15 3K/6.2K
RP16 3K/6.2K
RP3 220/330
2118/4516
74LS244
74LS373
74LS166
FIA-72
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
GOULD biomation
TITLE SCHEMATIC 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV N
SHEET 2 OF 6
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY



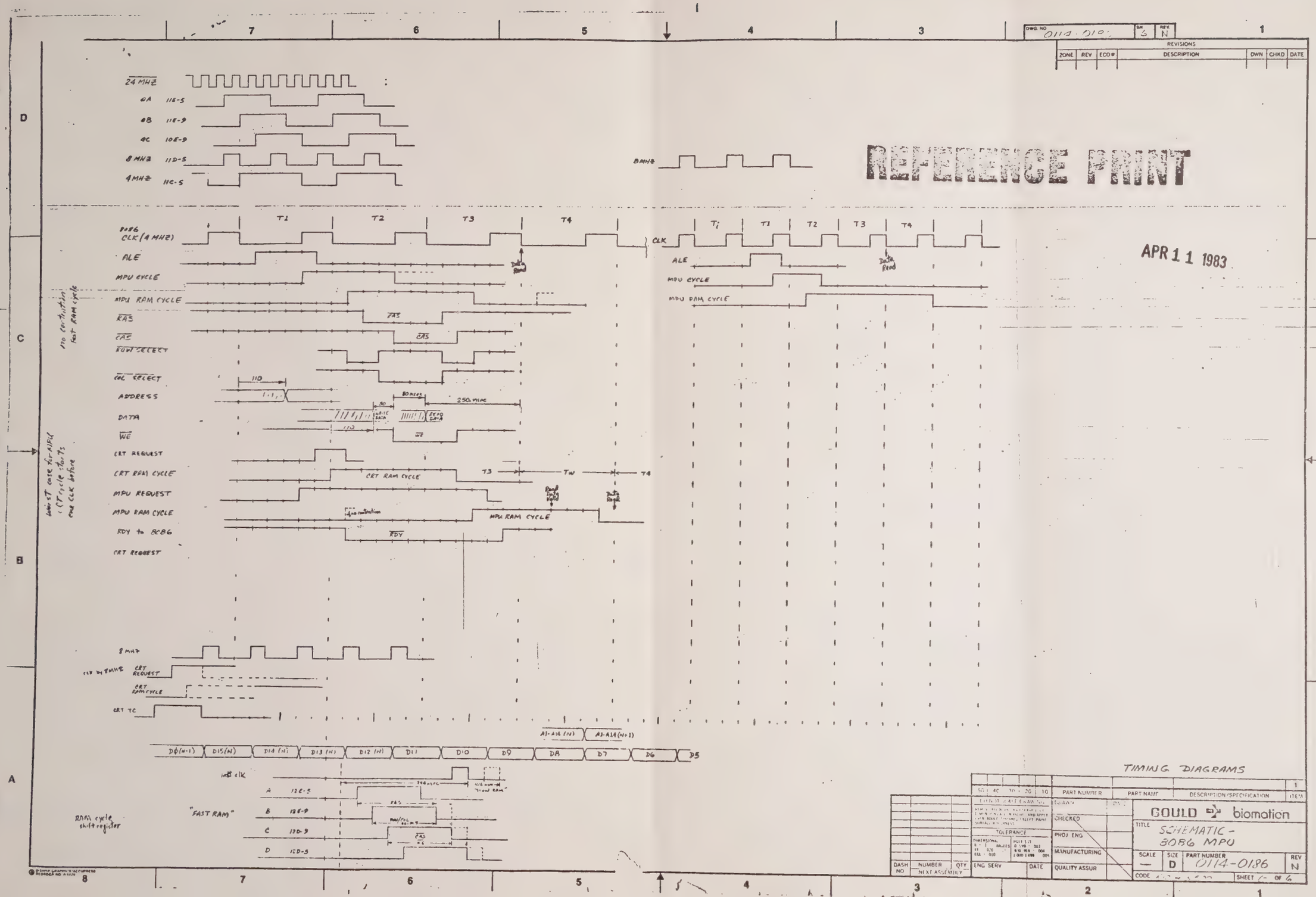
DWG. NO. 0114-0186
SH 3
REV N
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
APR 11 1983
CRT COL SELECT
CRT ROW SELECT
MPU COL SELECT
MPU ROW SELECT
CRT LATCH ENABLE
MPU LATCH ENABLE
to sht. 2
CRT RAM REQUEST
CRT RAM CYCLE
CRT TC
SHT 1 ALE
SHT 4 RAM ADRS
NMI to 8086 to SHT 1
MPU RESET SHT 1
RESET SWITCH
BRESET
RESET
to sht. 2
P14-79 PUP
P14-80
P14-15
P14-16
P14-75, P14-78
CAS Φ
CAS 1
WE1H
WE1L
WE2H
WE2L
RAM WRITE DATA EN
RAS
fm sht. 1
fm sht. 4
RAM PAGE 1
DT/R
8 MHZ to CRT P14-74
8MHZ CLK to sht 2,4
READY to 8088 to sht. 1
SLOW RAM
FAST RAM
last clock
IN = FAST RAM
OUT = SLOW RAM
CLK TO 8086 SLIGHTLY DELAYED, MORE DELAYED ON ↓ EDGE.
SHT 1
24 MHZ IN
24 MHZ OUT
UNUSED
TIMING AND RAM CONTROL
GOULD biomation
TITLE SCHEMATIC - 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV N
SHEET 3 OF 6



REFERENCE PRINT
APR 11 1983
DWG NO 0114-0186
SH 4
REV N
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
RP6 2.2K
RP14 2.2K
RP10 2.2K
3J 256x4 PROM 82S129
3K 256x4 PROM 82S129
10F 512x4 PROM 82S131
ROM8CS
ROM7CS
ROM6CS
ROM5CS
ROM4CS
ROM3CS
ROM2CS
ROM1CS
to sht. 5
from sht. 1
ALE
SHT 1
RAM PAGE 1
RAM ADRS
to sht. 3
I/O ADRS
IO PAGE
P14-11
9C S20
ENOFFBOARD DATA
to sht. 1
EN RAM READ
sht. 2
EN ROM READ
sht. 5
EN S.A. READ
sht. 1
74LS04
LS244
TP1-1
TP1-8
GND
RD
A15
RESET SW.
to sht. 3
fm 8086 sht. 1
ERD
GND1
BWR
GND2
BDEN
BDT/R
BM/IO
P14-7
P14-8
P14-9
P14-10
P14-13
P14-14
P14-12
SH. 1
RP9 3V/6.2K
RP7 3V/6.2K
fm sht 1
111DA
7D 74LS161
7C 74LS161
8C 74LS161
8D 74LS161
7B 74LS161
CA16
CA15
CA14
CA13
CRT page select (to sht. 2)
to sht. 2
RP5 2.2K
CA12
CA11
CA10
CA9
CA8
CA7
CA6
CA5
CA4
CA3
CA2
CA1
R19 220
R20 330
R21 220
R22 330
+5V
DATA DISPLAY INTERFACE
P14-70
P14-71
P14-69
RESET
ENABLE
1/2 MHZ CLOCK
CRT TC
sht. 3
LOAD
to 74LS166
to sht. 2
8MHZ CLK
fm sht 3
R5 2.2K
R18 2.2K
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
TOLERANCE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
GOULD biomation
TITLE SCHEMATIC - 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV N
CODE
SHEET 4 OF 6



DWG. NO. 0114-0186
SH 5
REV N
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
REFERENCE PRINT
APR 11 1983
sht. 4
ROM1CS
ROM2CS
ROM3CS
ROM4CS
ROM5CS
ROM6CS
ROM7CS
ROM8CS
A13
A12
A11
GND
VCC
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
3L
74LS244
3M
74LS244
EN PGM READ
1H
2732
2H
2732
1G
2732
1F
2732
1E
2732
1D
2732
1C
2732
1B
2732
1A
2732
2G
2F
2E
2D
2C
2B
2A
+5
RP1
3K/6.2K
+5V
RP2
3K/6.2K
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
TOLERANCE
GOULD biomation
TITLE SCHEMATIC 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV N
CODE
SHEET 5 OF 6



DWG. NO 0114-0186
SH 6
REV N
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
24 MHZ
QA 11E-5
QB 11E-9
QC 10E-9
8 MHZ 11D-5
4 MHZ 11C-5
8 MHZ
REFERENCE PRINT
APR 11 1983
T1
T2
T3
T4
8086 CLK (4 MHZ)
ALE
MPU CYCLE
MPU RAM CYCLE
RAS
CAS
ROW SELECT
COL SELECT
ADDRESS
DATA
WE
CRT REQUEST
CRT RAM CYCLE
MPU REQUEST
MPU RAM CYCLE
RDY to 8086
CRT REQUEST
no contention
Fast RAM cycle
Worst case for MPU
CRT cycle starts
one CLK before
110
80 nsec
250 nsec
50
WRITE DATA
READ DATA
Data Read
Ti
CLK
Tw
8 MHZ
CLK by 8 MHZ
CRT REQUEST
CRT RAM CYCLE
CRT TC
A1-A14 (N)
A1-A14 (N+1)
D0 (N-1)
D15 (N)
D14 (N)
D13 (N)
D12 (N)
D11
D10
D9
D8
D7
D6
D5
inst clk
A 12E-5
B 12E-9
C 12D-9
D 12D-5
"FAST RAM"
RAM cycle shift register
TIMING DIAGRAMS
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
TOLERANCE
GOULD biomation
TITLE SCHEMATIC - 8086 MPU
SCALE —
SIZE D
PART NUMBER 0114-0186
REV N
CODE
SHEET 6 OF 6

THRESHOLD/GPIB BOARD
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0171

A. ADDRESS DECODING - ALL OF THE ADDRESS AND DATA LINES FROM THE MPU ARE BUFFERED IN TO THE THRESHOLD BOARD VIA THE MOTHERBOARD. (SHEET 5 OF SCHEMATIC)

1. THE MPU DATA BUS IS BUFFERED IN BY THE TWO 74LS245'S (14F AND 12 F).

2. THE K101/102-D VERSION OF THE THRESHOLD/GPIB BOARD SHOULD ALWAYS HAVE THE JUMPER IN FROM E13 TO E14.

   THIS ALLOWS FOR "I/O MAPPED I/O " RATHER THAN MEMORY MAPPED I/O.

B. THRESHOLD VOLTAGES - THE K101/102-D ALLOWS FOR THE THRESHOLD VOLTAGE FOR EACH PROBE TO BE SELECTED FROM ONE OF FOUR SOURCES, VAR A, VAR B, TTL AND ECL.

1. (SHEET 1 OF SCHEMATIC) - THE 74LS273 HOLDING REGISTERS, LOCATION 6D, 4B, 12B AND 9B BUFFER THE MPU DATA BUS TO THE VARIABLE A DAC AND VARIABLE B DAC.

2. THE VARIABLE A DAC (VAR A) IS AT LOCATION 9A. CALIBRATION ADJUSTMENTS FOR VAR A (GAIN R6) (OFFSET R9)

3. THE VARIABLE B DAC (VAR B) IS AT LOCATION 4A. CALIBRATION ADJUSTMENTS FOR VAR B (GAIN R1) (OFFSET R2)

4. BOTH D TO A CONVERTERS HAVE A 10 BIT RESOLUTION.

5. THE TTL AND ECL THRESHOLD BOTH USE A VOLTAGE DIVIDER NETWORK AND ±10 V REFERENCE FOR LEVEL GENERATION.

C. (SHEET 2 OF SCHEMATIC) - THE SELECTION OF THE THRESHOLD VOLTAGE USED BY EACH PROBE IS DONE BY A SET OF 6 MULTIPLEXERS AND BUFFER AMPLIFIERS.

D. GPIB INTERFACE - (SHEET 3 OF SCHEMATIC) - THE GPIB INTERFACE FOR THE K101/102-D HAS BEEN PARTITIONED SUCH THAT THE HANDSHAKE REQUIRED TO TRANSMIT THE INDIVIDUAL BYTES OF INFORMATION, EITHER DATA OR CONTROL, IS DONE BY THE HARDWARE, WHILE ALL MESSAGE GENERATION OR INTERPRETATION IS DONE IN THE SOFTWARE.

1. GPIB MODE AND ADDRESS ARE DETERMINED VIA THE INTERACTIVE DISPLAY ON THE "INTERFACE MENU".
2. ONCE THE MODE IS DETERMINED, THE GPIB CONTROL REGISTER IS LOADED WITH THIS INFORMATION AND THE INTERRUPT IS ENABLED.
3. ALL DATA IS TRANSFERRED INTO OR OUT OF THE K101/102-D UNDER CONTROL OF THE INTERRUPT LINE.
4. IN "LISTEN MODE" THE RECEIPT OF A DATA BYTE OR A COMMAND WILL GENERATE THE INTERRUPT.
5. IN "TALKER MODE", THE INTERRUPT IS PRODUCED WHEN THE BYTE HAS BEEN ACCEPTED BY THE LISTENER.

E. A TO D CONVERTER - ONE OF THE FUNCTIONS CONTAINED ON THE THRESHOLD/GPIB BOARD IS A SOFTWARE CONTROLLED D TO A CONVERTER AND A COMPARATOR THAT PERFORMS A TO D CONVERSIONS FOR SELF-TEST USING A SUCCESSIVE APPROXIMATION SOFTWARE ROUTINE.

1. (SHEET 2 OF SCHEMATIC) - THREE MULTIPLEXERS ARE USED TO SELECT ANY ONE OF THE VOLTAGES USED IN THE K101/102-D. (5F, 6F, AND 7F)
2. THE SELECTED VOLTAGE IS THEN SCANNED BY THE SOFTWARE USING THE 12 BIT D TO A (LOCATION 8A).
3. WHEN THE D TO A VALUE EXCEEDS THE VOLTAGE BEING TESTED THE COMPARATOR (LM324, LOCATION 7A) SWITCHES.
4. THE MICROPROCESSOR COMPARES THE RESULTING VALUE WITH A TABLE OF VOLTAGES AND THEIR TOLERANCES TO DETERMINE THE PASS OR FAIL CONDITION OF THE TEST.

5. THE FRONT PANEL DVM IS BUFFERED ON TO THE THRESHOLD BOARD AT 6F (SHEET 3 OF SCHEMATIC).

G. TIMER - ONE ASPECT OF THE K101/102-D SELF TEST IS PERFORMED BY A PROGRAMMABLE INTERVAL TIMER I.C. (SHEET 4 OF SCHEMATIC) (8E)

1. THE TIMER USES A 2 MHZ CLOCK DERIVED FROM THE MICROPROCESSOR OSCILLATOR TO MEASURE THE EXTERNAL MASTER CLOCK PERIOD.

2. THIS ALLOWS THE MICROPROCESSOR TO TEST ALL OF THE SAMPLE CLOCK RATES.

H. RS232 AND RS449 INFORMATION ENTERS THE THRESHOLD BOARD THROUGH TWO "USARTS" FOUND ON SHEET 4 OF THE SCHEMATIC.

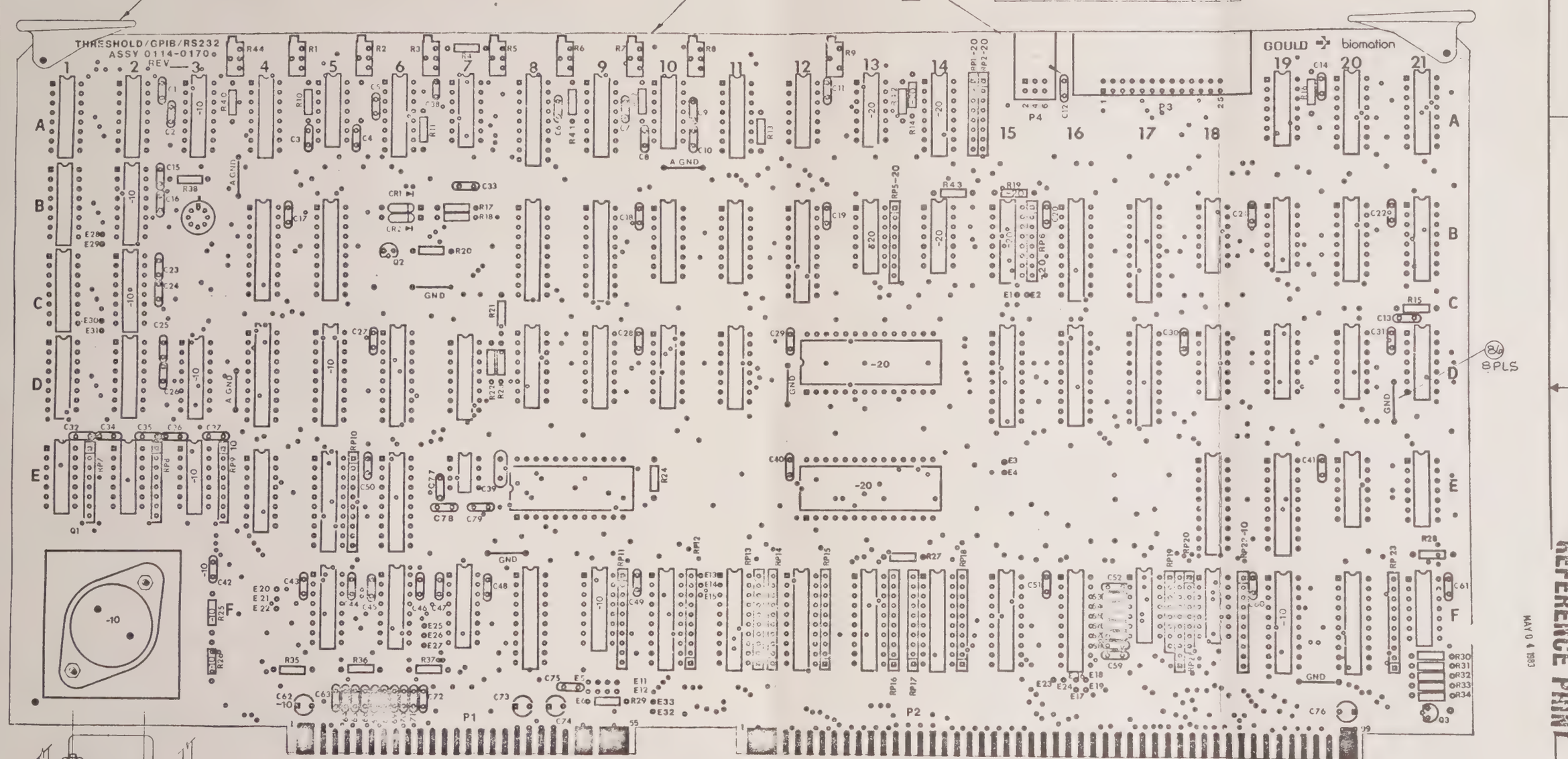
1. USART #1 (LOCATION 12D) HANDLES THE RS232 DATA.

2. USART #2 (LOCATION 12E) HANDLES THE RS449 DATA.

[1] C12 NOT LOADED

REV	ECO	DESCRIPTION	DWN	CHKD	DATE
U	2505	REV'D PER ECO	DWC		
V	3609	REV'D PER ECO			
W	2707	REV'D PER ECO	DWC		
J	1934	REVISED PER ECO			
K	1934	REVISED PER ECO			
L	2179	REVISED PER ECO			
M		REVISED PER ECO			
N					
Q	2498	REV'D PER ECO			
R	2501	REV'D PER ECO			

REV	ECO	DESCRIPTION	DWN	CHKD	DATE
D		REDRAWN PER ECO			
E	1701	REVISED PER ECO	DWC	JL	
F		REVISED PER ECO			
G		REVISED PER ECO			
H		REVISED PER ECO			



REFERENCE PRINT

MAY 0 4 1983

JUMPER LIST				
DESCRIPTION	REF DES	AS ETCH	K500 -10	K101 -20
RS 449 XC	E1-E2	IN		
INTR	E3-E4	IN		
SELECT A11	E5-E6	IN		
SELECT A10	E7-E8	OUT		
SELECT A9	E9-E10	OUT		
[illegible]	[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]		

DESCRIPTION	REF DES	AS ETCH	-10	-20
SELECT M/ID	E13-E14	IN	OUT	
SELECT IO PAGE	E14-E15	OUT	JUMPER	
RS 449 S/G	E16-E17	IN	OUT	
RS 449 S/C	E18-E19	IN	OUT	
[illegible]	E20-E21	OUT	JUMPER	
SELECT VERB MODE	E21-E22	[illegible]	OUT	

DESCRIPTION	REF DES	AS ETCH	-10	-20
	E25-E26	IN	OUT	
	E26-E27	OUT	JUMPER	
	E28-E29	OUT		JUMPER
	E30-E31	OUT		JUMPER
[illegible]	E32-E33	IN	OUT	

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

DRAWN	NELSON	DATE
CHECKED		
PROJ ENG		
MANUFACTURING		
QUALITY ASSUR		
ENG SERV.		DATE

GOULD biomation

TITLE ASSEMBLY THRESHOLD/GPIB/RS232

SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0170	W

CODE SHEET OF

1					1	1	0114-0172	P.C.B.				
2												
3					2	2	7000-0120	EJECTOR				
4					–	1	1700-0090	VOLT REG	Q1		LM 317 K	
5					4	5	1700-0086	OP AMP	1E, 2E, 3E, 5A 1E, 2E, 5A,	10A [1] 10A [2]	LM 324A	
6					1	1	1700-0063-20	I.C.	3B		REF-01EJ	
7												
8					2	2	1820-0077		4A, 9A		AD 7533 LN	
9					9	13	1820-0076		1A-1D, 2A, 2D, 5F, 6F, 7F, 2B, 2C, 3A, 3D [1] 1A-1D, 2A, 2D, 5F, 6F, 7F [2]		AD7508	
10					1	1	1820-0075		8A		AD 7541	
11					2	~	1800-0343		12D 12E		8251	
12					1	1	1800-0344		8E		8253	
13					2	~	1700-0101		13A 13B		14[illegible]	
14					2	~	1700-0102		14A 15B		26 LS 32	
15					1	–	1800-0200		14B		7433	
16					1	1	1800-0125		8D		74 LS 161	
17					13	14	1800-0231	I.C.	4B, 5B, 8B, 9B, 4D, 6E, 18E, 19E, 15F,	6D, 15D, 5E 12B 5D [1]	74 LS 273	
18									4B, 5B, 8B, 9B, 4D, 6E, 18E, 19E, 15F,	6D, 15D, 5E, 12B, [2]		

[1] USED ON K500 ONLY (-10)

[2] USED ON K101 ONLY (-20)

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	REL PER ERN #0092	[illegible]	[illegible]	[illegible]	
B	REVISED PER ECO #1485			[illegible]	
B	PROD REL ERN #129	[illegible]	[illegible]	[illegible]	
C	REVISED PER ECO #1579	[illegible]	[illegible]	[illegible]	
D	REVISED PER ECO #1700	[illegible]	[illegible]	[illegible]	
E	REVISED PER ECO #1701	[illegible]	[illegible]	[illegible]	
F	REVISED PER ECO #1833	[illegible]	[illegible]	[illegible]	

DASH NO.	NUMBER	QTY.
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

DRAWN S. RUDELL — DATE 12-22-80

CHECKED [illegible] — 4/10/81

ENGINEER

MANUFACTURING

QUALITY ASSURANCE

LIST OF MATERIAL

ASSY

THRESHOLD/GPIB/RS 232

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B 0114-0170 REV N

MODEL K101/K500

CODE

SHEET 1 OF 5

19					5	6	1800-0267	I.C.	13F,16F,20F,16B,17B, 19F [1] 13F, 16F, 20F, 16B, 17B [2]		74 LS 240
20					5	5	1800-0240		8F,10F,11F,16D,17D		74 LS 244
21					2	2	1800-0268		12F,14F		74 LS 245
22					5	5	1800-0193		10B,11B,9D-11D		74 LS 138
23					—	1	1800-0254		9F		74 LS 85
24					7	7	1800-0311		17F,18F,21F,18D 19D, ,20E,21E		7438
25					1	1	1800-0110		18B		74 LS 10
26					3	3	1800-0105		21D,19B,20D		74 LS 00
27					4	4	1800-0068		20A,21A,20B,21B		74 LS 112
28					1	1	1800-0111		12A		74 LS 20
29					1	1	1800-0309	I.C.	19A		74 LS 260
30											
31					1	1	1700-0071	I.C.	7E		LF356 AN
32					1	1	1700-0106	I.C.	7A		OP-11E
33					3	3	3000-3300	RESISTOR	R15 R23,33		330, 1/4W 5%
34					6	4	-2201		R20,24,28,30. [1] R14,19,20,24,28,30. [2]		2.2K,
35					4	4	-1001		R35-38		1K,
36					3	3	3000-2200	RESISTOR	R16,22,32		220, 1/4W, 5%

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO # 1885	9-21-81	MS	[illegible]	
H	REVISED PER ECO # 1867	9-21-81	MS	[illegible]	
J	REVISED PER ECO # 1805	9-22-81	BH	[illegible]	
K	REVISED PER ECO # 1954	9-22-81	B.H	[illegible]	
L	REVISED PER ECO # 2179		[illegible]	[illegible]	
M	REVISED PER ECO # 2202	1-29-82	[illegible]	[illegible]	
N	REVISED PER ECO # 2240	1-29-82	[illegible]	[illegible]	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY

THRESHOLD / GPIB / RS 232

biomation

B 0114-0170 REV W

MODEL K101/K500 CODE SHEET 2 OF 5

37					2	–	3000-1004	RESISTOR	R40, 41		1M, ¼W, 5%	
38					1	1	3000-2006		R31		20, ¼W, 5%	
39					1	1	3000-5106		R34		51, ¼W, 5%	
40					1	1	3000-2701		R21		2.7K, ¼W, 5%	
41					3	1	3000-2002		R18 [1] R18,42,43 [2]		20K, ¼W, 5%	
42					–	2	3000-3600		R10, 12		360, ¼W, 5%	
43					~	1	3100-1240		R25		124, ⅛W, 1%	
44					~	1	3100-9760		R26		976,	
45					1	3	3100-1003		R4,11,13 [1] R4 [2]		100K,	
46					1	1	3100-4990		R17		499, ⅛W, 1%	
47					2	~	3000-3302	RESISTOR	R11,13		33K, ¼W, 5%	
48					3	3	3300-0070	POT	R7,8,44		10K, 20T	
49					4	6	3300-0060	POT	R1-3,5,6,9 [1] R2,3,5,9 [2]		500, 20T	
50					2	–	3300-0012	POT	R1,6 [2]		1KΩ, 20T	
51					4	3	3700-0048	RES PACK	6A, 11A, 4E [1] 6A, 11A, 7D, 4E [2]		10K, .1%, 16 PIN	DIP
52					2	3	3700-0083		RP10,11,22 [1] RP10,11 [2]		2.2K 10 PIN	SIP
53					9	9	3700-0049		RP12-18,20,23		3K/6.2K 10 PIN	SIP
54					1	~	3700-0084	RES PACK	RP2		2.7K, 8 PIN 4 RES	SIP

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
P	REVISED PER ECO #2242	1-29-82	[illegible]	[illegible]	
Q	REVISED PER ECO # 2488	4-[illegible]-82	[illegible]	[illegible]	
R	REVISED PER ECO # 2501	4-[illegible]	[illegible]	[illegible]	
S	REVISE PER ECO # 2614	6-28-82	[illegible]	[illegible]	
T	REVISED PER ECO # 2703	11-9-82	[illegible]	[illegible]	
U	REVISED PER ECO # 3589	3/14/83	MW	DWN	3-16-83
V	REVISED PER ECO # 3605	3/15/83	MW	DWN	3-16-83

ASSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY

THRESHOLD / GPIB / RS 232

MODEL K101 / K500

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B	0114-0170	REV W
CODE	SHEET 3 OF 5	

COMPONENTS		COST	COST

	-60	-50	-40	-30	-20	-10	PART NO.	PART NAME	REF DESIGNATION	VENDOR NO		
55					5	2	3700-0056	RES PACK	RP19, 21 [1] RP1, 5, 6, 19, 21 [2]		180, 8 PIN	SIP
56					2	3	3700-0076	RES PACK	RP7, 8, 9 [1] RP7, 8 [2]		47, 8 PIN	SIP
57					2	—	3000-7500	RESISTOR	R10, 12 [2]		750, 1/4W, 5%	
58					2	2	1000-0003	DIODE	CR1, 2		HP 5082-2811	
59					1	1	1300-0028	TRANSISTOR	Q2		2N3904	
60					1	1	1400-0019	TRANSISTOR	Q3		2N3906	
61					1	1	3000-2001	RESISTOR	R27		2K, 1/4W 5%	
62					1	1	3000-3001	RESISTOR	R29		3K, 1/4W 5%	
63					46	47	4010-0103	CAP, CERAMIC	C1, 2, 6, 7, 9, 11, 14-32, 34-37, 39-41, 43-51, 60, 61, 75, 78, 79 [1] C42		.01 µf	
65					14	14	4010-0470	CAP, CERAMIC	C3-5, 8, 10, 13, 33, 38, 53-57, 59		47 pf	
66					1	1	4010-0471	CAP, CERAMIC	C77		470PF, 100V, 5%	
67					12	12	4010-0104	CAP, CERAMIC	C 63-72, 52, 58		.1 µf	
68					2	3	4400-0045	CAP,	C62, 73, 74 [1] C73, C74 [2]		33 µf, 25 V ALUM.	
69					1	1	4400-0043	CAPACITOR	C76		47 µf, 6V ALUM.	
70												
71					1	1	6000-0417	HEADER	P4		6 PIN	
72					1	1	6000-0388-20	HEADER	P3		26 PIN, SHORT EARS	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	W	REVISED PER ECO #3706	5/4/83	MW	DGW	5/4/83

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY

THRESHOLD / GPIB / RS232

MODEL K101 / K500

biomation

CODE		REV
B	0114-0170	W

SHEET 4 OF 5

73					-	1	7000-0418	HEAT SINK	@ Q1				
74					2	1	6100-0119	SOCKET 14 PIN DIP	(X7A)-10 (X7A,X14B)-20				
75					2	2	6100-0120	SOCKET 16 PIN DIP	X 4A, 9A				
76					1	1	6100-0049	SOCKET 18 PIN DIP	X 8A				
77					1	1	6100-0122	SOCKET 24 PIN DIP	X 8E				
78					2	~	6100-0151	SOCKET 28 PIN DIP	X 12D, X12E				
79													
80					—	1	7200-0016	INSULATOR			TO-3		
81					—	2	7000-0221	WASHER			#4 INSULATING		
82					—	2	———	SCREW			#4-40 P.H.		
83					—	2	———	WASHER			#4 FLAT		
84					—	2	———	KEP NUT			#4-40		
85													
86					8	8	9000-0054	BUS WIRE			GND STRAP		
87													
88													
89													
90													

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY

THRESHOLD / GPIB / RS 232

MODEL K101 / K500

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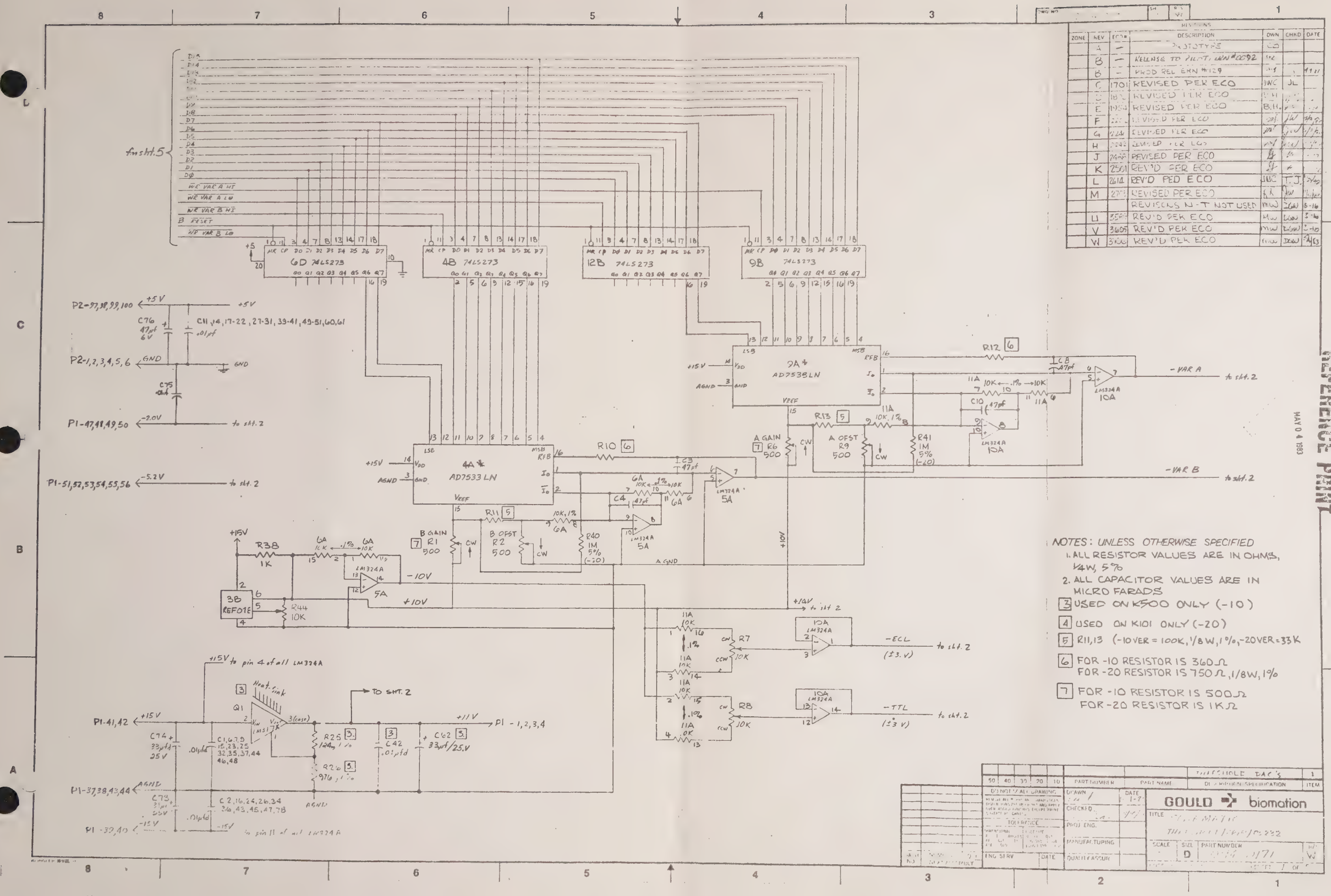
B	0114-0170	REV W
CODE		SHEET 5 OF 5



REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
A | — | PROTOTYPE
B | — | RELEASE TO PILOT, ERN #0092
B | — | PROD REL ERN #1129
C | 1701 | REVISED PER ECO | JWC | JL
D | 1800 | REVISED PER ECO
E | 1954 | REVISED PER ECO | B.H.
F | REVISED PER ECO
G | 2241 | REVISED PER ECO
H | 2242 | REVISED PER ECO
J | 2488 | REVISED PER ECO
K | 2501 | REV'D PER ECO
L | 2614 | REV'D PER ECO | JWC | T.J.
M | 2703 | REVISED PER ECO
REVISIONS N-T NOT USED
U | 3589 | REV'D PER ECO | MW | DGW | 3-16
V | 3605 | REV'D PER ECO | MW | DGW | 3-10
W | 3700 | REV'D PER ECO | MW | DGW | 3-23
fn sht. 5
WR VAR A HI
WR VAR A LO
WR VAR B HI
B RESET
WR VAR B LO
6D 74LS273
4B 74LS273
12B 74LS273
9B 74LS273
9A AD7533LN
4A AD7533LN
P2-97,98,99,100 +5V
P2-1,2,3,4,5,6 GND
P1-47,48,49,50 -2.0V to sht. 2
P1-51,52,53,54,55,56 -5.2V to sht. 2
C76 47µf 6V
C11,14,17-22,27-31,39-41,49-51,60,61 .01µf
C75 .01µf
R12 6
C8 47pf
LM324A 10A
-VAR A to sht. 2
-VAR B to sht. 2
R13 5
A GAIN R6 500
A OFST R9 500
R41 1M 5% (-20)
C10 47pf
R10 6
C3 47pf
C4 47pf
LM324A 5A
R11 5
B GAIN R1 500
B OFST R2 500
R40 1M 5% (-20)
R38 1K
LM324A 5A
-10V
+10V
3B REFOTE
R44 10K
+14V to sht. 2
R7 10K
R8 10K
-ECL (±3.V) to sht. 2
-TTL (±3 V) to sht. 2
+15V to pin 4 of all LM324A
Heat sink
Q1 LM317K
TO SHT. 2
P1-41,42 +15V
P1-37,38,43,44 AGND
P1-39,40 -15V
C74 33µf 25V
C73 33µf 25V
C1,6,7,9 15,23,25 32,35,37,44 46,48
C2,16,24,26,34 36,43,45,47,78
R25 124
R26 976
C42 .01µf
C62 33µf/25.V
+11V P1-1,2,3,4
to pin 11 of all LM324A
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS
3 USED ON K500 ONLY (-10)
4 USED ON K101 ONLY (-20)
5 R11,13 (-10VER = 100K, 1/8W, 1%, -20VER = 33K
6 FOR -10 RESISTOR IS 360Ω FOR -20 RESISTOR IS 750Ω, 1/8W, 1%
7 FOR -10 RESISTOR IS 500Ω FOR -20 RESISTOR IS 1KΩ
THRESHOLD DAC'S
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
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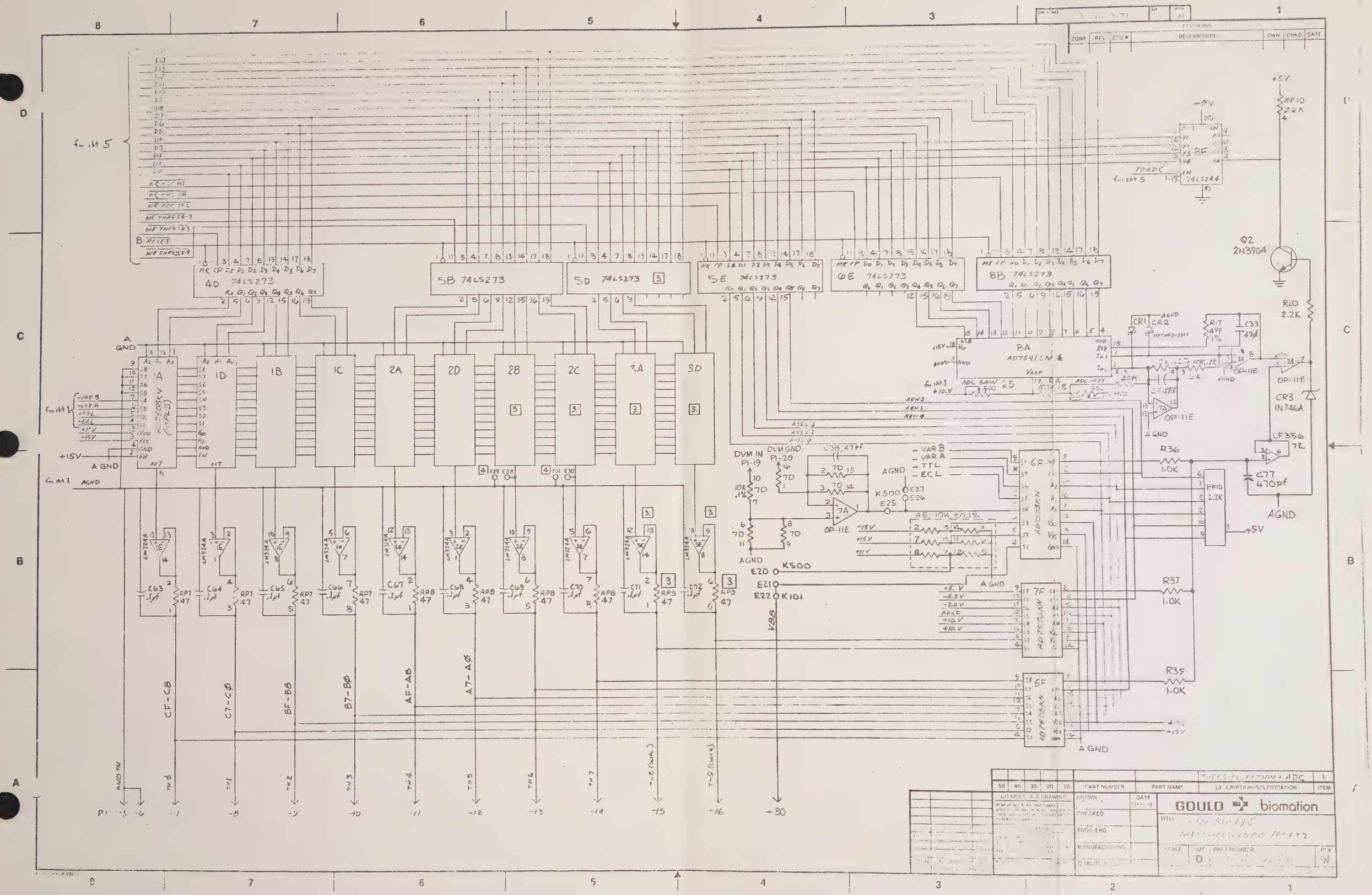
TITLE
SCALE
SIZE D
PART NUMBER
REFERENCE PRINT
MAY 04 1983



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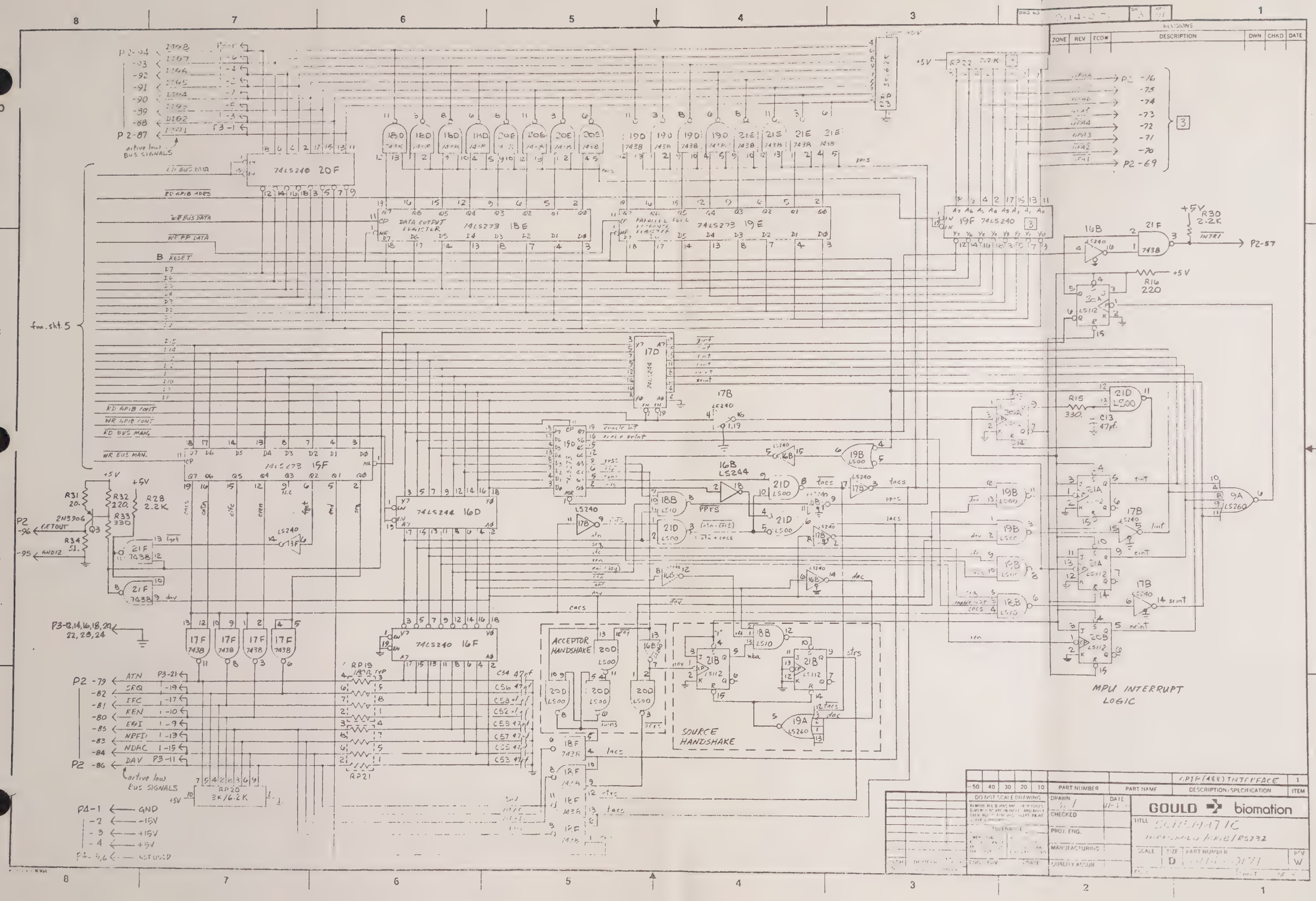
DESCRIPTION/SPECIFICATION
PART NUMBER
PART NAME
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
SCALE
SIZE
PART NUMBER
REV
ITEM
DO NOT SCALE DRAWING



REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
active low BUS SIGNALS
RD BUS DATA
RD GPIB ADRS
WR BUS DATA
WR PP DATA
RESET
fm. sht. 5
RD GPIB CONT
WR GPIB CONT
RD BUS MAN.
WR BUS MAN.
74LS240 20F
74LS273 18E
74LS273 19E
74LS240 19F
74LS273 15F
74LS244 16D
74LS240 16F
DATA OUTPUT REGISTER
PARALLEL POLL RESPONSE REGISTER
ACCEPTOR HANDSHAKE
SOURCE HANDSHAKE
MPU INTERRUPT LOGIC
P2-57
P2-69
P3-12,14,16,18,20,22,23,24
P2-79 ATN
-82 SRQ
-81 IFC
-80 REN
-85 EOI
-83 NRFD
-84 NDAC
P2-86 DAV
active low BUS SIGNALS
P4-1 GND
-2 -15V
-3 +15V
-4 +5V
P4-5,6 NOT USED
GPIB (488) INTERFACE
DO NOT SCALE DRAWING
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
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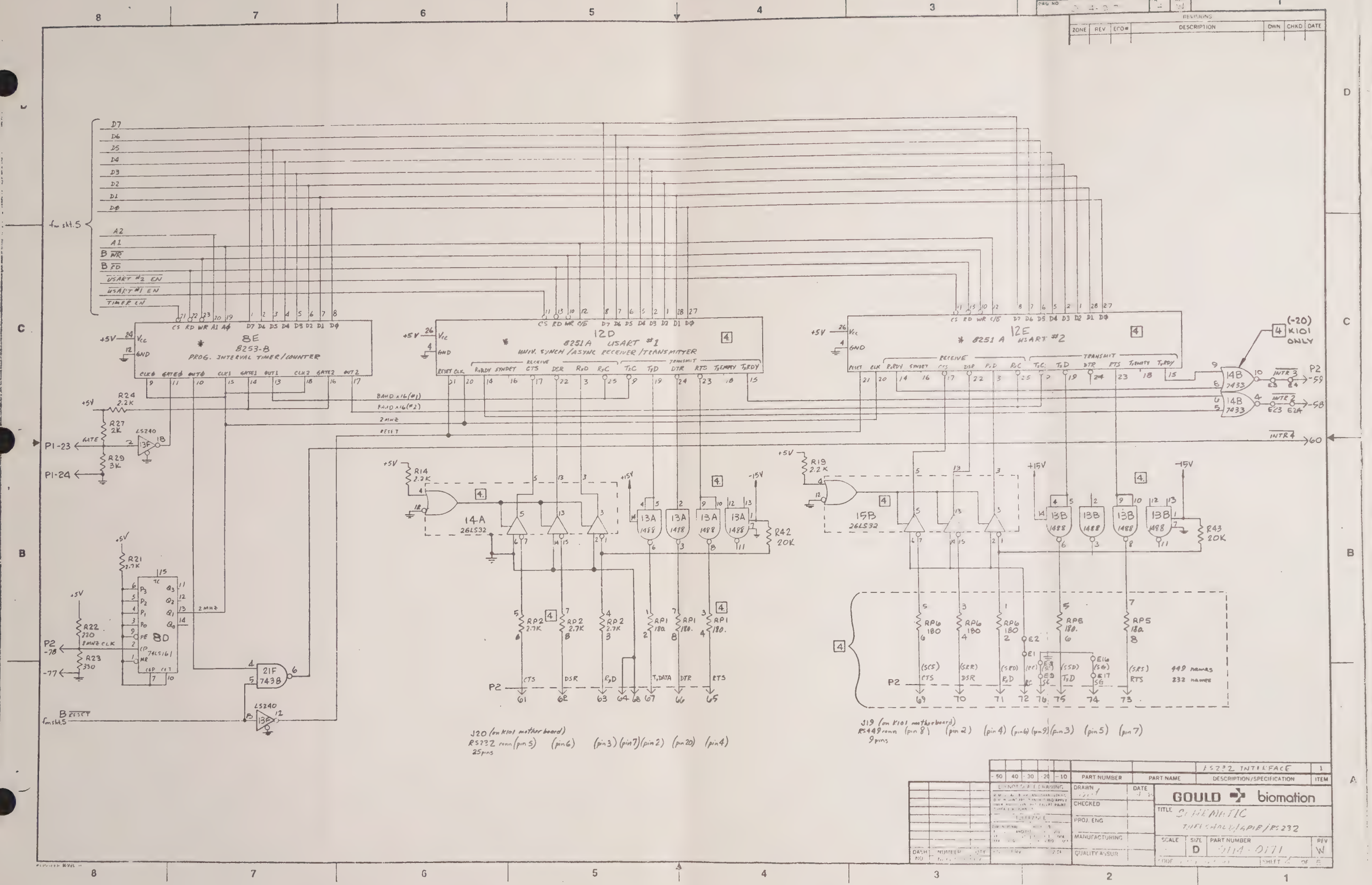
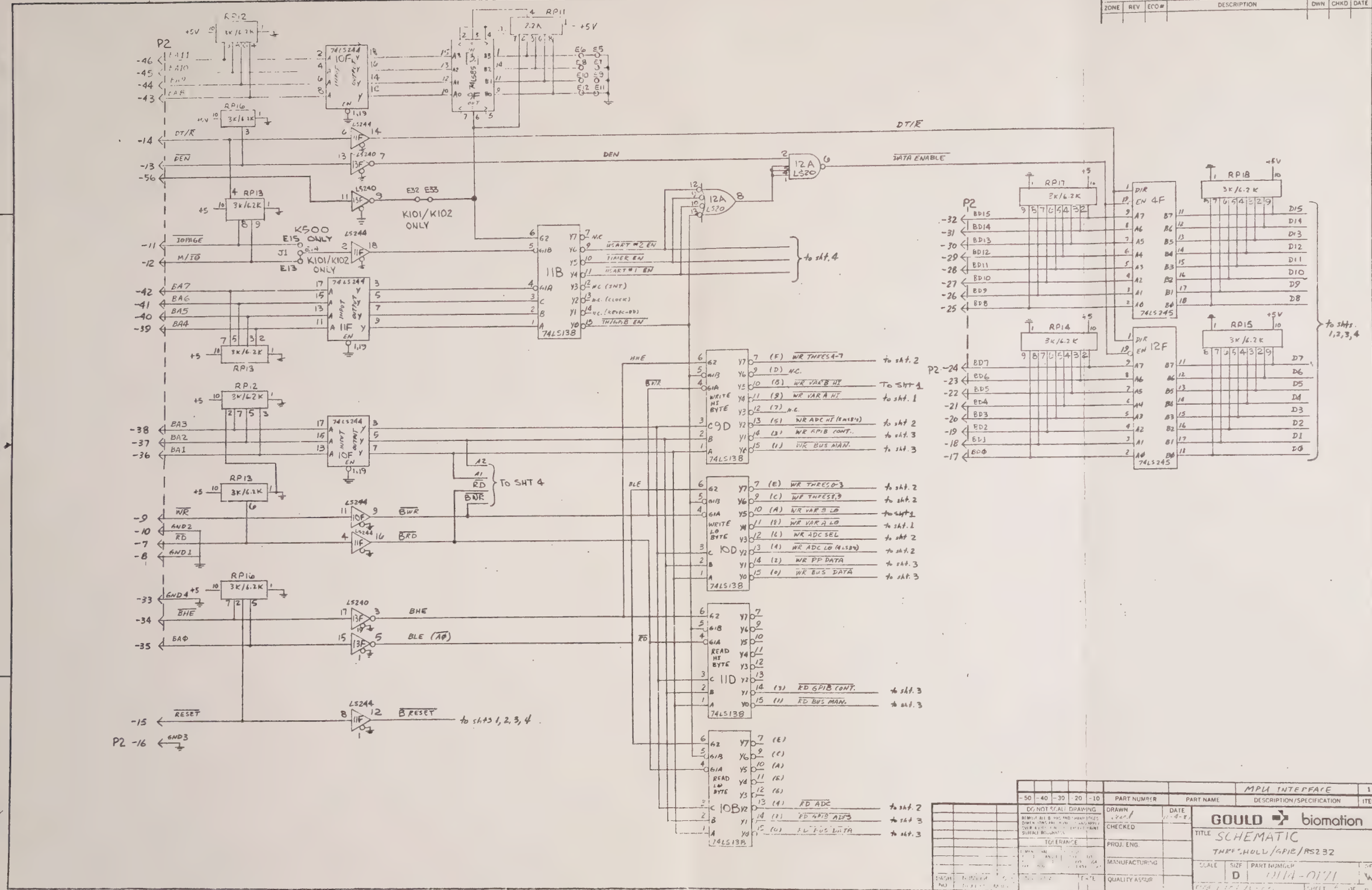
TITLE SCHEMATIC
SCALE
SIZE D
PART NUMBER
REV W



8E
8253-B
PROG. INTERVAL TIMER/COUNTER
12D
8251A USART #1
UNIV. SYNCH/ASYNC RECEIVER/TRANSMITTER
12E
8251 A USART #2
(-20) K101 ONLY
14B 7433
14A 26LS32
15B 26LS32
13A 1488
13B 1488
8D 74LS161
21F 7438
LS240
R24 2.2K
R27 2K
R29 3K
R21 2.7K
R22 220
R23 330
R14 2.2K
R19 2.2K
R42 20K
R43 20K
RP2 2.7K
RP1 180
RP6 180
RP5 180
P1-23
P1-24
P2
-78
-77
BAUD x16(#1)
BAUD x16(#2)
2MHZ
RESET
INTR 3
INTR 2
INTR 4
-59
-58
60
J20 (on K101 motherboard)
RS232 conn (pin 5) (pin 6) (pin 3) (pin 7) (pin 2) (pin 20) (pin 4)
25 pins
J19 (on K101 motherboard)
RS449 conn (pin 8) (pin 2) (pin 4) (pin 6) (pin 9) (pin 3) (pin 5) (pin 7)
9 pins
449 names
232 names
RS232 INTERFACE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE
SIZE D
PART NUMBER 0114-0171
REV W
SHEET 4 OF 5



DWG NO. 0114-0171
SH 5
REV W
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
P2
RP12 3K/6.2K
RP11 2.2K
RP16 3K/6.2K
RP13 3K/6.2K
RP17 3K/6.2K
RP18 3K/6.2K
RP14 3K/6.2K
RP15 3K/6.2K
RP2 3K/6.2K
74LS244
74LS138
74LS245
LS240
LS244
LS20
DT/R
DEN
DATA ENABLE
K500 ONLY
K101/K102 ONLY
IOPAGE
M/IO
BA7
BA6
BA5
BA4
BA3
BA2
BA1
WR
GND2
RD
GND1
GND4
BHE
BAΦ
RESET
GND3
11B
9F
10F
11F
12A
12A
9D
10D
11D
10B
4F
12F
USART #2 EN
TIMER EN
USART #1 EN
N.C. (INT)
N.C. (CLOCK)
N.C. (KEYBOARD)
TH/GPIB EN
to sht. 4
to shts. 1,2,3,4
WR THRES4-7
WR VAR B HI
WR VAR A HI
WR ADC HI (8MSB'S)
WR GPIB CONT.
WR BUS MAN.
WR THRES0-3
WR THRES8,9
WR VAR B LO
WR VAR A LO
WR ADC SEL
WR ADC LO (4LSB'S)
WR PP DATA
WR BUS DATA
RD GPIB CONT.
RD BUS MAN.
RD ADC
RD GPIB ADDS
RD BUS DATA
To SHT 1
To SHT 4
to sht. 1
to sht. 2
to sht. 3
BLE (AΦ)
B RESET
to shts 1, 2, 3, 4
MPU INTERFACE
DESCRIPTION/SPECIFICATION
ITEM
PART NUMBER
PART NAME
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE
SIZE D
PART NUMBER 0114-0171
REV W

CLOCK BOARD
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0161

THE CLOCK BOARD HOLDS THE CIRCUITRY TO PROVIDE ALL INTERNAL CLOCK PERIODS AND PROGRAMMABLE LOGIC FUNCTIONS WHICH DECODE THE EXTERNAL CLOCK INPUTS IN ACCORDANCE WITH THE "MASTER CLOCK", "SAMPLE CLOCK" AND "ENABLE" BOOLEAN EXPRESSIONS SELECTED BY THE INSTRUMENT OPERATOR.

ALSO, THE LEVEL MEMORY, WHICH STORES THE LEVEL AT WHICH EACH SAMPLE WAS RECORDED, IS LOCATED ON THE CLOCK BOARD.

A. ALL INTERNAL CLOCKS ARE DERIVED FROM THE 100 MHZ OSCILLATOR SHOWN ON SHEET 1 OF THE CLOCK BOARD SCHEMATICS.

1. THE POT R19 ALLOWS ADJUSTMENT OF THE AVERAGE VALUE OF THE 100 MHZ SIGNAL ON THE EMITTER OF Q2 SO THAT THE SYMETRY OF THE CLOCK OUTPUT AT 12C-12 CAN BY SET.

   VARIABLE CAPACITOR C8 ADJUSTS THE OSCILLATOR FREQUENCY.

2. IC'S 9E AND 10E ARE 10137 BCD COUNTERS CONNECTED AS DECADE DIVIDERS TO PROVIDE THE 10 MHZ AND 1 MHZ DECADES.

   THE 1 MHZ OUTPUT OF 10E GOES TO Q1 WHICH SHIFTS THE LEVEL, MAKING IT COMPATABLE WITH THE INPUT REQUIREMENTS OF IC 9C.

3. IC'S 9C AND 9D ARE CMOS DUAL BCD COUNTERS OPERATING BETWEEN -5 V AND GROUND FOR ECL COMPATABILITY.

4. THE OUTPUTS OF ALL 6 DECADE DIVIDERS ARE FED TO THE INPUTS OF THE 10164 8 TO 1 MULTIPLEXER AT 10C.

   THE MPU CAN SELECT ANY DECADE AS THE OUTPUT OF 10C.

5. FOR CLOCK FREQUENCIES GREATER THAN 10 MHZ, THE SELECT LINES TO 10C AND THE 10109 "OR" GATE AT 10D ARE SET TO ALL ZEROS BY THE MPU.

   THIS ENABLES THE 100102 AT 12C TO PASS THE 100 MHZ (10 NSEC) CLOCK.

6. THE SELECTED DECADE FEEDS THE INPUT TO THE 10016 PROGRAMMABLE BINARY COUNTER AT 11B.

7. THE COMBINATION OF THE DECADE DIVIDERS COMBINED WITH THE PROGRAMMABLE COUNTER ALLOWS THE SELECTION OF CLOCK PERIODS FROM 10 NSEC TO 160 NSEC IN A 1 THROUGH 16 SEQUENCE.

8. THE BCD OUTPUTS OF THE 100 KHZ DECADE COUNTER ALSO DRIVE THE SELECT LINES OF THE 4028 CMOS DE-MULTIPLEXER AT 9B.

   THE OUTPUTS OF 9B PROVIDE A 1 OF 8 PULSE PATTERN TO A JACK ON THE INSTRUMENT FRONT PANEL AS PROBE TEST DATA.

   THE 1 MHZ CLOCK AND THE LSB OF 9C ARE ALSO FED TO THE PROBE TEST JACK AS TEST CLOCKS.

B. <u>EXTERNAL CLOCK CIRCUITS</u> AND <u>CLOCK DISTRIBUTION</u> CAN BE FOUND ON <u>SHEETS 2 AND 3</u> OF THE SCHEMATIC:

   3 LATCH ENABLES

   3 SAMPLE CLOCKS

   1 CONTROL (MASTER) CLOCK

ALL 7 CIRCUITS ARE ESSENTIALLY THE SAME. ONLY THE CONTROL CLOCK SELECTION, WHICH IS THE MOST COMPLEX, WILL BE DISCUSSED HERE.

1. THE CONTROL CLOCK SELECTION GATES HAVE 13 INPUTS:

1	INTERNAL CLOCK	
3	"AND" CLOCKS	(AJ,BJ,CJ)
3	"$\overline{\text{AND}}$" CLOCKS	($\overline{AJ}$,$\overline{BJ}$,$\overline{CJ}$)
3	"OR" CLOCKS	(AK,BK,CK)
3	"$\overline{\text{OR}}$" CLOCKS	($\overline{AK}$,$\overline{BK}$,$\overline{CK}$)

NOTE: THE MAJOR DIFFERENCE BETWEEN CONTROL CLOCK SELECTION AND THE LATCH ENABLE SELECTION IS THE ABSENCE OF INTERNAL CLOCKS FOR LATCH ENABLE AND THE EXISTENCE OF INTERNAL "MPU" DIAGNOSTIC LATCH ENABLE!!

C. "AND" CLOCKS (MASTER CLOCKS) — ARE SELECTED BY THE 100102 GATES AT 3H AND 5H ON SHEET 3 OF THE SCHEMATIC.

1. EACH OF THESE GATES HAS 3 INPUTS.
2. PIN 19 IS COMMON TO ALL GATES AND IS DRIVEN BY THE OUTPUT OF THE "OR" CLOCK SELECTION GATES.
3. ONE PIN OF EACH OF THE GATES IS DRIVEN BY ONE OF THE "J" CLOCK INPUTS OR THEIR COMPLEMENTS.
4. THE MPU CONTROLS THE THIRD INPUT, PLACING A LOW ON THOSE GATES WHO'S "J" CLOCK INPUT WILL BE HIGH WHEN THE SELECTED CLOCK IS TRUE.
5. ONLY WHEN ALL SELECTED "AND" CLOCKS OR THE "OR" CLOCK IS TRUE, WILL ALL OF THE OUTPUTS OF 3H AND 5H BE LOW, ALLOWING CONTROL CLOCK AT 4J-9 TO GO HIGH.

D. INTERNAL CLOCK DISTRIBUTION CAN BE FOUND ON SHEET 3 OF THE SCHEMATIC.

1. WHEN AN INTERNAL CLOCK MODE IS SELECTED, ALL EXTERNAL CLOCKS ARE DE-SELECTED BY THE MPU AND 3H-21 IS PULLED LOW, ENABLING INTERNAL CLOCKS TO PASS THROUGH TO 4J-9.

E. "OR" CLOCK SELECTION IS SHOWN ON SHEET 3 OF THE SCHEMATIC.

1. THE "OR" CLOCKS ARE SELECTED BY THE 100102'S AT 5D AND PARTS OF 4A AND 4D.
2. THE "MPU" PLACES A LOW ON ONE INPUT OF EACH GATE WHOSE OTHER INPUT WILL BE LOW WHEN ONE OF THE SELECTED "OR" CLOCKS IS TRUE.

   THE "OR" CLOCKS ARE THE "K" CLOCK INPUTS.

F. SYNCHRONOUS START-UP OF THE CONTROL CLOCK IS PROVIDED BY THE 10231 DUAL FLIP-FLOPS AT 5J ON SHEET 3 OF THE SCHEMATIC.

1. THIS PREVENTS "SLIVER" CLOCKS FOR BEING PASSED AT THE BEGINNING OF A RECORD CYCLE.

G. THE LEVEL MEMORY CIRCUIT CAN BE FOUND ON SHEET 4 OF THE SCHEMATIC.

1. THIS CIRCUIT RECORDS WHAT THE LEVEL OF TRACE CONTROL IS FOR EACH WORD RECORDED ON THE DATA BOARDS.

2. LEVEL DATA ENTERS THE CLOCK BOARD VIA J1, A 20-PIN HEADER.

3. 10176'S AT 11E AND 11F AND A 10173 AT 11J ACT AS A PIPELINE FOR THE DATA WHILE THE DECISION WHETHER OR NOT TO RECORD IT IS MADE.

   THIS DECISION IS MADE ON THE CONTROL BOARD WHICH SENDS THE SIGNALS "ARMED" AND "TRACED" ALONG WITH THE LEVEL DATA.

4. WHEN "TRACED" IS HIGH, IT'S COMPLEMENT IS CLOCKED INTO 11F ALONG WITH THE LEVEL DATA.

5. THIS THEN ALLOWS 12E TO PRODUCE A WRITE ENABLE PULSE ON THE NEXT CONTROL CLOCK.

6. IF "TRACED" IS FALSE, 12E IS DISABLED AND THE LEVEL DATA IN 11F IS WRITTEN OVER AT THE NEXT SAMPLE WITHOUT BEING RECORDED.

   IF "ARMED" GOES FALSE, THE LEVEL MEMORY LOCKS UP.

7. 10016'S AT 11G AND 12H ARE ADDRESS COUNTERS FOR THE 10422 MEMORIES AT 12G AND 12F.

8. THE LEVEL MEMORY IS MULTIPLEXED TWO WAYS:
   WITH PINS 13 AND 14 OF THE 10231 AT 11D SELECTING WHICH MEMORY PHASE WILL BE WRITTEN TO ON EACH SAMPLE.

9. 11D-3 PROVIDES UNIFORM 10 NSEC PULSES WHEN RECORDING, REGARDLESS OF THE SAMPLE RATE.

10. IN READ MODE, 12D-3 IS DISABLED, MAKING THE OUTPUT OF 11D-3 BECOME 1/2 THE FREQUENCE OF THE INPUT.

11. WHEN "ARMED" GOES FALSE, THE "D" INPUT GOES TRUE, STOPPING THE PULSE.

H. THE MPU INTERFACE IS FOUND ON SHEET 5 OF THE SCHEMATIC.

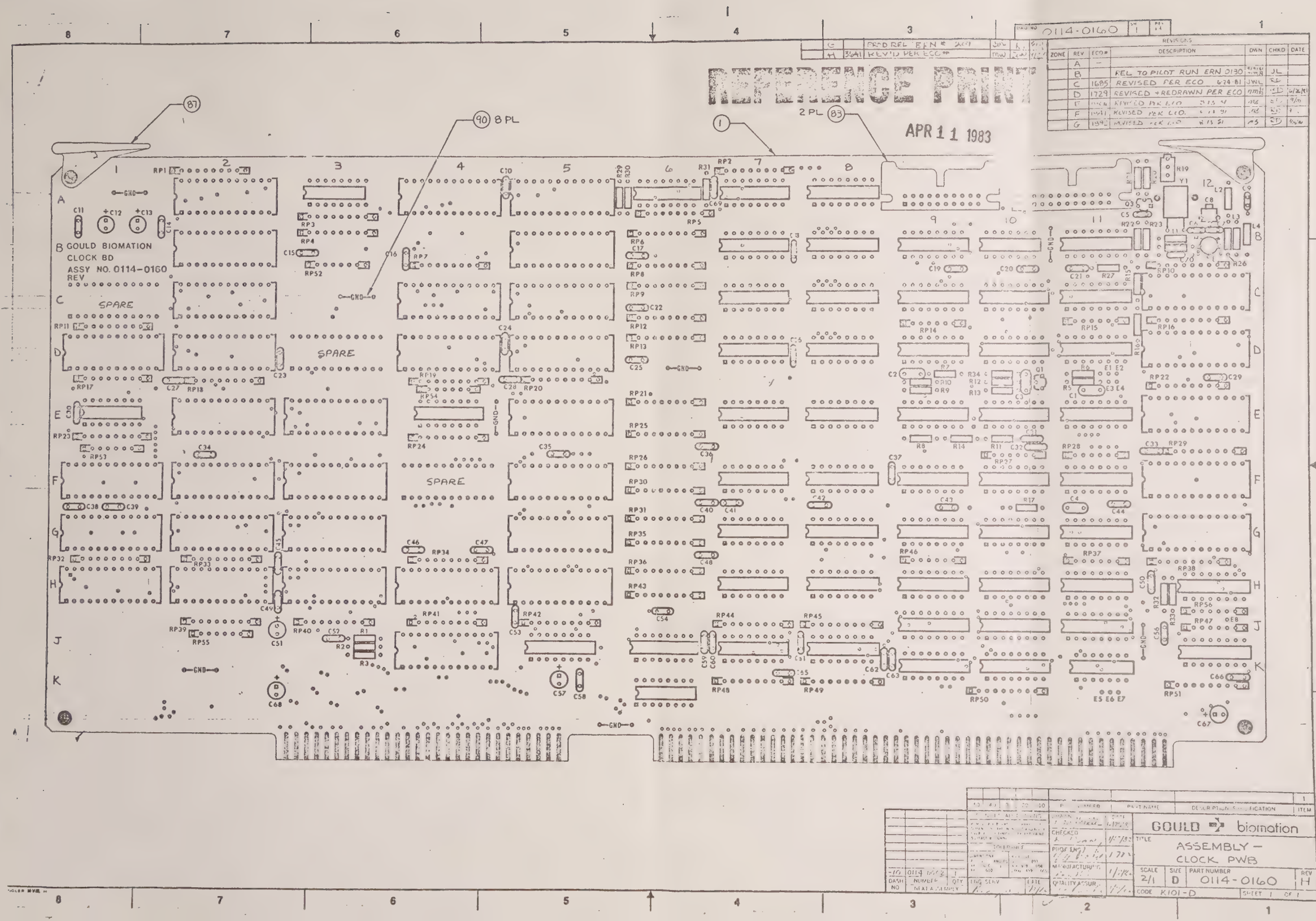
1. THE 74S85 AT 12J DECODES A4-A7 FROM THE MPU TO PROVIDE "MY ADDRESS" WHEN THE CLOCK BOARD IS ADDRESSED.

   "MY ADDRESS" ENABLES THE 10124 TTL TO ECL LEVEL TRANSLATORS WHICH BUFFER THE MPU DATA BUS ON TO THE CLOCK BOARD.

2. THE 10161 DE-MULTIPLEXER AT 9J DECODES A1, A2, AND A3 ALONG WITH THE MPU CONTROL SIGNAL "BWR" TO CREATE "LOAD" PULSES FOR THE 10176 HOLDING REGISTERS AT 7A-7H, 8A-8H, 9G, 9H, 10J, AND 10H.

3. THE 10173 MUX LATCH AT 10G MULTIPLEXES 8 BITS OF READ DATA INTO TWO 4-BIT NIBBLES WHICH ARE TRANSLATED FROM TTL TO ECL LEVELS BY THE 10125 AT 10F.

4. THE 74368 AT 9F IS A TRI-STATE BUFFER WHICH IS ENABLED BY "$\overline{\text{BRD}}$" AND "MY ADDRESS".



REFERENCE PRINT
APR 11 1983
0114-0160
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A —
B REL TO PILOT RUN ERN 0130 JL
C 1685 REVISED PER ECO 6-24-81 JWL
D 1729 REVISED + REDRAWN PER ECO
E REVISED PER ECO
F REVISED PER ECO.
G REVISED PER ECO
GOULD BIOMATION
CLOCK BD
ASSY NO. 0114-0160
REV
SPARE
SPARE
SPARE
GND
GOULD biomation
TITLE ASSEMBLY — CLOCK PWB
SCALE 2/1
SIZE D
PART NUMBER 0114-0160
REV H
CODE K101-D
SHEET 1 OF 1

		COST	COST

	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	FAB
1						1	0114-0162	PWB				FAB
2												
3						2	1400-0019	TRANSISTOR	Q1, Q3		2N3906	
4						4	3000-1200	RESISTOR	R1-3, R34		120Ω 1/4W 5%	
5						1	1300 0038	TRANSISTOR	Q2		BFR 91	
6												
7						1	1800-0105	I.C.	11K		74LS00	
8						1	1800-0254	I.C.	12J		74LS 85	
9						1	1800-0349	I.C.	9F		74368A	
10						1	1800-0280	IC	6K		74 S37	
11						1	1820-0028	I.C.	9B		4028	
12						1	1820-0065	I.C.	10B		4069	
13						2	1820-0063	I.C.	9C, 9D		14518	
14												
15						7	1850-0077	I.C.	1D, 2H, 4C, 4D,		100101	
16									4H, 4J 12E			
17						1	6100-0119	SOCKET	X6K		14 PIN	
18												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REFERENCE ONLY

APR 11 1983

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	4/8/81	NB		
B	RELEASE TO PILOT RUN ERN# 0130	4/9/81	TMH	JL	
C	REVISED PER ECO # 1689	6-24-81	[illegible]	RD	
D	REVISED PER ECO # 1729	6-27-81	TMH	RD	
E	REVISED PER ECO # 1806	8-14-81	MB	RD	
F	REVISED PER ECO # 1841	8-14-81	MB	RD	
G	REVISED PER ECO # 1892	8-14-81	MB	RD	

-10	0114-0002	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	M Bush	3-9-81
CHECKED	R. Dear	2/5/82
ENGINEER	[illegible]	1-7-82
MANUFACTURING	[illegible]	1/7/82
QUALITY ASSURANCE	[illegible]	1/7/82

LIST OF MATERIAL

ASSY, CLOCK PWB

biomation

B	0114-0160	REV H

MODEL K101-D | CODE | SHEET 1 OF 5

									REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						25	1850-0078	I.C.	2A thru 2G, 12C,	12D, 4A	100102	
20						—			5A thru 5H, 3E thru 3H, 1F, 1G, 1H			
21						2	1850-0088	I.C.	12F, 12G		10422	
22						4	1850-0094	I.C.	1E, 4E, 3A, 6A		10216	
23						2	1850-0097	I.C.	5J, 11D,		10231	
24						22	1850-0098	I.C.	7A thru 7H, 9G, 11E, 9H, 10J		10176	
25						—			8A thru 8H, 10H, 11F			
26						2	1850-0105	I.C.	10G, 11J		10173	
27						1	1850-0099	I.C.	10C		10164	
28						1	1850-0100	I.C.	9J		10161	
29						2	1850-0101	I.C.	9E, 10E		10137	
30						1	1850-0103	I.C.	10F		10125	
31						5	1850-0104	I.C.	6J, 7J, 8J, 9K, 10K		10124	
32						1	1850-0108	I.C.	10D		10109	
33						2	1850-0113	I.C.	11H, 11C,		10101	
34						3	1850-0114	I.C.	11B, 11G, 12H		10016	
35						2	6100-0137	SOCKET	12F, 12G		24 PIN	
36						2	2100-0014	INDUCTOR	L2, L3		.1 uh.	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	PROD REL PER ERN #0207	1/24/82	MB	RD	
	H	REV'D PER ECO #3641	4/6/83	MW	DGW	4/7/83

REFERENCE PRINT

APR 11 1983

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY, CLOCK PWB

biomation

B 0114-0160 REV H

MODEL K101-D CODE SHEET 2 OF 5

		COST	COST

	-60	-50	-40	-30	-20	-10	PART NUMBER	PART TYPE	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TITLE
37						1	2100-0012	INDUCTOR	L1		.47uh	
38						1	2100-0036	INDUCTOR	L4		SHIELD BEAD	
39												
40						1	2950-5106	RESISTOR	R24		51Ω 1/8W 5%	
41												
42						1	3000-8200		R21		820Ω 1/4W 5%	
43						1	-1006		R9		10Ω 1/4W 5%	
44						1	-1501		R26		1.5K 1/4W 5%	
45						1	-1600		R15		160Ω 1/4W 5%	
46						1	-1800		R16		180Ω 1/4W 5%	
47												
48						3	-2001		R8, R7, 32		2K 1/4W 5%	
49						4	-2200		R10, 12, 20, 23		220Ω 1/4W 5%	
50												
51						1	-3006		R5		30Ω 1/4W 5%	
52						1	-4700		R13		470Ω 1/4W 5%	
53						1	-5100		R27		510Ω 1/4W 5%	
54						1	3000-5600	RESISTOR	R22		560Ω 1/4W 5%	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME

COMPONENT LEAD SPACING

REFERENCE PRINT

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	APR 11 1983
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY, CLOCK PWB

biomation

B 0114-0160 REV H

MODEL K101-D

CODE

SHEET 3 OF 5

55						1	3000-3001	RESISTOR	R33		3K 1/4W 5%	
56						1	3000-6800	RESISTOR	R6		680Ω 1/4W 5%	
57						3	3000-6806	RESISTOR	R11, 14, 17		68Ω 1/4W 5%	
58						3	3000-2201	RESISTOR	R29, 30, 31		2.2K 1/4W 5%	
59						1	3300-0067	POT	R19		200Ω	
60						1	3700-0051	RES PAK	RP14		10K 8PIN	SI
61						4	-0049		RP48-51		3K/6.2K 10 PIN	S
62						4	-0057		RP47, 52, 53, 54		2.2K 8 PIN	SI
63						4	-0060		RP3, 5, 23, 24		51Ω 10 PIN	S
64						6	3700-0091	RES PAK	RP15, 27, 28, 37,	46, 56	68Ω 8 PIN	
65												
66						36	3700-0092	RES PAK	RP1, 2, 4, 6-13,	16-22	68Ω 10 PIN	S
67						—			25, 26, 29-36, 38-45			
68						1	5100-0004	CRYSTAL	Y1		100 MHZ	
69						1	3700-0096	RES PAK	RP55		100Ω 8PIN 7RES	
70						1	4010-0330	CAPACITOR	C70		33pf	
71						2	4010-0680	CAPACITOR	C1, C3		68 PF	
72												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	AP

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY, CLOCK PWB

APR 1 1 1983

MODEL K101-D

biomation

B 0114-0160

CODE

SHEET 4 OF

73						1	4010-5606	CAPACITOR	C7		5.6pF	
74												
75												
76						57	4010-0103	CAPACITOR	C2,4-6,9-11,14-50		.01 uf	.1 sq.
77									52-54,56,58-63,65,66,69			
78												
79						6	4400-0043	CAPACITOR	C12,13,51,57,67,68		47uf/6V ALUM.	
80						1	4600-0009	VAR. CAP.	C8		1.25-3 pf	
81												
82												
83						2	6000-0384	HEADER	J1, J2		20 PIN RT. ANGLE	
84												
85						2	6100-0137	SOCKET	12F, 12G		24 PIN .4"	
86												
87						1	0112-0228-05	EJECTOR	A5			
88						1	7000-0120	EJECTOR HANDLE				
89												
90						8	9000-0054	GND BUSS				FAB

COST	COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
		APR 11 1983				

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

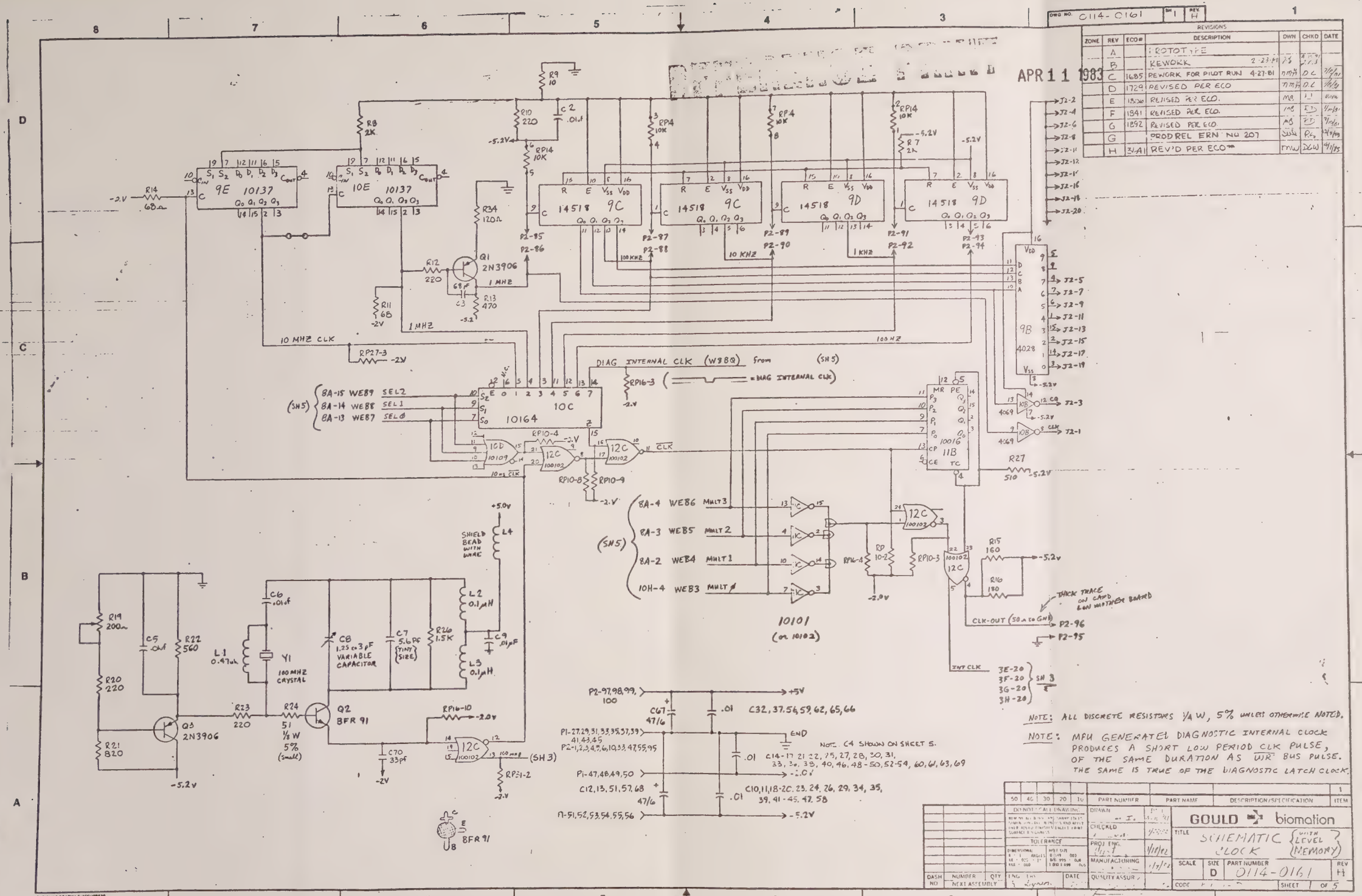
	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

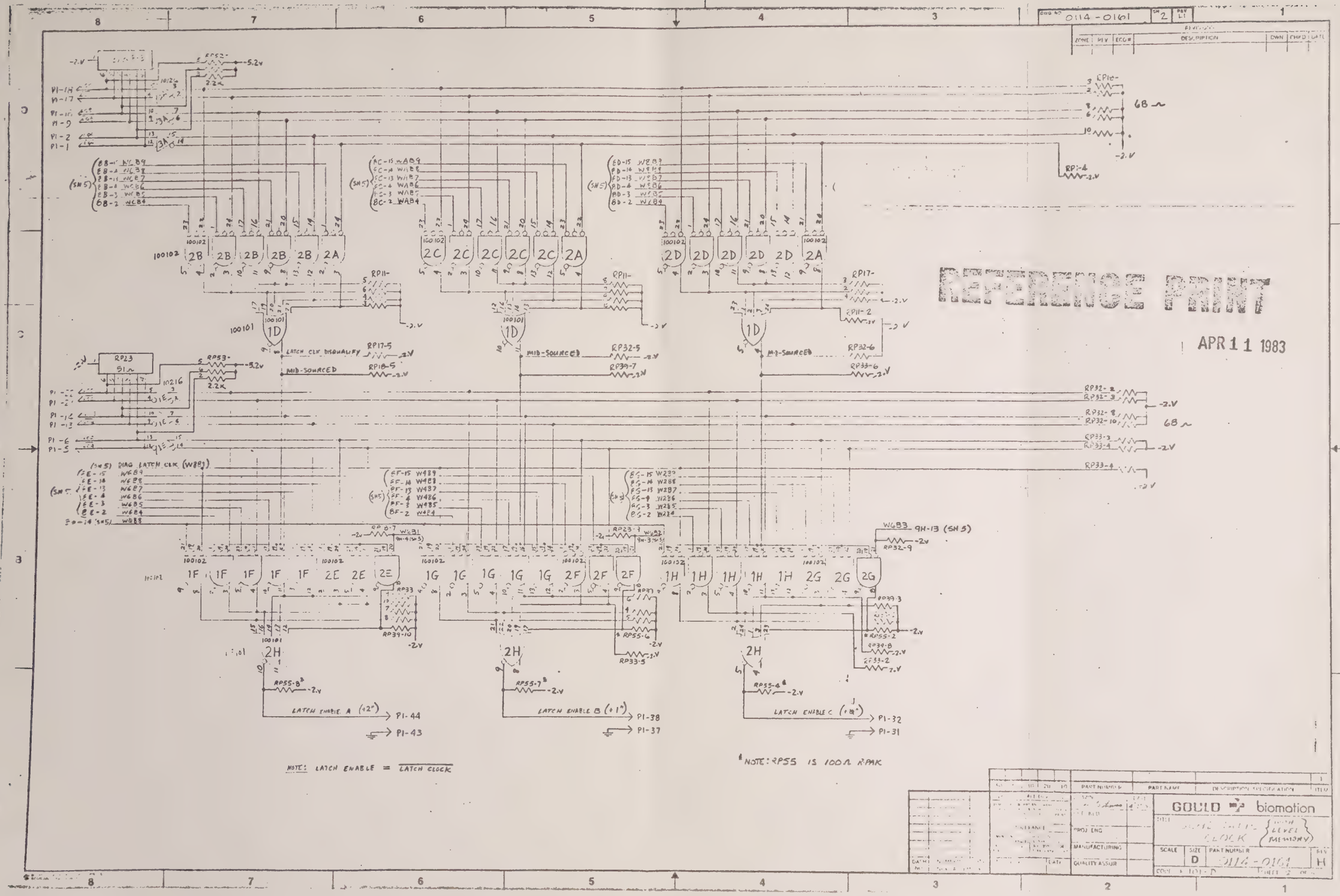
LIST OF MATERIAL

ASSY, CLOCK PWB

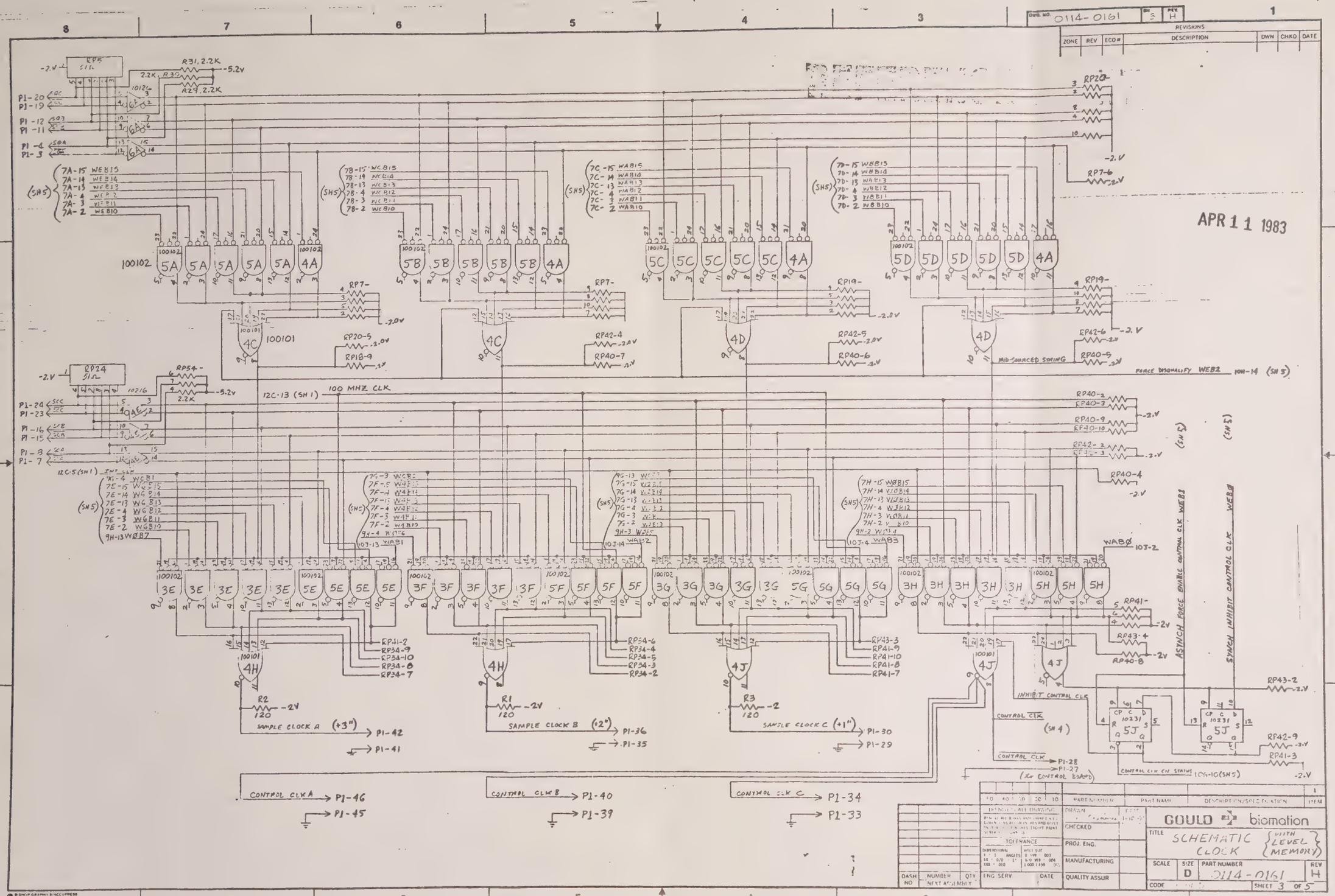
biomation

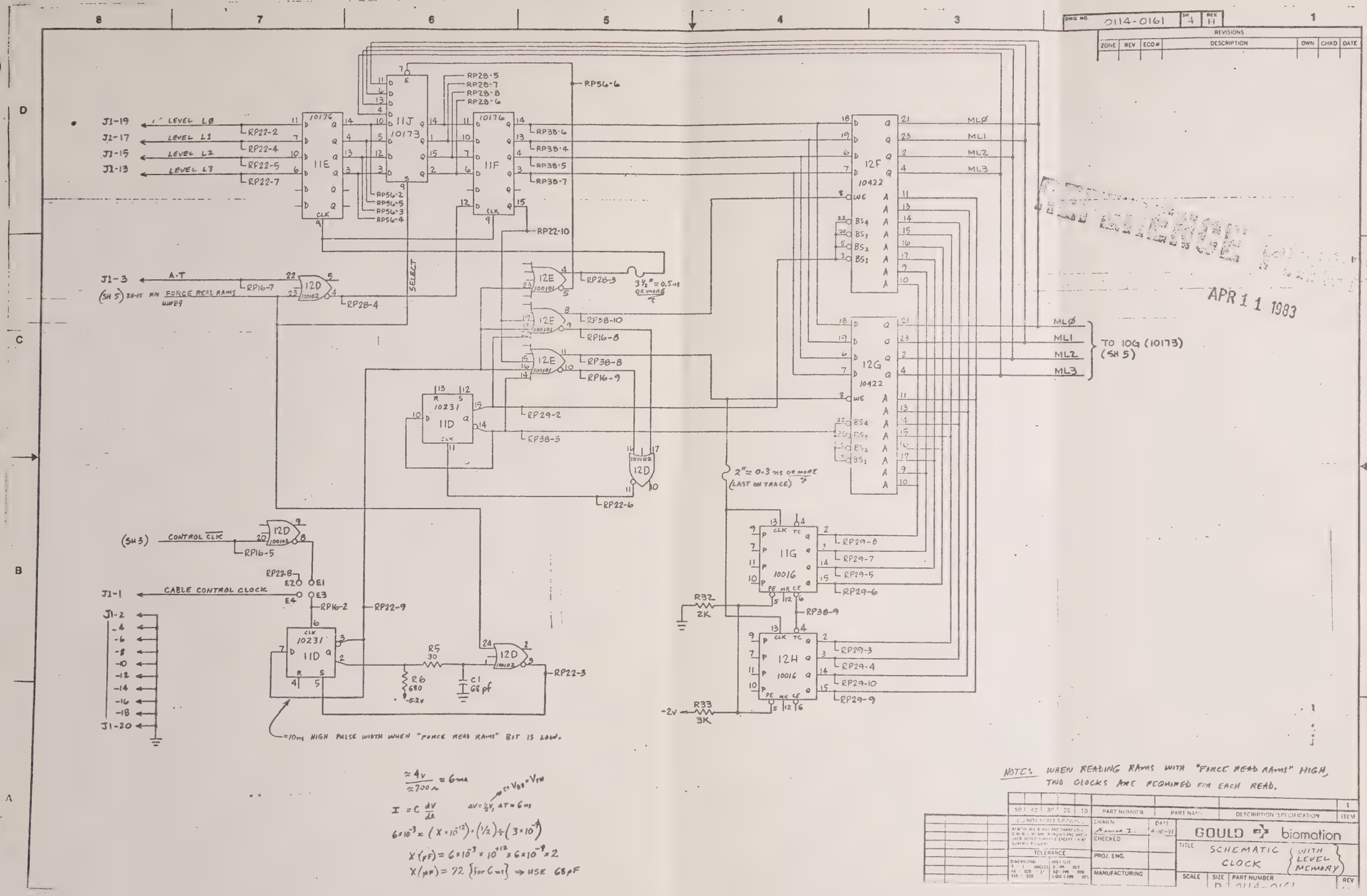
B	0114-0160	REV H
MODEL K101-D	CODE	SHEET 5 OF 5


DWG NO. 0114-0161
SH 1
REV H
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A PROTOTYPE
B REWORK 2-23-81
C 1685 REWORK FOR PILOT RUN 4-27-81
D 1729 REVISED PER ECO
E 1806 REVISED PER ECO.
F 1941 REVISED PER ECO.
G 1892 REVISED PER ECO.
G PROD REL ERN NO 207
H 3141 REV'D PER ECO
APR 11 1983
9E 10137
10E 10137
14518 9C
14518 9C
14518 9D
14518 9D
9B 4028
10C 10164
10101 (or 10102)
11B 10016
12C 100102
10D 10109
4069
Q1 2N3906
Q2 BFR 91
Q3 2N3906
BFR 91
Y1 100 MHZ CRYSTAL
C8 1.25 to 3 pF VARIABLE CAPACITOR
C7 5.6 pF (TINY SIZE)
SHIELD BEAD WITH WIRE
10 MHZ CLK
1 MHZ
100 KHZ
10 KHZ
1 KHZ
100 HZ
DIAG INTERNAL CLK (W8BQ) from (SH5)
= DIAG INTERNAL CLK
CLK
CLK-OUT (50Ω to GND)
THICK TRACE ON CARD LOW IMPEDANCE BOARD
INT CLK
SH 3
NOTE: ALL DISCRETE RESISTORS 1/4 W, 5% UNLESS OTHERWISE NOTED.
NOTE: MPU GENERATED DIAGNOSTIC INTERNAL CLOCK PRODUCES A SHORT LOW PERIOD CLK PULSE, OF THE SAME DURATION AS WR BUS PULSE. THE SAME IS TRUE OF THE DIAGNOSTIC LATCH CLOCK.
NOTE: C4 SHOWN ON SHEET 5.
C32, 37, 56, 59, 62, 65, 66
C14-17, 21, 22, 25, 27, 28, 30, 31, 33, 36, 38, 40, 46, 48-50, 52-54, 60, 61, 63, 69
C10, 11, 18-20, 23, 24, 26, 29, 34, 35, 39, 41-45, 47, 58
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)
SIZE D
PART NUMBER 0114-0161
REV H
SHEET 1 OF 5

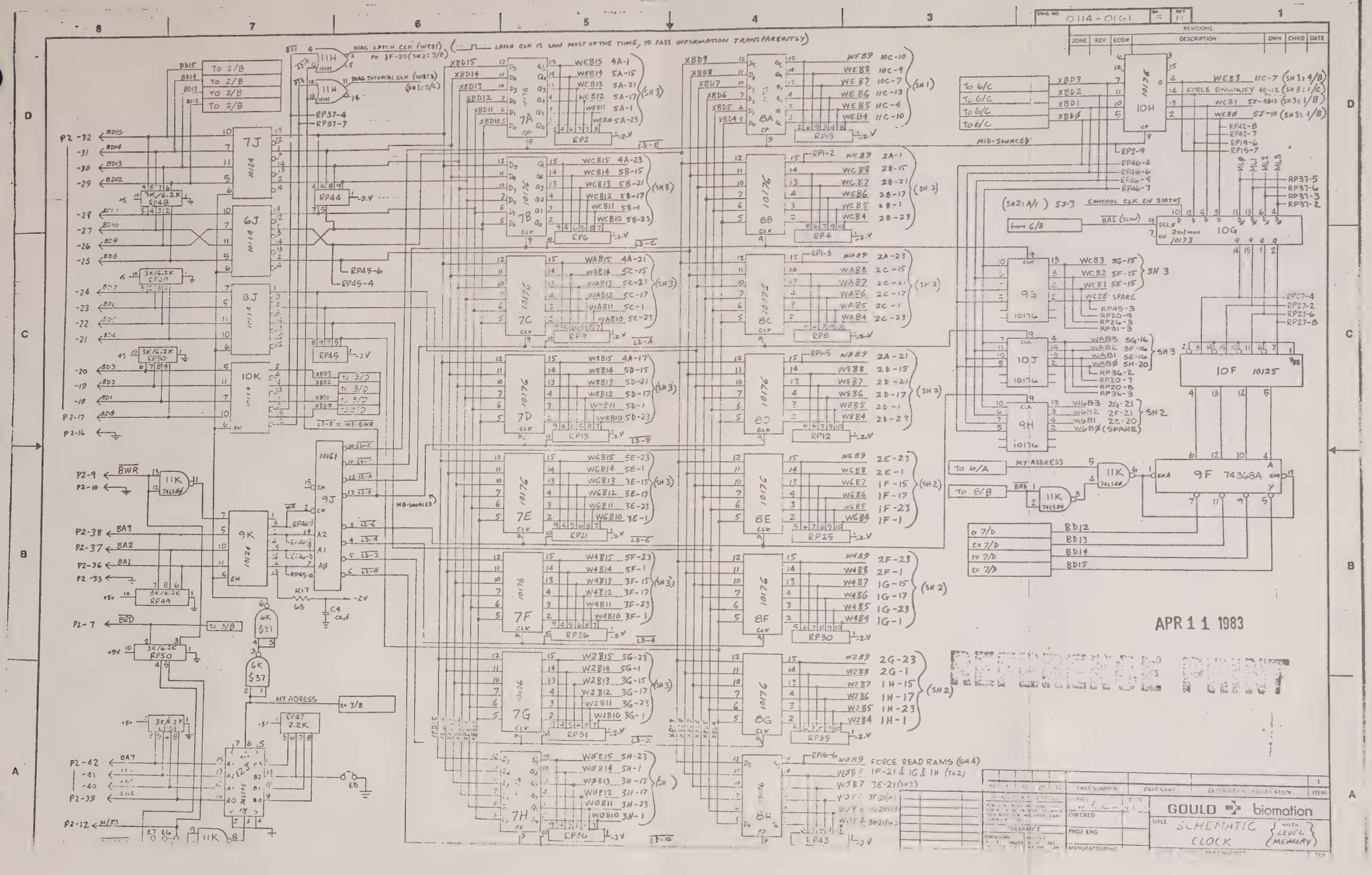


0114-0161
REFERENCE PRINT
APR 11 1983
LATCH CLK DISQUALIFY
MID-SOURCED
DIAG LATCH CLK (W8B9)
LATCH ENABLE A (+2")
LATCH ENABLE B (+1")
LATCH ENABLE C (+0")
P1-44
P1-43
P1-38
P1-37
P1-32
P1-31
NOTE: LATCH ENABLE = LATCH CLOCK
*NOTE: RP55 IS 100Ω RPAK
GOULD biomation
SCALE
SIZE D
PART NUMBER 0114-0161
REV H


DWG. NO. 0114-0161
SH 3
REV H
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
APR 11 1983
100 MHZ CLK
12C-13 (SH 1)
SAMPLE CLOCK A (+3")
SAMPLE CLOCK B (+2")
SAMPLE CLOCK C (+1")
CONTROL CLK A
CONTROL CLK B
CONTROL CLK C
FORCE DISQUALIFY WEB2
ASYNCH FORCE ENABLE CONTROL CLK WEB2
SYNCH INHIBIT CONTROL CLK WEB2
INHIBIT CONTROL CLK
CONTROL CLK
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)
SCALE
SIZE D
PART NUMBER 0114-0161
REV H
SHEET 3 OF 5
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM



DWG NO. 0114-0161 SH 4 REV H
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
J1-19 LEVEL LØ
J1-17 LEVEL L1
J1-15 LEVEL L2
J1-13 LEVEL L3
J1-3 A.T
(SH 5) BH-15 MM FORCE READ RAMS
(SH 3) CONTROL CLK
J1-1 CABLE CONTROL CLOCK
J1-2
-4
-6
-8
-10
-12
-14
-16
-18
J1-20
11E 10176
11J 10173
11F 10176
12D 100102
12E 100101
12F 10422
12G 10422
11D 10231
11G 10016
12H 10016
SELECT
RP56-6
RP28-5
RP28-7
RP28-8
RP28-6
RP22-2
RP22-4
RP22-5
RP22-7
RP56-2
RP56-5
RP56-3
RP56-4
RP38-6
RP38-4
RP38-5
RP38-7
RP22-10
RP16-7
RP28-4
RP28-3
3½" ≈ 0.5ns OR MORE
RP38-10
RP16-8
RP38-8
RP16-9
RP29-2
RP38-3
RP22-6
RP16-5
RP22-8
RP16-2
RP22-9
RP22-3
R5 30
R6 680 -5.2v
C1 68 pf
≈10ns HIGH PULSE WIDTH WHEN "FORCE READ RAMS" BIT IS LOW.
2" ≈ 0.3 ns OR MORE (LAST ON TRACE)
RP29-8
RP29-7
RP29-5
RP29-6
RP38-9
RP29-3
RP29-4
RP29-10
RP29-9
R32 2K
R33 3K
-2v
MLØ
ML1
ML2
ML3
TO 10G (10173) (SH 5)
APR 11 1983
≈ 4v / ≈ 700Ω ≈ 6ma
I = C dV/dt
ΔV = ½V, ΔT = 6ns
6×10⁻³ = (X × 10⁻¹²) · (½) ÷ (3×10⁻⁹)
X(pF) = 6×10⁻³ × 10⁺¹² × 6×10⁻⁹ × 2
X(pF) = 72 {for 6ns} ⇒ USE 68pF
NOTE: WHEN READING RAMS WITH "FORCE READ RAMS" HIGH, TWO CLOCKS ARE REQUIRED FOR EACH READ.
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
DATE 4-10-81
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)
SCALE
SIZE D
PART NUMBER 0114-0161
REV



DWG. NO. 0114-0161
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
DIAG LATCH CLK (WEB1) TO 1F-20 (SH2: 7/B)
LATCH CLK IS LOW MOST OF THE TIME, TO PASS INFORMATION TRANSPARENTLY
DIAG INTERNAL CLK (WEB3) (SH1: 5/C)
MID-SOURCED
FORCE DISQUALIFY
CONTROL CLK EN STATUS
MY ADDRESS
FORCE READ RAMS (SH4)
APR 11 1983
REFERENCE PRINT
GOULD biomation
SCHEMATIC CLOCK
WITH LEVEL MEMORY

HIGH SPEED DATA BOARD
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0110

THE K101-D DATA BOARD,(3 IDENTICAL BOARDS PER SYSTEM), CONTAINS THE FOLLOWING CIRCUITRY:

1. DATA INPUT BUFFERS
2. GLITCH DETECTION LOGIC
3. DATA LATCHES
4. SAMPLE REGISTERS
5. DATA PIPELINE
6. RECORD (HIGH SPEED) MEMORY
7. MEMORY CONTROL LOGIC
8. MPU INTERFACE

A. SHEETS 3, 4, 5, AND 6 OF THE SCHEMATIC DIAGRAM SHOW THE INPUT CIRCUITS, DATA LATCHES, SAMPLE REGISTERS AND RECORD MEMORY FOR 16 CHANNELS OF A SINGLE DATA BOARD.

NOTE: FOR CIRCUIT DESCRIPTION ALL REFERENCES WILL BE TO THE CHANNEL F INPUT FOUND AT THE TOP OF SHEET 3 OF THE SCHEMATIC. THE CIRCUITRY FOR THE OTHER 15 CHANNELS IS IDENTICAL EXCEPT AS NOTED.

B. THE DIFFERENTIAL SIGNAL FROM THE PROBE (SHEET 3) IS BUFFERED ONTO THE BOARD BY THE 10216 LINE RECEIVER/ BUFFER AT LOCATION 2B.

   1. OUTPUT OF THE BUFFER IS PRESENTED TO THE 10121 GATES AT 2D.

C. CONTROL SIGNALS FROM THE MPU HOLDING REGISTERS (SHEET 7) SELECT WHICH OF FOUR DATA SOURCES WILL BE PASSED THROUGH TO THE SAMPLING CIRCUITRY.

THE DATA SOURCES ARE:

1. MEMORY DATA - THIS IS A RECIRCULATION OF THE CHANNEL MEMORY OUTPUT USED ONLY FOR SELF-DIAGNOSTIC PURPOSES. (MEMORY SELECT)

2. PROBE DATA - USED IN NORMAL INPUT MODE. (NORMAL SELECT)

3. MULTIPLEX DATA - DATA FROM THE HIGH ORDER CHANNELS IS ALSO ROUTED TO THE HIGH ORDER CHANNELS (F - 8). IN THIS CASE, CHANNEL F IS PAIRED WITH CHANNEL 7, ALLOWING SINGLE PROBING WHEN DE-MULTIPLEX IS SELECTED. (DEMUX SELECT)

4. DIAGNOSTIC DATA - SUPPLIED BY THE MPU FOR SELF-DIAGNOSTIC PURPOSES.

D. THE OUTPUT OF 2D IS PRESENTED TO THE CIRCUIT MADE UP OF 2E (10106), 2H (10130), AND 2J (10231). THIS CIRCUIT HAS THREE DIFFERENT MODES OF OPERATION.

1. SAMPLE MODE - PINS 6 AND 12 OF THE 10106 (LOCATION 2E) ARE HELD HIGH BY THE MPU, DISABLING THESE GATES IN SAMPLE MODE. 2H-6 AND 9 ARE HELD LOW BY THE MPU WHICH CAUSES THE OUTPUT OF THE LATCH TO FOLLOW THE INPUT ASYNCHRONOUSLY.

   THE 10231 AT 2J IS THE SAMPLE REGISTER. THE INPUT DATA IS TRANSFERRED TO THE OUTPUT AND HELD AT THE RISING EDGE OF THE SAMPLE CLOCK ON PIN 9.

2. LATCH MODE - AS IN SAMPLE MODE GATE 2E IS DISABLED. PIN 6 OF THE 10130 (LOCATION 2H) IS HELD LOW, ALLOWING THE LATCH ENABLE CLOCK AT 2H-9 TO CONTROL THE LATCH.

   WHEN LATCH CLOCK IS LOW, 2H IS TRANSPARENT AS IN SAMPLE MODE. WHEN LATCH CLOCK GOES HIGH, THE DATA THAT WAS TRUE AT THE CLOCK TRANSITION IS HELD AT THE OUTPUT.

- THE 10231 SAMPLE REGISTER AT 2J FUNCTIONS THE SAME AS IN SAMPLE MODE.

3. <u>GLITCH MODE</u> - THE MPU SIGNAL "GLITCH DISABLE" IS LOW IN THIS MODE, ALLOWING THE OUTPUTS OF THE 10106 TO BE CONTROLLED BY THE INPUT DATA AND THE DATA IN THE SAMPLE REGISTER.

   THE MPU SIGNAL "GLITCH ENABLE" IS HIGH IN THIS MODE, DISABLING THE D INPUT OF THE 10130 AT LOCATION 2H.

   THE STATE OF THE LATCH OUTPUT IS THEN CONTROLLED BY THE OUTPUTS OF 2E VIA THE ASYNCHRONOUS SET AND RESET PINS.

E. SAMPLING CIRCUIT OPERATION IS AS FOLLOWS:

1. ASSUME THAT 2H-2 AND 2J-2 ARE HIGH TO START.
2. THE INPUT 2E-5 IS HIGH, DISABLING THE UPPER GATE WHICH GOES TO 2H-5.
3. THE INPUT 2E-13 IS LOW, ALLOWING ANY LOW INPUT SIGNAL TO RESET 2H-2 BY PLACING A HIGH ON 2H-4, THE DIRECT RESET.
4. 2H-2 REMAINS IN THIS NEW STATE REGARDLESS OF ANY ACTIVITY ON THE INPUT SIGNAL.
5. AT THE NEXT SAMPLE CLOCK, THE OUTPUT 2J-15 GOES TO A LOW AND;
6. THE UPPER GATE OF 2E IS ENABLED TO RESPOND TO A HIGH INPUT SIGNAL ONLY.
7. IF AT ANY TIME, THE INPUT SIGNAL GOES HIGH, THE SIGNAL 2D-3 GOES LOW AND 2E-3 GOES HIGH, SETTING THE OUTPUT OF 2H TO A HIGH FOR THE NEXT SAMPLE CLOCK.

F. BESIDES GOING TO THE "GLITCH-FEEDBACK COMPARISON GATES", THE OUTPUTS OF THE SAMPLE REGISTER GO TO THREE PLACES:

1. MULTIPLEXER 2L FOR MPU DIAGNOSTIC ACCESS.
2. TO PIPELINE REGISTER 2K.
3. THE INVERTED DATA FROM 2J-14 GOES TO THE CONTROL BOARD WORD RECOGNITION CIRCUITS.

G. THE "PIPELINE" CONSISTS OF TWO STAGES OF D REGISTERS CONTAINED IN THE 10176 AT 2K. THE SOURCE OF THE "PIPELINE CLOCK" DEPENDS ON THE CLOCK MODE SELECTED.

1. IN EXTERNAL MULTI-PHASE MODE, THE "PIPE CLOCK" IS THE SAME AS THE MASTER CLOCK (CONTROL CLOCK).
2. IN ALL OTHER MODES, THE PIPE CLOCK IS THE SAME AS THE SAMPLE CLOCK.

NOTE THAT THE DATA IN BOTH STAGES OF THE PIPELINE IS ALSO PRESENT AT THE MULTIPLEXERS FOR MPU DIAGNOSTIC ACCESS. (2L & 1L)

H. PIPELINE DATA IS PRESENTED TO THE INPUTS OF BOTH 6E AND 6D WHICH BEGINS TWO-WAY MEMORY MULTIPLEXING.

1. 6E AND 6D ACT AS PRE-MEMORIES AND ARE CLOCKED BY THE RISING EDGE OF THE SIGNALS $\overline{WE}$ Ø1 AND $\overline{WE}$ Ø2 RESPECTIVELY.
2. $\overline{WE}$ Ø1 AND $\overline{WE}$ Ø2 ARE 180° OUT OF PHASE, CAUSING SAMPLES TO BE STORED ALTERNATELY IN THE TWO 10422, 256 X 4 RAMS.

I. THE 10173 AT 5D DEMULTIPLEXES THE MEMORY. THE DATA OUT OF 5D GOES BACK TO THE 10121 INPUT SELECTORS FOR DIAGNOSTIC RECIRCULATION AND TO THE MULTIPLEXERS FOR MPU ACCESS.

J. EACH PHASE OF THE MEMORY HAS ITS OWN ADDRESS COUNTER FOUND ON SHEET 1 OF THE SCHEMATIC. THE COUNTERS ADVANCE ON THE RISING EDGE OF THE $\overline{WE}$ SIGNALS.

K. MEMORY CONTOL LOGIC IS FOUND ON SHEET 2 OF THE SCHEMATIC.

1. THE 100155 MUX LATCH AT 6H KEEPS TRACK OF CONTROL SIGNALS FROM THE MPU AND RECORD CONTROL BOARD.

   6-H ALSO CONTROLS WHICH PHASE OF THE MEMORY WILL BE WRITTEN TO OR READ FROM NEXT VIA THE SIGNALS Ø1 AND Ø2 WHICH ALTERNATELY ENABLE 2 GATES OF THE 100101 AT 5J.

2. WHEN USING AN INTERNAL CLOCK, THE "OLD TRACED" OUTPUT (PIN 2) FROM 6H COMBINES WITH "$\overline{\text{ASYNCH MODE}}$" FROM THE MPU TO FORM "$\overline{\text{MEMORY ALIVE}}$" WHICH ENABLES 5J - 5 & 9.

3. WHEN EXTERNAL SAMPLE CLOCKS ARE SELECTED, "$\overline{\text{MEMORY ALIVE}}$" IS DERIVED FROM THE MPU CONTROL SIGNAL "$\overline{\text{SYNCH MODE}}$" AND "$\overline{\text{TRACED}}$" FROM THE CONTROL BOARD.

   THE OUTPUTS 5J-5 AND 5J-9 ARE THE "$\overline{WE}$" PULSES FOR THE RECORD MEMORIES.

4. THE "HALTED" OUTPUT FROM THE 100155 DISABLES THE GATES AT 5K. THESE GATES PASS THE SAMPLE CLOCK AND SELECT THE SOURCE OF THE PIPE CLOCK.

5. IC 6J DISTRIBUTES ALL CLOCKS AND THE "$\overline{WE}$" SIGNALS. NOTE THAT THE WIDTH OF THE '173 CLOCKS AT 6J-10 IS SET BY A DIFFERENCE IN PROPOGATION DELAY WHEN THE SAME SIGNAL FEEDS BOTH INPUTS VIA TWO DIFFERENT PATHS.

L. THE MPU INTERFACE IS FOUND ON SHEET 7 OF THE SCHEMATIC.

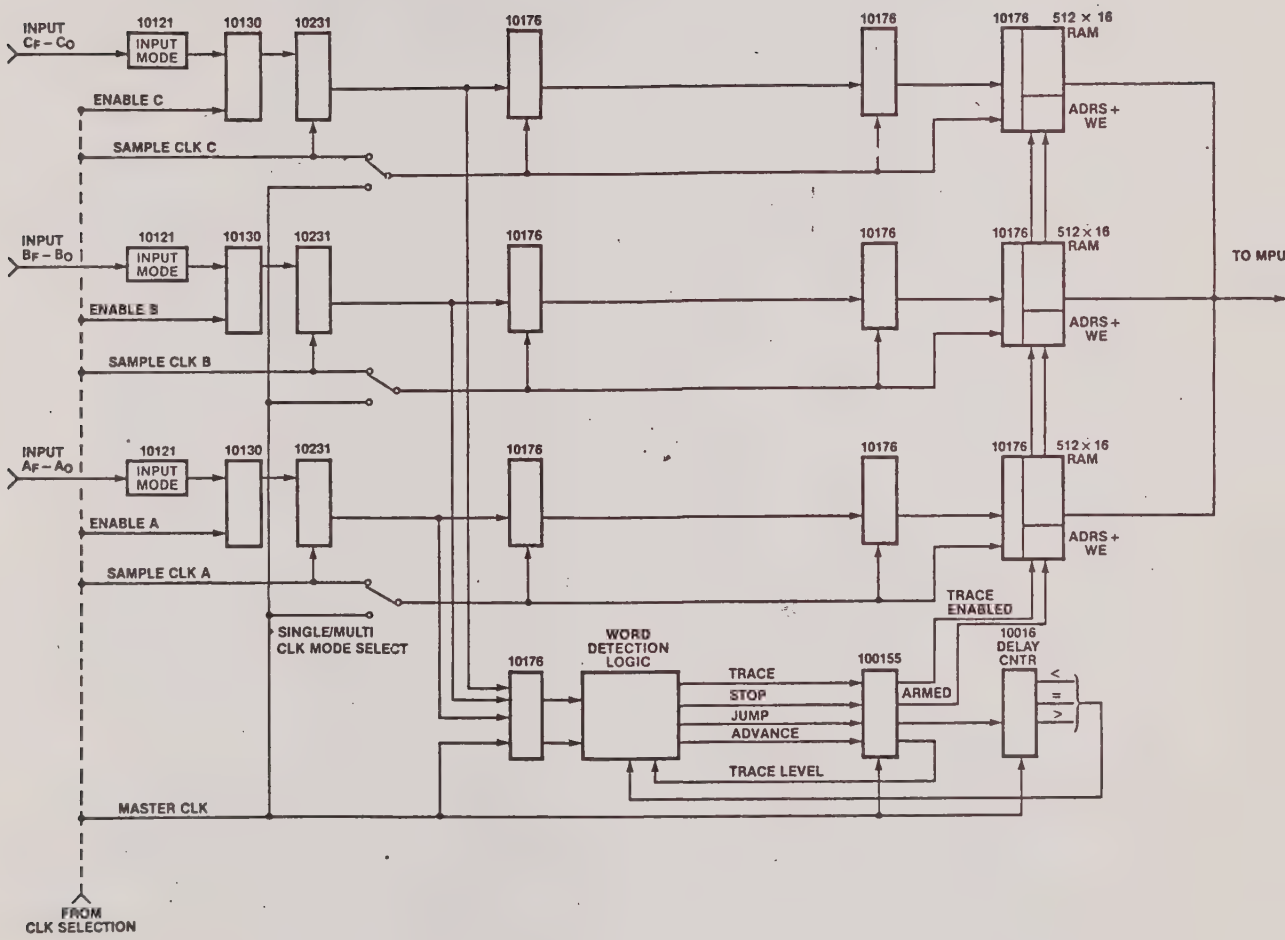
1. 8K, 9M, AND ASSOCIATED CIRCUITS DECODE THE MPU ADDRESS BUS.

2. THE 10124'S AT 6M, 7L, 10L AND 9K ARE TTL TO ECL LEVEL TRANSLATORS FOR THE DATA BUS.

   THESE FEED THE INPUTS OF THE 10176 HEX D LATCHES WHICH HOLD THE CONTROL INFORMATION FROM THE MPU.

3. THE 10173'S AT 12M AND 13M MULTIPLEX THE LOWER 8 BITS OF THE "READ" DATA TO THE MPU.

4. THE 10125'S AT 1M, 2M, 3M, AND 11M ARE TTL TO ECL LEVEL TRANSLATORS.



BLOCK DIAGRAM
HIGH SPEED DATA AQUISITION AND CONTROL LOGIC

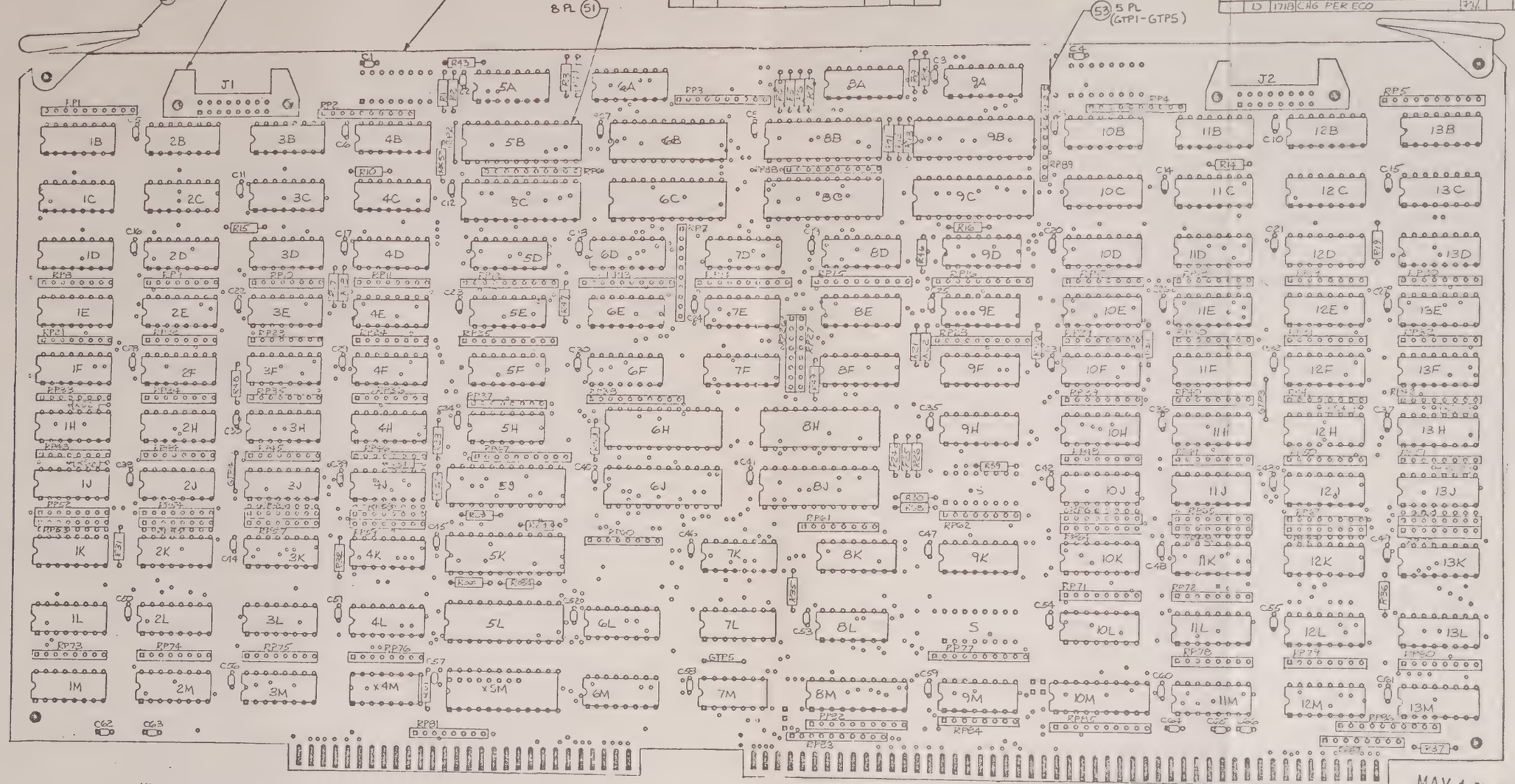
DWG NO 0114-0110 SH 1 REV H

REV	ECO#	DESCRIPTION	DWN	CKD	DATE
H	1823	REVISED PER ECO.	MB		
H	—	PROD REL, ERN #0207	MB		1/31/82

REV	ECO#	DESCRIPTION	DWN	CKD	DATE
E	1818	REVISED PER ECO.	MB		
F	1842	REVISED PER ECO.	MB		
G	1890	REVISED PER ECO.	MB		

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PRE PILOT REL. ERN #0101	KH		
	B		PILOT REL ERN #0130	KH		
	C	1717	CHG PER ECO	KH		
	D	1718	CHG PER ECO	KH		



MAY 17 1982

REFERENCE PRINT

50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

DRAWN 3-12-81

CHECKED

PROJ ENG 1-7-82

MANUFACTURING 1/7/82

GOULD biomation

TITLE ASSY DATA PWB

SCALE 2:1 | SIZE D | PART NUMBER 0114-0110 | REV H

-10 0114-0008 1

COMMENTS		TOTAL COST	UNIT COST
"CER-DIP ONLY" PKGS (FOR 10K ECL DEVICES)			

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0114-0112	PWB				FAB
2												
3												
4						1	1800-0280	I.C.	8L	74S37		
5						2	1800-0240		8M 10M	74LS244		
6						1	1800-0123		7M	74LS14		
7						1	1800-0290	I.C.	9M	74S85		
8												
9												
10						4	1850-0114	I.C.	5A, 6A, 8A, 9A	10016		
11						16	1850-0109		1E-4E, 1F-4F	10106		
12							—		10E-13E, 10F-13F			
13						1	1850-0022		4K	10107		
14						16	1850-0107		1C-4C, 1D-4D	10121		
15							—		10C-13C, 10D-13D			
16						5	1850-0104		8K, 9K, 7L, 10L	10124		
17							—		6M			
18						4	1850-0103	I.C.	1M-3M, 11M	10125		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PRE-PILOT REL PER ERN# 0101				
B	PILOT REL PER ERN# 0130			JL	
C	CHANGE PER ECO 1717	6-2-81			
D	CHANGE PER ECO 1718	6-2-81			
E	REVISED PER ECO# 1818	9-15-81	MS		
F	REVISED PER ECO# 1842	9-15-81	MS		
G	REVISED PER ECO# 1890	9-15-81	MS		

ECO PENDING # [illegible]

DASH NO.	NUMBER	QTY
-10	0114-0002	3

NEXT ASSEMBLY

DRAWN [illegible] DATE 2-13-81
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL

ASSEMBLY, DATA PWB

MODEL K101-D

bionation

B 0114-0110 PF

CODE

SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						8	1850-0102	I.C.	1H-4H, 10H-13H	10130		
20						1	1850-0100	I.C.	7K	10161		
21						6	1850-0105	I.C.	5D, 5E, 9E 12M	10173	CERAMIC ONLY	
22							—		13M, 9D			
23						8	1850-0090	I.C.	1L-4L, 10K, 11L 12L, 13L	10174	CERAMIC ONLY	
24						20	1850-0098	I.C.	6E, 7E, 6D, 7D	10176		
25							—		1K-3K, 11K, 12K,	5F, 7F, 8E,	8F	
26							—		5H, 9F, 6F, 9H, 6L,	8D, 13K		
27						8	1850-0097	I.C.	1J-4J, 10J-13J	10231		
28						8	1850-0094	I.C.	1B-4B, 10B-13B	10216		
29						2	6100-0120	SOCKET 16P	4J, 10J			
30												
31						3	1850-0077	I.C.	8H, 5J, 5K	100101		
32						3	1850-0078	I.C.	6J, 8J, 5L	100102		
33						1	1850-0091	I.C.	6H	100155		
34												
35						8	1850-0088	I.C.	5B, 6B, 8B, 9B	10422		
36									5C, 6C, 8C, 9C			

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	H	REVISED PER ECO #1823	9/5/81	MB		
	H	PROD REL PER ERN #00107	1/29/82	MB		
	J	REVISED PER E.C.O. No 2769	3/14/89	[illegible]	DGW	3/14/89
	K	REVISED PER ECO #3616	3/[illegible]	[illegible]	DGW	3/14/92

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	Burrow	2-13-81
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

ASSEMBLY, DATA PWB

MODEL K101-D

biomation

B	0114-0110	REV
CODE		SHEET 2 OF 3

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						4	3700-0060	RESISTOR PAK	RP1,2,4,5		51Ω, 10 PIN 9 RES	
38												
39						11	3700-0094	RESISTOR PAK	RP7,12-16,25, 28,38,47,86		75Ω, 10 PIN 9 RES	
40												
41						4	3700-0080	RESISTOR PAK	RP88,89,3,6		100Ω, 10 PIN, 9 RES	
42						8	3700-0044	RESISTOR PAK	RP52,54,56,58, 63,65,67,69		220Ω 8 PIN 4 RES	
43						8	3700-0016	RESISTOR PAK	RP53,55,57,59, 64,66,68,70		1KΩ 8 PIN 7 RES	
44						4	3700-0049	RESISTOR PAK	RP77,82,83,85		3K/6.2K 10 PIN	
45						1	3700-0057	RESISTOR PAK	RP84		2.2K 8 PIN 7 RES	
46						49	3700-0047	RESISTOR PAK	RP9-11,17-24,26,27, 29-37,39-46,48-51,		75Ω, 8 PIN, 7 RES	
47							—		60-62,71-76,78-81, 87			
48						58	4010-0103	CAPACITOR	C2,3,5-12,14-61		.01μf 100V	
49						7	4400-0043	CAPACITOR	C1,4,62,63,64,65,66		47μf 6V	
50						2	6000-0374	CONNECTOR	J1, J2	3M	16 PIN HEADER W/EARS	
51						11	6100-0137	SOCKET	X5B, X5C, X6B, X6C,		24 PIN, .4"	
52									X8B, X8C, X9B, X9C, x6J, x6H, x5M			
53						5	9000-0054	BUSS WIRE	GTP1-GTP5		GND	
54						2	7000-0120	EJECTOR				

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN Bnt — DATE 2·13·81
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL

ASSEMBLY, DATA PWB

biomation

B 0114-0110 REV

MODEL K101-D — CODE — SHEET 3 OF 4

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY 60	-50	40	-30	20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55												
56						51	3000-7506	RESISTOR	R1-19, 21-31, 60, 61 33-37, 43-50, 52-56, 58,		75Ω 1/4W 5%	
57												
58												
59						4	3000-5106	RESISTOR	R32, 51, 57, 59		51Ω 1/4W 5%	
60												
61						1	6100-0046	SOCKET	X4M		16 PIN	
62												
63												
64												
65												
66												
67												
68												
69												
70												
71												
72												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN [signature] DATE 9.15.81
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL

ASSEMBLY
DATA PWB

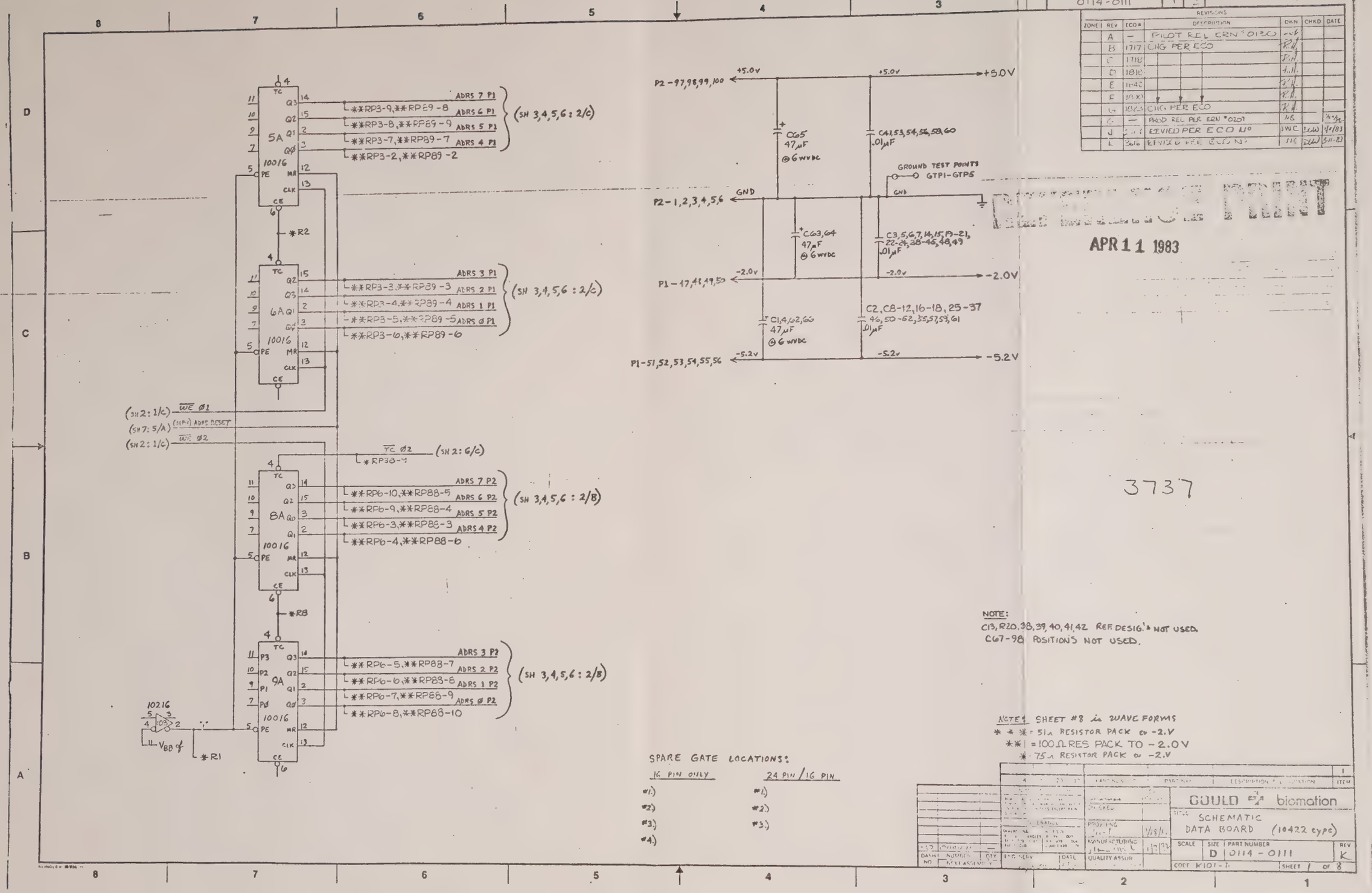
MODEL

biomation

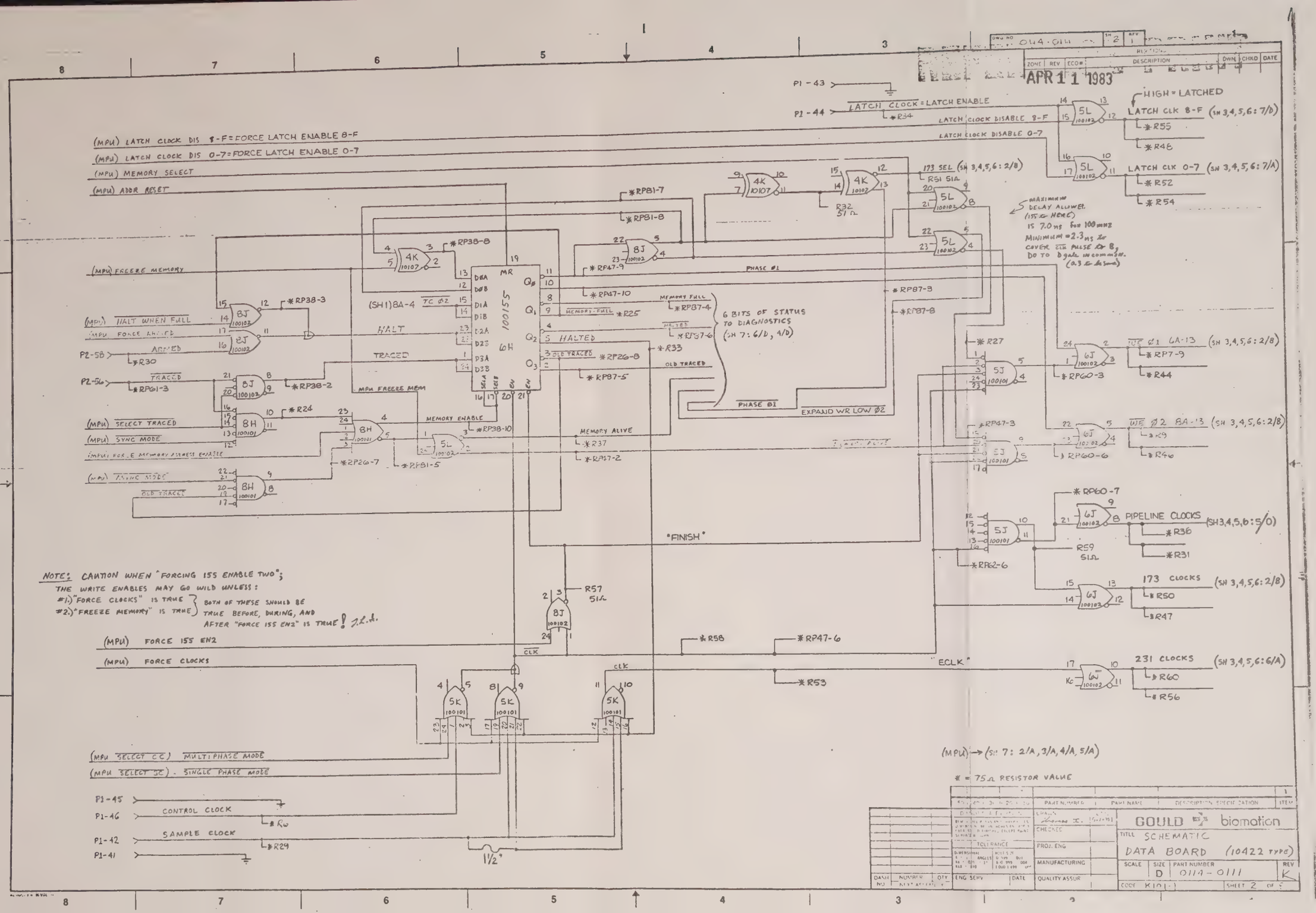
B 0114-0110 REV

CODE

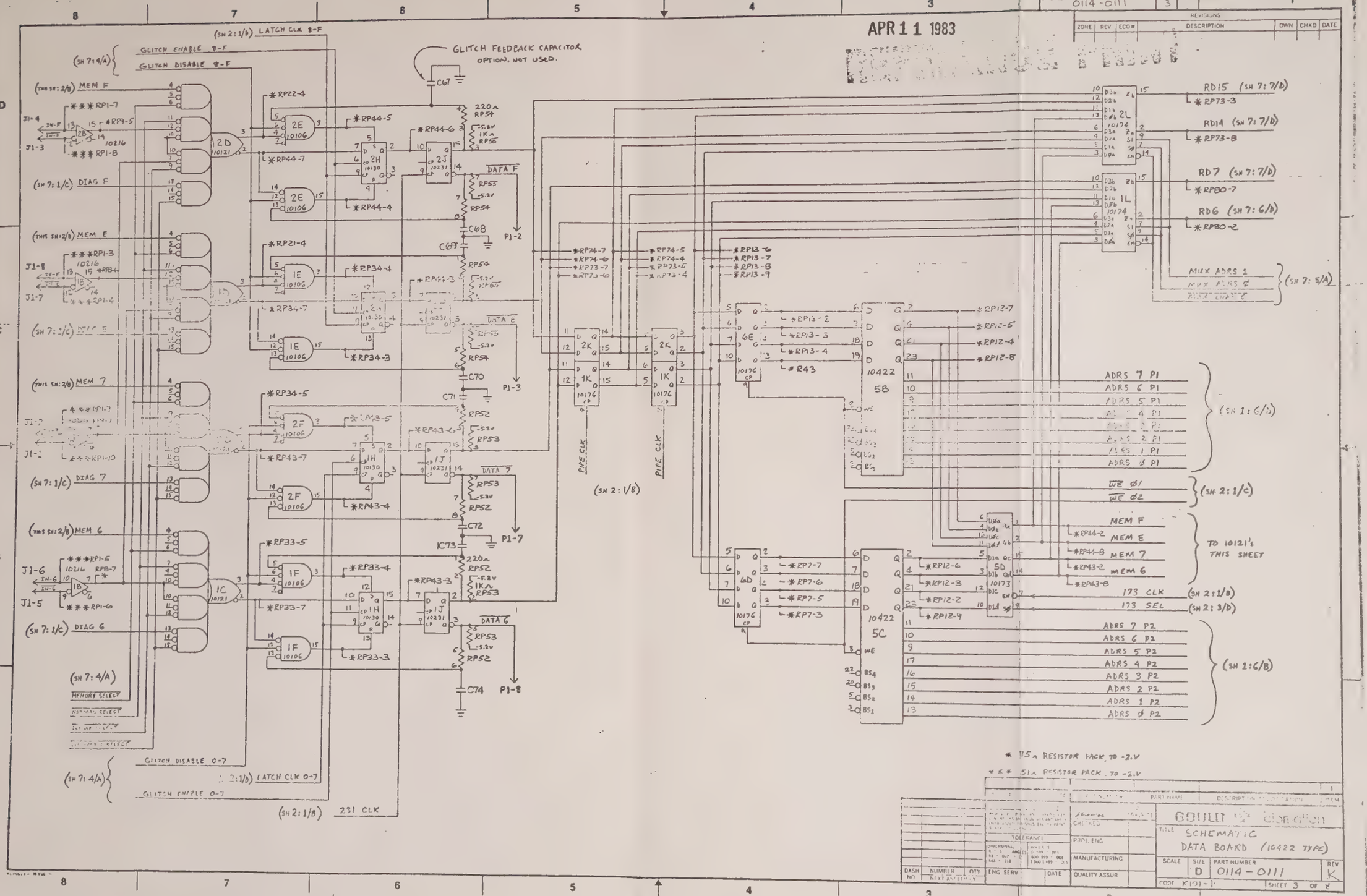
SHEET 4 OF 4



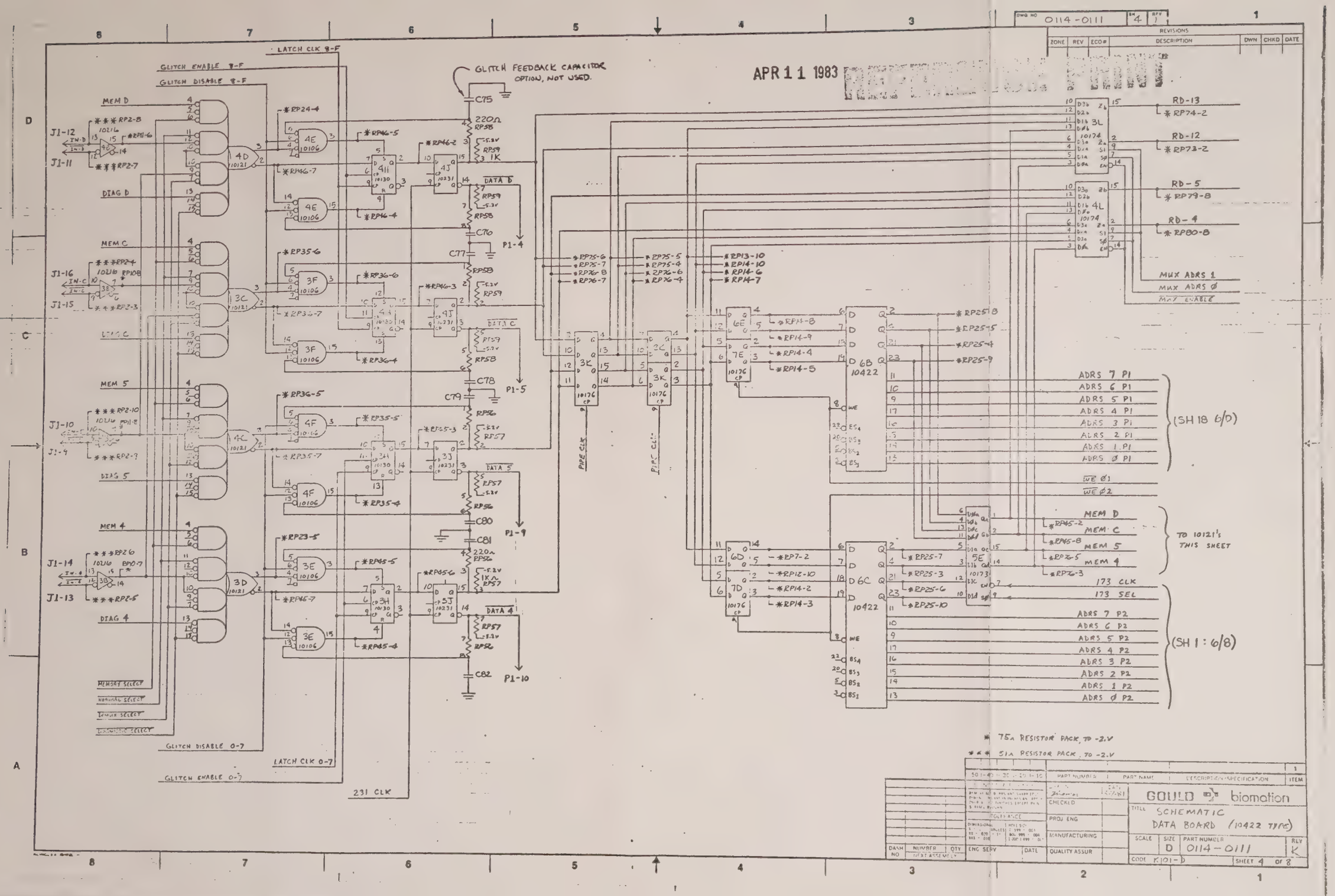
DWG NO 0114-0111
SH 1
REV
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
A | — | PILOT REL ERN #0130
B | 1717 | CHG PER ECO
C | 1718
D | 1810
E | 1840
F | 1830
G | 1823 | CHG PER ECO
G | — | PROD REL PER ERN #0207
J | | REVIED PER ECO NO
K | 3616 | REVISED PER ECO NO
5A 10016
6A 10016
8A 10016
9A 10016
10216
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 3,4,5,6 : 2/C)
(SH 3,4,5,6 : 2/B)
(SH 2 : 1/C) WE Ø1
(SH 7 : 5/A) (MPU) ADRS RESET
(SH 2 : 1/C) WE Ø2
TC Ø2 (SH 2 : 6/C)
*RP38-4
*R2
*R8
*R1
VBB
P2-97,98,99,100
P2-1,2,3,4,5,6
P1-47,48,49,50
P1-51,52,53,54,55,56
+5.0V
-2.0V
-5.2V
GND
C65 47µF @ 6 WVDC
C41,53,54,56,58,60 .01µF
C63,64 47µF @ 6 WVDC
C3,5,6,7,14,15,19-21, 22-24,38-45,48,49 .01µF
C1,4,62,66 47µF @ 6 WVDC
C2,C8-12,16-18,25-37 46,50-52,55,57,59,61 .01µF
GROUND TEST POINTS GTP1-GTP5
APR 11 1983
3737
NOTE:
C13,R20,38,39,40,41,42 REF DESIG.'s NOT USED.
C67-98 POSITIONS NOT USED.
NOTE: SHEET #8 is WAVE FORMS
* * * = 51Ω RESISTOR PACK to -2.V
** = 100Ω RES PACK TO -2.0V
* = 75Ω RESISTOR PACK to -2.V
SPARE GATE LOCATIONS:
16 PIN ONLY
24 PIN / 16 PIN
#1.)
#2.)
#3.)
#4.)
GOULD biomation
SCHEMATIC
DATA BOARD (10422 type)
SCALE
SIZE D
PART NUMBER 0114-0111
REV K
CODE K101-1
SHEET 1 OF 8



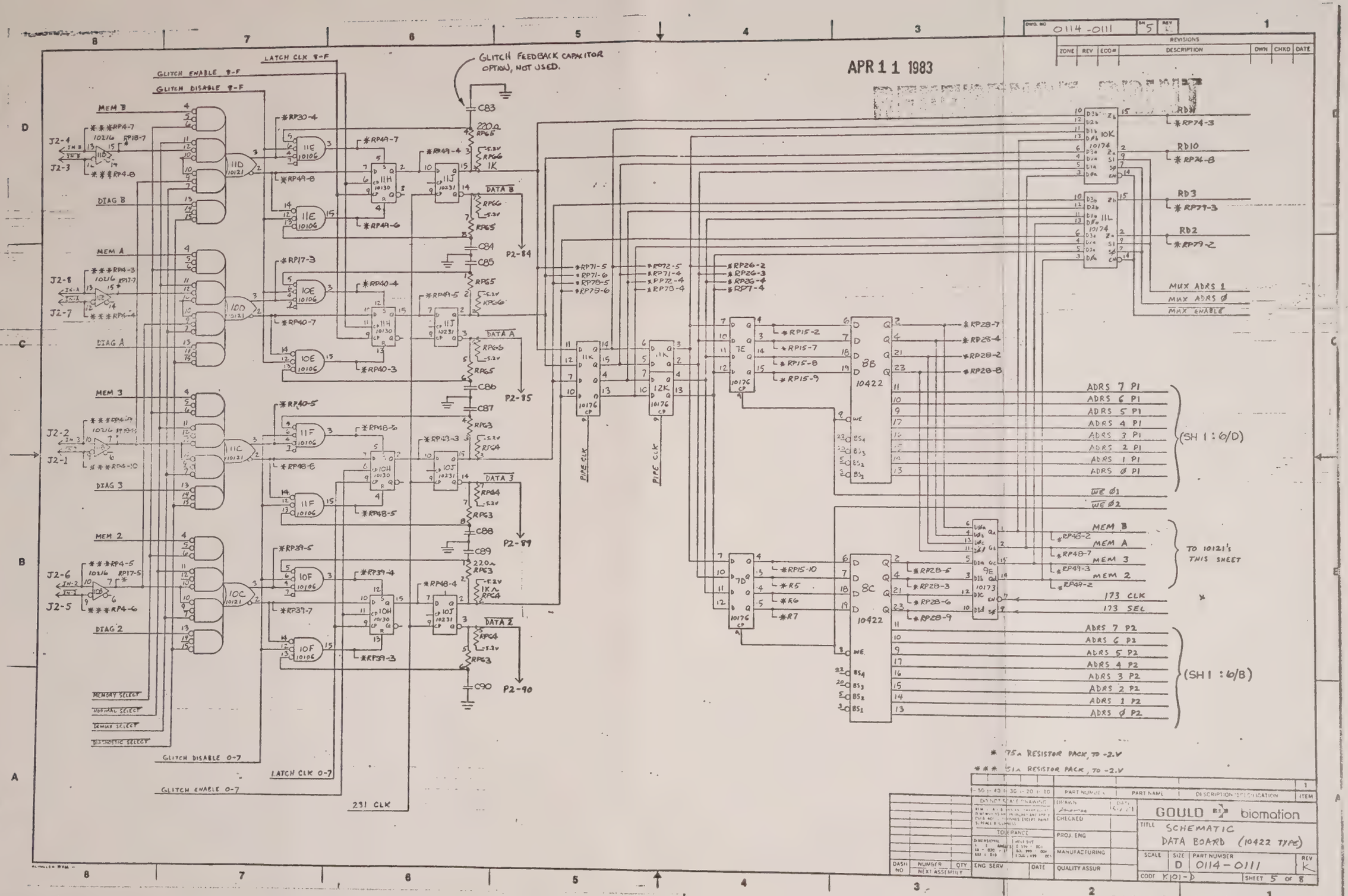
APR 11 1983
P1-43
P1-44
LATCH CLOCK = LATCH ENABLE
LATCH CLOCK DISABLE 8-F
LATCH CLOCK DISABLE 0-7
HIGH = LATCHED
LATCH CLK 8-F (SH 3,4,5,6: 7/D)
LATCH CLK 0-7 (SH 3,4,5,6: 7/A)
(MPU) LATCH CLOCK DIS 8-F = FORCE LATCH ENABLE 8-F
(MPU) LATCH CLOCK DIS 0-7 = FORCE LATCH ENABLE 0-7
(MPU) MEMORY SELECT
(MPU) ADDR RESET
173 SEL (SH 3,4,5,6: 2/B)
MAXIMUM DELAY ALLOWED (155 to HERE) IS 7.0 ns for 100 MHz MINIMUM = 2.3 ns to COVER CLK PULSE to B, DO TO D gate in common. (0.3 to be sure)
(MPU) FREEZE MEMORY
(MPU) HALT WHEN FULL
(MPU) FORCE ARMED
P2-58
P2-56
ARMED
TRACED
(SH1) 8A-4
TC Ø2
HALT
TRACED
MPU FREEZE MEM
MEMORY FULL
HALTED
OLD TRACED
6 BITS OF STATUS TO DIAGNOSTICS (SH 7: 6/D, 4/D)
PHASE Ø1
EXPAND WR LOW Ø2
WE Ø1 6A-13 (SH 3,4,5,6: 2/B)
WE Ø2 8A-13 (SH 3,4,5,6: 2/B)
(MPU) SELECT TRACED
(MPU) SYNC MODE
(MPU) FORCE MEMORY ADDRESS ENABLE
(MPU) ASYNC MODE
OLD TRACED
MEMORY ENABLE
MEMORY ALIVE
"FINISH"
PIPELINE CLOCKS (SH 3,4,5,6: 5/D)
173 CLOCKS (SH 3,4,5,6: 2/B)
231 CLOCKS (SH 3,4,5,6: 6/A)
"ECLK"
NOTE: CAUTION WHEN "FORCING 155 ENABLE TWO";
THE WRITE ENABLES MAY GO WILD UNLESS:
#1.) "FORCE CLOCKS" IS TRUE
#2.) "FREEZE MEMORY" IS TRUE
BOTH OF THESE SHOULD BE TRUE BEFORE, DURING, AND AFTER "FORCE 155 EN2" IS TRUE!
(MPU) FORCE 155 EN2
(MPU) FORCE CLOCKS
(MPU SELECT CC) MULTIPHASE MODE
(MPU SELECT SC) SINGLE PHASE MODE
P1-45
P1-46
CONTROL CLOCK
P1-42
P1-41
SAMPLE CLOCK
1½"
(MPU) → (SH 7: 2/A, 3/A, 4/A, 5/A)
* = 75Ω RESISTOR VALUE
GOULD biomation
TITLE SCHEMATIC
DATA BOARD (10422 TYPE)
SCALE
SIZE D
PART NUMBER 0114-0111
REV K
SHEET 2

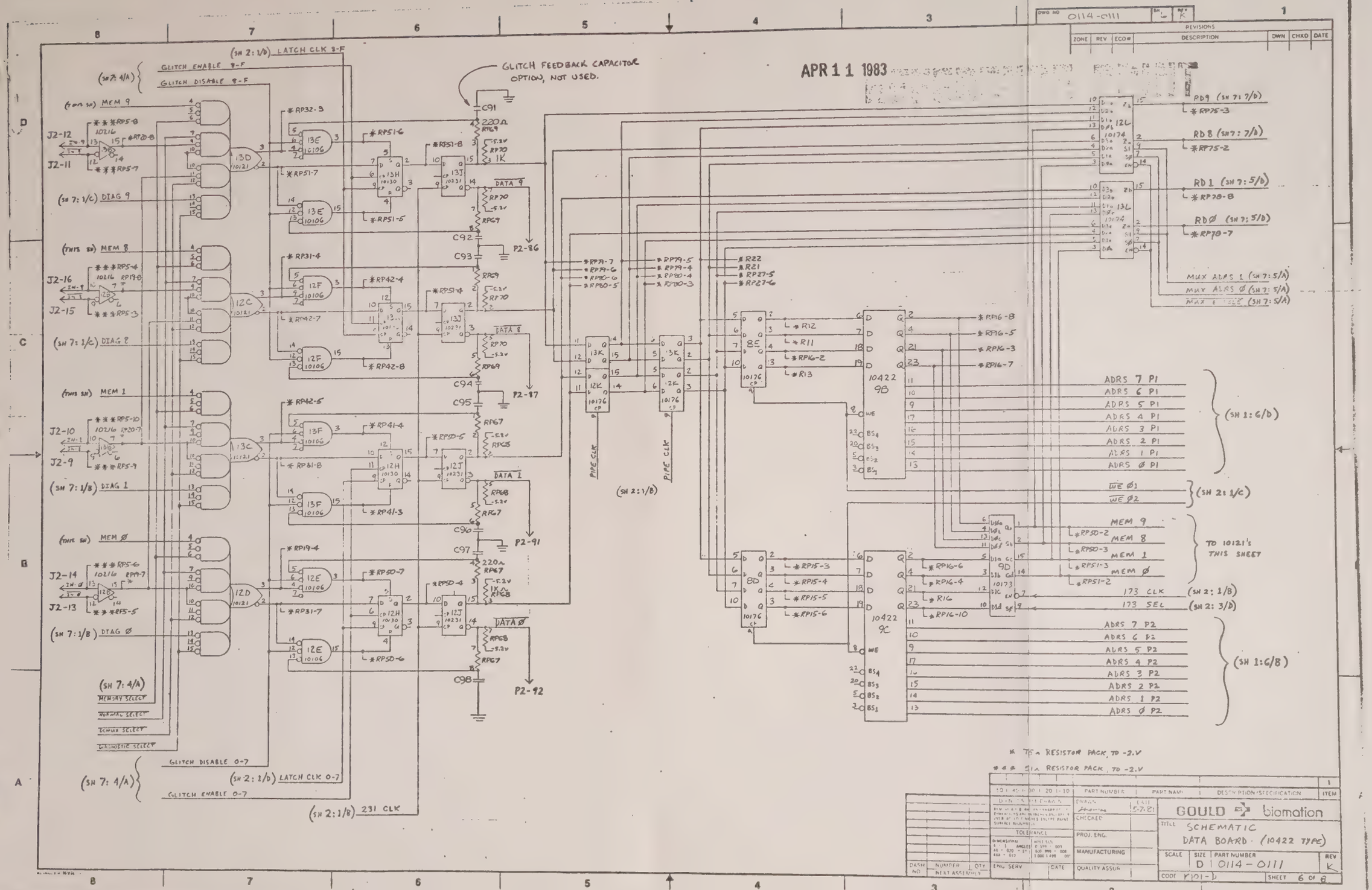


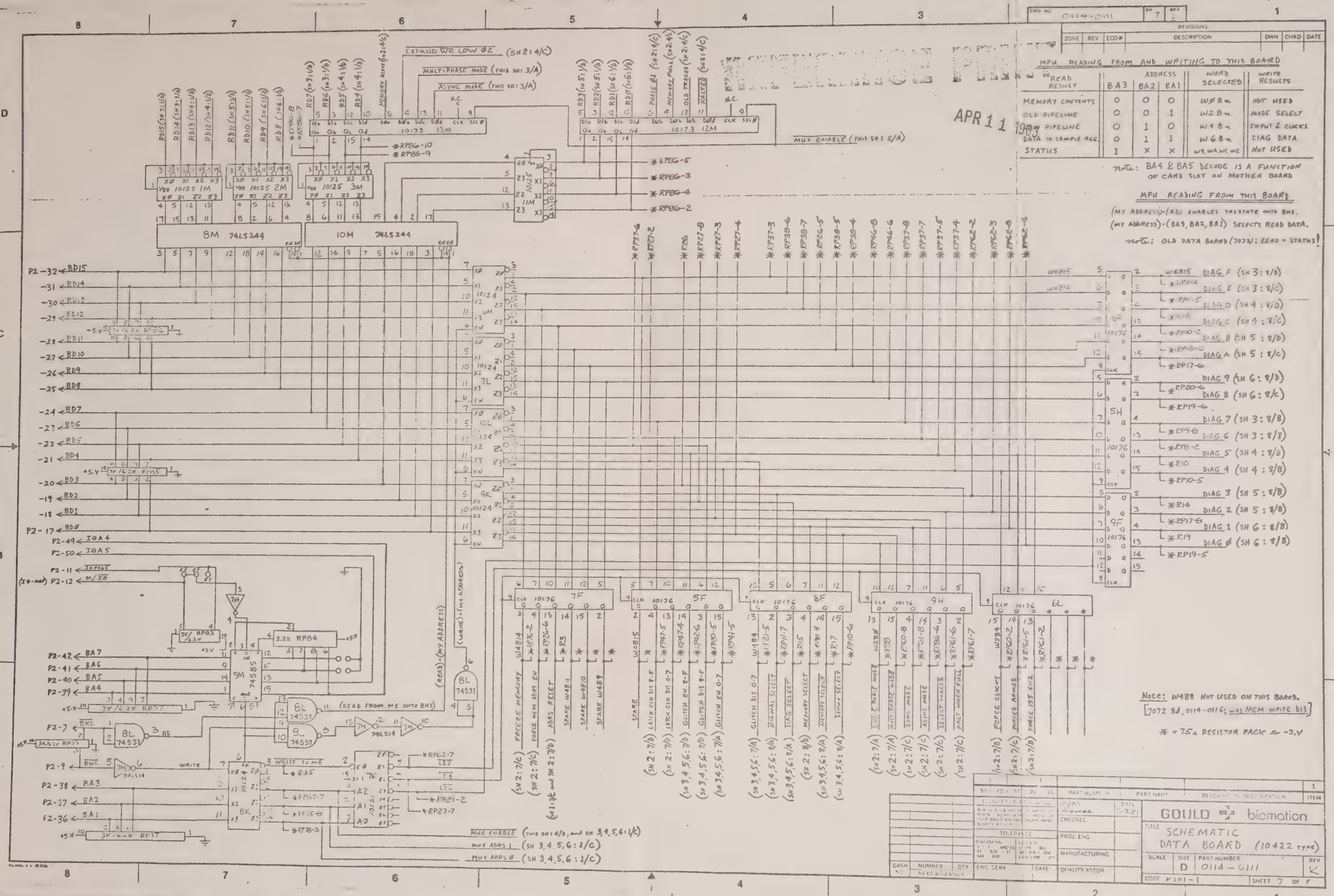
APR 11 1983
DWG NO 0114-0111
SH 3
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
(SH 2:1/D) LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
(SH 7:4/A)
(THIS SH:2/B) MEM F
(SH 7:1/C) DIAG F
(THIS SH:2/B) MEM E
(SH 7:1/C) DIAG E
(THIS SH:2/B) MEM 7
(SH 7:1/C) DIAG 7
(THIS SH:2/B) MEM 6
(SH 7:1/C) DIAG 6
(SH 7:4/A)
MEMORY SELECT
NORMAL SELECT
GLITCH DISABLE 0-7
(SH 2:1/D) LATCH CLK 0-7
GLITCH ENABLE 0-7
(SH 2:1/B) 231 CLK
DATA F
DATA E
DATA 7
DATA 6
P1-2
P1-3
P1-7
P1-8
PIPE CLK
(SH 2:1/B)
RD15 (SH 7:7/D)
RD14 (SH 7:7/D)
RD7 (SH 7:7/D)
RD6 (SH 7:6/D)
MUX ADRS 1
MUX ADRS Ø
(SH 7:5/A)
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
(SH 1:6/D)
WE Ø1
WE Ø2
(SH 2:1/C)
MEM F
MEM E
MEM 7
MEM 6
TO 10121's THIS SHEET
173 CLK (SH 2:1/B)
173 SEL (SH 2:3/D)
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1:6/B)
* 115Ω RESISTOR PACK, TO -2.V
** 51Ω RESISTOR PACK, TO -2.V
GOULD Corporation
TITLE SCHEMATIC DATA BOARD (10422 TYPE)
SCALE SIZE D PART NUMBER 0114-0111 REV K
CODE K101-1 SHEET 3 OF 8



DWG NO 0114-0111
SH 4
REV 1
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
APR 11 1983
LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
MEM D
DIAG D
MEM C
DIAG C
MEM 5
DIAG 5
MEM 4
DIAG 4
MEMORY SELECT
NORMAL SELECT
DEMUX SELECT
GLITCH DISABLE 0-7
LATCH CLK 0-7
GLITCH ENABLE 0-7
231 CLK
DATA D
DATA C
DATA 5
DATA 4
PIPE CLK
RD-13
RD-12
RD-5
RD-4
MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
(SH 18 6/D)
WE Ø1
WE Ø2
MEM D
MEM C
MEM 5
MEM 4
TO 10121's THIS SHEET
173 CLK
173 SEL
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1 : 6/8)
* 75Ω RESISTOR PACK, TO -2.V
*** 51Ω RESISTOR PACK, TO -2.V
GOULD biomation
TITLE SCHEMATIC DATA BOARD (10422 TYPE)
SCALE
SIZE D
PART NUMBER 0114-0111
REV K
CODE K101-D
SHEET 4 OF 8


DWG. NO 0114-0111
SH 5
REV K
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
APR 1 1 1983
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
MEM B
DIAG B
MEM A
DIAG A
MEM 3
DIAG 3
MEM 2
DIAG 2
J2-4
J2-3
J2-8
J2-7
J2-2
J2-1
J2-6
J2-5
DATA B
DATA A
DATA 3
DATA 2
P2-84
P2-85
P2-89
P2-90
PIPE CLK
RD11
RD10
RD3
RD2
MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
WE Ø1
WE Ø2
(SH 1 : 6/D)
MEM B
MEM A
MEM 3
MEM 2
173 CLK
173 SEL
TO 10121's THIS SHEET
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1 : 6/B)
MEMORY SELECT
NORMAL SELECT
TEMUX SELECT
DIAGNOSTIC SELECT
GLITCH DISABLE 0-7
GLITCH ENABLE 0-7
LATCH CLK 0-7
231 CLK
* 75Ω RESISTOR PACK, TO -2.V
*** 51Ω RESISTOR PACK, TO -2.V
GOULD biomation
TITLE SCHEMATIC DATA BOARD (10422 TYPE)
SCALE
SIZE D
PART NUMBER 0114-0111
REV K
CODE K101-D
SHEET 5 OF 8
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION
ITEM


APR 1 1 1983
DWG NO 0114-0111
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
(SH 2: 1/D) LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
(SH 7: 4/A)
MEM 9
DIAG 9
MEM 8
DIAG 8
MEM 1
DIAG 1
MEM Ø
DIAG Ø
J2-12
J2-11
J2-16
J2-15
J2-10
J2-9
J2-14
J2-13
10216
13D 10121
12C 10121
13C 10121
12D 10121
13E 10106
12F 10106
13F 10106
12E 10106
13H 10130
13J 10231
12H 10130
12J 10231
DATA 9
DATA 8
DATA 1
DATA Ø
P2-86
P2-87
P2-91
P2-92
C91
C92
C93
C94
C95
C96
C97
C98
220Ω RP69
RP70 1K
RP67
RP68 1K
PIPE CLK
(SH 2: 1/B)
13K
12K
12L
13L
10174
8E
8D
9D
10176
10422 9B
10422 9C
10173
RD9 (SH 7: 7/D)
RD8 (SH 7: 7/B)
RD1 (SH 7: 5/D)
RDØ (SH 7: 5/D)
MUX ADRS 1 (SH 7: 5/A)
MUX ADRS Ø (SH 7: 5/A)
MUX ENABLE (SH 7: 5/A)
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
(SH 1: 6/D)
WE Ø1
WE Ø2
(SH 2: 1/C)
MEM 9
MEM 8
MEM 1
MEM Ø
TO 10121'S THIS SHEET
173 CLK (SH 2: 1/B)
173 SEL (SH 2: 3/D)
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1: 6/B)
(SH 7: 4/A)
MEMORY SELECT
NORMAL SELECT
TEMUX SELECT
DIAGNOSTIC SELECT
GLITCH DISABLE 0-7
GLITCH ENABLE 0-7
(SH 2: 1/D) LATCH CLK 0-7
(SH 2: 1/B) 231 CLK
* 75Ω RESISTOR PACK, TO -2.V
*** 51Ω RESISTOR PACK, TO -2.V
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
GOULD biomation
TITLE SCHEMATIC
DATA BOARD (10422 TYPE)
SCALE SIZE PART NUMBER REV
D 0114-0111 K
CODE K101-1 SHEET 6 OF 8
DASH NO NUMBER QTY
NEXT ASSEMBLY
ENG SERV DATE
TOLERANCE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR

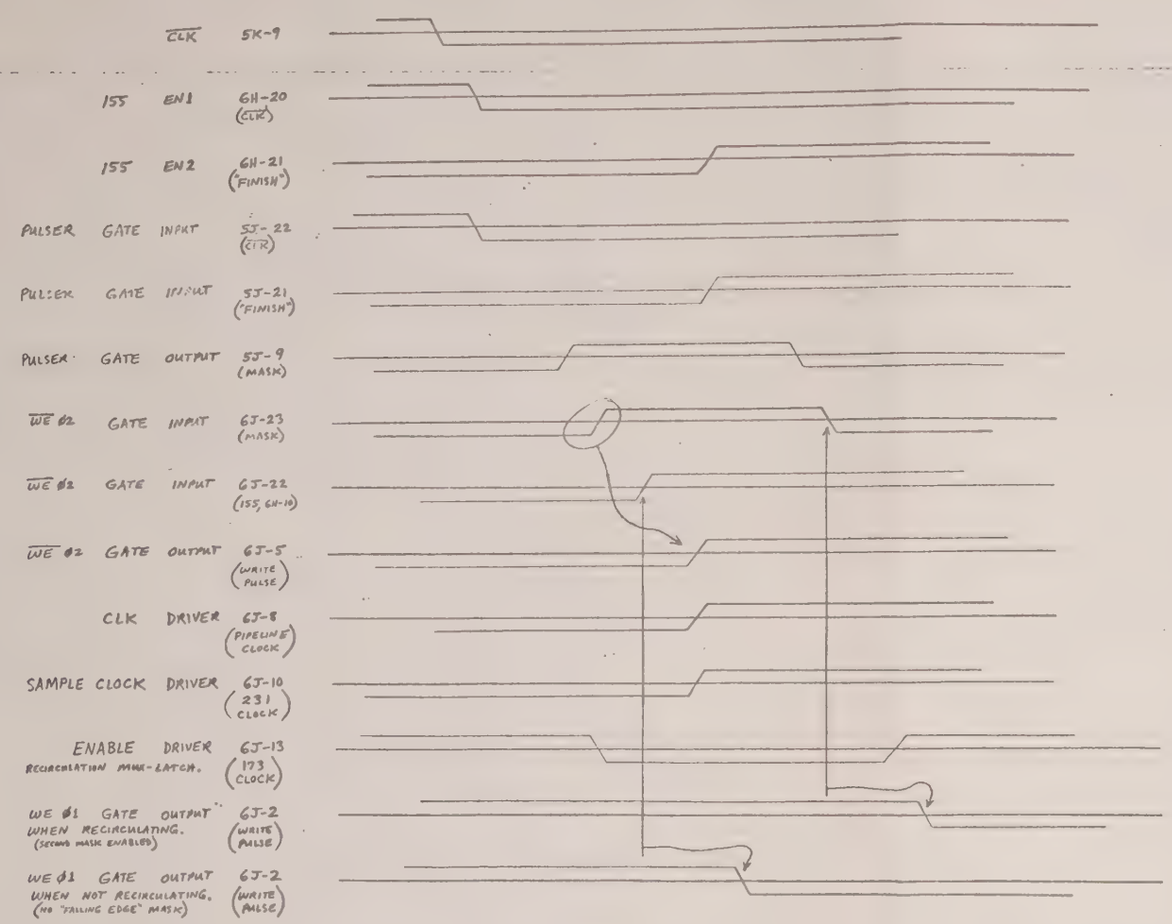

DWG NO 0114-0111
SH 7
REV K
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
MPU READING FROM AND WRITING TO THIS BOARD
READ RESULT | ADDRESS BA3 BA2 BA1 | WORD SELECTED | WRITE RESULTS
MEMORY CONTENTS 0 0 0 W0 B→ NOT USED
OLD PIPELINE 0 0 1 W2 B→ MODE SELECT
NEW PIPELINE 0 1 0 W4 B→ INPUT & CLOCKS
DATA IN SAMPLE REG 0 1 1 W6 B→ DIAG DATA
STATUS 1 X X W8, WA, WC, WE NOT USED
note: BA4 & BA5 DECODE IS A FUNCTION OF CARD SLOT ON MOTHER BOARD
MPU READING FROM THIS BOARD
(MY ADDRESS)·(RD) ENABLES TRISTATE ONTO BUS.
(MY ADDRESS)·(BA3, BA2, BA1) SELECTS READ DATA.
note: OLD DATA BOARD (7072): ZERO = STATUS!
APR 11 1983
EXPAND WR LOW ØZ (SH 2:4/C)
MULTIPHASE MODE (THIS SH: 3/A)
ASYNC MODE (THIS SH: 3/A)
MUX ENABLE (THIS SH: 5/A)
8M 74LS244
10M 74LS244
1M 10125
2M 10125
3M 10125
11M 10125
12M 10173
13M 10173
7L 10124
10L 10124
9K 10124
5H 10176
9F 10176
7F 10176
5F 10176
8F 10176
9H 10176
6L 10176
9M 74S85
8L 74S37
9L 74S37
8K 10124
7H 74LS14
2.2K RP84
3K/6.2K RP77
3K/6.2K RP85
3K/6.2K RP83
3K/6.2K RP82
3K/6.2K RP78
Note: W4B8 NOT USED ON THIS BOARD.
[7072 Bd, 0114-0116; was MEM WRITE DIS]
* = 75Ω RESISTOR PACK to -2.V
MUX ENABLE (THIS SH: 4/D, and SH 3,4,5,6: 1/C)
MUX ADRS 1 (SH 3,4,5,6: 2/C)
MUX ADRS Ø (SH 3,4,5,6: 1/C)
GOULD biomation
SCHEMATIC
DATA BOARD (10422 type)
SIZE D
PART NUMBER 0114-0111
REV K
CODE K101-1
SHEET 7 OF 7

DWG NO 0114-0111 SH 3 REV K

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DATA BOARD WAVEFORMS



REPLACED PRINT

APR 11 1983

DASH NO	NUMBER	QTY	ENG SERV	DATE
	NEXT ASSEMBLY			

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DRAWN [signature] DATE 5-7-81
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC DATA BOARD

SCALE | SIZE D | PART NUMBER 0114-0111 | REV K

CODE K101-D | SHEET 8 OF 8

CONTROL BOARD
THEORY OF OPERATION

REFERENCE SCHEMATIC # 0114-0121

THE CONTROL BOARD CONTAINS ALL DECISION-MAKING LOGIC FOR CONTROL OF THE RECORDING PROCESS. THIS INCLUDES WORD RECOGNITION CIRCUITS, DELAY COUNTERS, AND THE LOGIC TO COMBINE DELAY CONDITIONS WITH DETECTED WORDS TO CAUSE THE UNIT TO STOP RECORDING, JUMP OR ADVANCE TO ANOTHER LEVEL WITH DIFFERENT RECORD PARAMETERS AND SELECTIVELY RECORD OR NOT RECORD THE INPUT DATA.

A. WORD RECOGNITION CIRCUITS ARE SHOWN ON SHEETS 1, 2, AND 3 OF THE SCHEMATIC.

   1. WORD RECOGNITION IS ACCOMPLISHED SEPARATELY FOR SECTIONS A, B, AND C WITH THE SEPARATE WORDS BEING COMBINED IN THE WORD SELECTION CIRCUITS WHICH WILL BE DISCUSSED LATER.

   2. THE SECTION C CIRCUIT, FOUND ON SHEET 3, WILL BE USED HERE AS AN EXAMPLE. SECTIONS A AND B ARE IDENTICAL TO SECTION C.

B. WORD RECOGNITION CIRCUIT OPERATION:

   1. $\overline{\text{DATA}}$ FROM THE $\overline{Q}$ OUTPUTS OF THE SAMPLE REGISTERS ON THE C DATA BOARD ENTERS THE CONTROL BOARD VIA THE MOTHER BOARD AND IS SYNCHRONIZED WITH THE CONTROL CLOCK IN THE 10176 REGISTERS AT LOCATIONS 1H, 2H, AND 3H.

   2. THE DATA OUT OF THE REGISTERS IS PRESENTED TO 4 OF THE 8 ADDRESS INPUTS AND TO EACH OF 4 10422 256 X 4 STATIC RAMS.

   3. THE OTHER 4 ADDRESS LINES OF THE 10422'S ARE DRIVEN WITH "LEVEL", A 4-BIT NUMBER REPRESENTING THE LEVEL OF TRACE CONTROL.

4. THE 4 DATA OUTPUTS OF THE 10422'S CORRESPOND TO THE 4 COMBINATIONAL FUNCTIONS OF THE K101, "S", "J", "A", AND "T".

5. THE MPU INITIALIZES THE RAM'S TO HAVE ZERO'S ONLY AT THOSE ADDRESS LOCATIONS AND BIT POSITIONS THAT CORRESPOND TO THE COMBINATIONS SELECTED BY THE OPERATOR FOR "S", "J", "A", AND "T" AT EACH LEVEL.

6. THUS; THE RAMS ACT AS PROGRAMMABLE LOGIC ARRAYS WHICH RESPOND TO DIFFERENT "S", "J", "A", AND "T" COMBINATIONS AT EACH OF 16 LEVELS FOR A TOTAL OF 48 COMBINATIONS.

7. THE 100101 OR GATE AT 3D COMBINES THE OUTPUTS FROM 4 RAM'S INTO THE SIGNALS "STOP C", "JUMP C", "ADVANCE C" AND "TRACE C".

8. THE 10176 AT 2J IS A HOLDING REGISTER FOR MPU CONTROL SIGNALS USED DURING INITIALIZATION.

9. THE 10164 AT 4C IS A MULTIPLEXER WHICH GIVES THE MPU ACCESS TO THE SECTION OUTPUTS FOR DIAGNOSTIC PURPOSES.

C. <u>WORD SELECTION CIRCUITS</u> ARE FOUND ON SHEET 4 AND 5 OF THE SCHEMATIC. THE "<u>STOP A, B, & C</u>", "<u>JUMP A, B, & C</u>", "<u>ADVANCE A, B, & C</u>", AND "<u>TRACE A, B, & C</u> SIGNALS ARE COMBINED WITH THE DELAY CONDITION SIGNALS "$\overline{T<D}$", "$\overline{T=D}$", AND "$\overline{T>D}$" IN THESE CIRCUITS.

FOR PURPOSE OF THIS DISCUSSION, ONLY THE "ADVANCE" SELECT CIRCUIT WILL BE CONSIDERED. THE "STOP", "JUMP" AND "TRACE" CIRCUITS OPERATE IN ESSENTIALLY THE SAME MANNER AS "ADVANCE".

1. THE SIGNALS "ADVANCE A, B, AND C" AND THEIR COMPLEMENTS ALONG WITH THE DELAY CONDITION SIGNALS "$\overline{T<D}$", "$\overline{T=D}$", AND "$\overline{T>D}$" ARE PRESENTED TO THE INPUTS OF THE 100102'S AT 5C AND 5D.

2. EACH OF THE GATES IN 5D AND 5C IS ALSO FED WITH ONE OF THE OUTPUTS OF 4B, 5B, AND 6B, 10145A HIGH SPEED 4 X 16 RAM'S.

3. THE OUTPUTS OF 5C AND 5D ARE NOR'ED TOGETHER IN THE 100101 AT 5F, WHOSE INPUTS MUST BE LOW FOR "ADVANCE" TO GO HIGH.

4. "ADVANCE" WILL BE LOW IF ANY OF THE GATES OF 5C OR 5D HAVE LOWS ON ALL THREE INPUTS.

5. PIN 19 OF 5C AND 5D IS UNIVERSAL TO ALL GATES AND IS LOW AT ALL TIMES EXCEPT DURING DIAGNOSTIC TESTS OR ARM INITIALIZATION WHEN THE MPU CAN PULL IT HIGH TO "FORCE $\overline{\text{ADVANCE}}$".

<u>EXAMPLE OPERATION</u>:

** ASSUME THE OPERATOR HAS SELECTED "ADVANCE IF DATA = A AND T = D".

** FOR THIS SELECTION, THE MPU WOULD INITIALIZE THE 10145'S TO PLACE LOWS ON 5C-1, 17, AND 21 AND 5D-17 AND 24 AT THE APPROPRIATE "LEVEL".

** THE CONTROLLING INPUTS TO THESE GATES BECOME "ADVANCE B", "$\overline{T<D}$", "$\overline{T>D}$", "ADVANCE C", AND "ADVANCE A".

** IF ANY ONE OF THESE SIGNALS IS LOW — INDICATING THAT THE SELECTED EQUATION IS FALSE — THE OUTPUT OF THE GATE IT CONTROLS WILL BE HIGH, CAUSING "$\overline{\text{ADVANCE}}$" TO BE TRUE AND "ADVANCE" TO BE FALSE.

6. THE ADDRESS INPUTS TO THE 10145A'S IS THE 4-BIT "LEVEL" NUMBER. THUS IT IS POSSIBLE TO SELECT A DIFFERENT "ADVANCE" EQUATION FOR EACH OF THE 16 LEVELS OF TRACE.

7. THE INPUTS TO THE 100101 AT 7D PARALLEL THE INPUTS TO 5F THAT ARE CONTROLLED BY THE WORD RECOGNITION LOGIC, DISREGARDING THE DELAY CONDITIONS.

8. THE OUTPUTS OF 7D ARE CALLED "EVENT" AND "$\overline{\text{EVENT}}$". THESE SIGNALS ARE USED TO CONTROL THE DELAY COUNTER IN EVENTS DELAY MODE.

9. THE 10176 REGISTERS AT 6A AND 7A ARE USED TO HOLD MPU CONTROL SIGNALS WHICH CAN FORCE "STOP", "$\overline{\text{STOP}}$", "JUMP", "$\overline{\text{JUMP}}$", "ADVANCE", "$\overline{\text{ADVANCE}}$", "TRACE", "$\overline{\text{TRACE}}$", "EVENT" AND "$\overline{\text{EVENT}}$" TO A DESIRED LOGICAL STATE, OVERIDING THE NORMAL INPUT CONDITIONS.

10. THESE ARE USED DURING THE DIAGNOSTIC CHECKS AND THE ARM INITIALIZATION SEQUENCE.

11. 6A ALSO ENABLES THE 10231 AT 5A TO "FORCE ADVANCE" FOR ONE CLOCK PERIOD.

    THIS IS USED FOR MANUAL ADVANCE AND TO BEGIN THE "ARMED" CYCLE WHEN THE UNIT ADVANCES OUT OF LEVEL F INTO LEVEL 0 ON THE FIRST CONTROL CLOCK.

D. THE LEVEL SWITCHING CIRCUIT IS FOUND ON SHEET 6 OF THE SCHEMATIC'S.

1. THE 100155 AT LOCATION 5G IS A QUAD MULTIPLEX LATCH.

   THE TWO SETS OF INPUTS TO THE LATCH COME FROM 10145A RAM'S AT LOCATIONS 5H AND 5J.

2. THE ADDRESS INPUT TO 5H AND 5J IS THE 4-BIT NUMBER "LEVEL".

3. 5H AND 5J ARE INITIALIZED BY THE MPU SO THAT AT ANY GIVEN LEVEL ADDRESS, 5H CONTAINS THE NUMBER OF THE NEXT SEQUENTIAL LEVEL AND 5J CONTAINS THE NUMBER OF THE USER SELECTED "JUMP-TO" LEVEL.

4. THE 100155 HAS TWO ENABLE INPUTS, BOTH OF WHICH MUST BE LOW FOR THE SELECTED INPUT TO BE TRANSFERRED TO THE OUPUTS AS THE NEXT "LEVEL".

- ONE OF THE ENABLES IS DRIVEN WITH THE CONTROL SIGNAL "$\overline{\text{JUMP OR ADVANCE}}$", ALLOWING THE LEVEL TO CHANGE ONLY WHEN A "JUMP" OR "ADVANCE" CONDITION IS DETECTED.

  THE SECOND ENABLE IS A 3 NSEC PULSE DERIVED FROM THE CONTROL (MASTER) CLOCK.

5. THE NEW LEVEL THEN BECOMES THE NEW ADDRESS FOR THE LEVEL RAMS 5H AND 5J.

6. THE PROPOGATION DELAYS AROUND THE LOOPS ARE THAT MUCH GREATER THAN THE 3 NSEC LATCH ENABLE THAT GLITCH-FREE OPERATION OCCURS.

7. "$\overline{\text{JUMP}}$" ON 5G PINS 16 AND 17 SELECTS WHICH SET OF INPUTS WILL BE LATCHED, THUS THE DECISION WHETHER TO JUMP OR ADVANCE GIVES PRIORITY TO JUMPING, EVEN IF THE "ADVANCE" CONDITION IS TRUE AT THE SAME TIME.

E. THE <u>DELAY COUNTER</u> CIRCUIT IS LOCATED ON <u>SHEET 8</u> OF THE SCHEMATICS.

1. THE 10016'S AT 13-C AND 13-E FORM A SIMPLE PROGRAMMABLE SYNCHRONOUS COUNTER.

2. THE 10145A RAMS AT 14-C AND 14-F ARE ADDRESSED BY "LEVEL".

   EACH ADDRESS IS INITIALIZED BY THE MPU WITH THE 2's COMPLEMENT PLUS 1 OF THE DELAY NUMBER FOR THE CORRESPONDING "LEVEL".

3. THE COUNTER CANNOT COUNT A DELAY SHORTER THAN 2.

FOLLOWING IS AN EXAMPLE OF CIRCUIT OPERATION WHEN THE COUNTER IS LOADED FOR THE SHORTEST POSSIBLE DELAY:

******* COUNTER LOADED TO FFFF (HEX)

******* THE COUNTER IS LOADED BY THE FIRST CLOCK AFTER ENTERING A NEW LEVEL.

******* THEREFORE, FOR "DELAY TC" TO BECOME TRUE REQUIRES 2 CLOCKS; ONE TO ENTER THE NEW LEVEL AND ONE TO LOAD THE DELAY COUNTER.

4. NOTE THAT THE OUTPUTS OF THE COUNTERS GO TO THE MULTIPLEXERS AT 12D AND 12E FOR MPU DIAGNOSTIC ACCESS.

F. THE RECORD CONTROL CIRCUITS ARE FOUND ON SHEET 7 OF THE SCHEMATICS.

1. THE IC'S AT LOCATIONS 12A, 12B, AND 14B STORE THE STATUS OF THE CONTROL BOARD PRIOR TO THE MOST RECENT CONTROL CLOCK.

   NOTE THAT ALL OF THEIR OUPTUT SIGNAL NAMES ARE IN PAST TENSE.

2. THE INPUT CONDITIONS THAT CAUSED THEM TO BECOME TRUE MAY OR MAY NOT REMAIN TRUE AFTER BEING LATCHED.

3. THESE "REMEMBERED STATE" SIGNALS ARE DECODED AT 11D, 11C, 11B, 11A, 11F, AND 9B ALONG WITH "DELAY TOP COUNT" TO CONTROL THE DELAY STATUS BITS, "T D", "T D" AND "T D", TO STOP THE RECORDING AT THE CORRECT TIME AND TO CONTROL THE PROCESS OF SELECTIVE TRACE RECORDING.

4. THE 100155 MUX LATCH AT 12B HAS THREE INPUTS.

   TWO OF THESE, "$\overline{\text{ADVANCE}}$" AND "JUMP" ARE CONNECTED TO BOTH THE A AND B MUX INPUTS AND ARE CLOCKED TO THE OUTPUT REGARDLESS OF THE STATE OF THE MUX SELECTION CONTROL ON 12B-16 & 17.

   THE TWO OUTPUT SIGNALS "ADVANCED" AND "JUMPED" ARE OR'ED TOGETHER FORMING "$\overline{\text{DELAY PE}}$", WHICH ALLOWS THE DELAY COUNTER TO BE LOADED ON THE NEXT CLOCK, AND "ADVANCED OR JUMPED" WHICH IS USED TO CONTROL THE STATES OF THE DELAY CONDITION SIGNALS.

5. THE MUX SELECT CONTROL SIGNAL FOR 12B IS "EVENT MODE" WHICH IS AN OUTPUT OF THE 10145A RAM AT 13A.

   THIS BIT IS HIGH AT THOSE LEVELS IN WHICH THE OPERATOR HAS SELECTED EVENTS DELAY MODE.

- IF "EVENTS MODE" IS LOW, THE A MUX INPUTS OF 12B ARE SELECTED, CAUSING 12B-9 TO LATCH LOW ON EVERY CLOCK.

  WHEN "EVENTS MODE" IS HIGH, 12B-9 WILL LATCH LOW ONLY WHEN "$\overline{\text{EVENT}}$" IS LOW.

6. THE SIGNAL AT 12B-9 IS CALLED "$\overline{\text{EVENTED}}$". "$\overline{\text{EVENTED}}$" IS COMBINED WITH "$\overline{\text{OLD T D}}$" (WHICH IS LOW IF T WAS LESS THAN D PRIOR TO THE LAST CLOCK) TO FORM "$\overline{\text{DELAY CE}}$".

   THUS, IN EVENTS DELAY MODE, THE DELAY COUNTER IS ONLY ALLOWED TO INCREMENT ONCE FOR EACH SAMPLE ON WHICH THE SELECTED EVENT COMBINATION WAS TRUE.

7. THE 100155 AT 14B ALSO HAS THREE INPUTS, TWO OF WHICH ARE CONNECTED TO BOTH THE A AND B MUX INPUTS.

   "STOP" BECOMES "STOPPED" AFTER BEING CLOCKED THROUGH 14B AND CAUSES "ARMED" TO GO FALSE ENDING THE RECORDING PROCESS.

   "TRACE" BECOMES "TRACED" AND "$\overline{\text{TRACED}}$".

   "TRACED" IS COMBINED WITH "ARMED" AND IS FED TO A BNC CONNECTOR ON THE INSTRUMENTS REAR PANEL AS "$\overline{\text{GATE}}$".

   "$\overline{\text{TRACED}}$" IS ROUTED TO THE DATA BOARDS WHERE IT COMBINES WITH "ARMED" TO ALLOW THE SAMPLE WHICH CAUSED THE "TRACE" CONDITION TO BE RECORDED.

8. THE THIRD INPUT TO 14B IS "ADVANCE" WHICH IS CONNECTED ONLY TO A "B" MUX INPUT.

   THE MUX CONTROL INPUT WHICH DETERMINES WHETHER "ADVANCE" WILL BE LATCHED IN 14B IS "END LEVEL", ONE OF THE OUTPUTS OF THE 10145A RAMS AT 13A.

9. "END LEVEL" WILL BE HIGH ONLY AT THE LEVEL SELECTED AS END LEVEL BY THE OPERATOR.

10. THE OUTPUT SIGNAL AT 14B-9 IS CALLED "ADVANCED AND ENDED" AND AS IT'S NAME IMPLIES, IT WILL BE TRUE ONLY IF "ADVANCE" AND "END LEVEL" ARE BOTH TRUE WHEN 14B IS CLOCKED.

    "ADVANCED AND ENDED" CAUSES "ARMED" TO GO FALSE, ENDING THE RECORDING PROCESS.

11. THE 10176 AT 12A HAS SIX INPUTS.

    ONE OF THESE, "CYCLE RESET" IS USED ONLY BY THE MPU DURING THE ARM INITIALIZATION CYCLE OR DURING SELF DIAGNOSTICS.

    THE OTHER FIVE INPUTS TO 12A COORDINATE THE SWITCHING OF THE DELAY STATUS BITS.

12. "$\overline{\text{D=1 IF JUMP}}$" AND "$\overline{\text{D=1 IF ADVANCE}}$" COME FROM THE 10145A RAM AT 13A.

    THESE SIGNALS PROVIDE A LOOK AHEAD FUNCTION TO PROVIDE DELAYS OF "ONE" WHICH THE 10016 DELAY COUNTER CAN NOT PROVIDE.

13. "$\overline{\text{D=1 IF JUMP}}$" AND "$\overline{\text{D=1 IF ADVANCE}}$" WILL BE LOW ONLY IF THE "NEXT LEVEL" (EITHER THE "JUMP-TO" OR THE "ADVANCE-TO" LEVEL OR BOTH) HAS A DELAY OF "ONE" SELECTED.

14. THE OUTPUTS OF 12A "$\overline{\text{D=1 IF JUMPED}}$" AND "$\overline{\text{D=1 IF ADVANCED}}$" ARE COMBINED WITH "$\overline{\text{JUMPED}}$" AND "$\overline{\text{ADVANCED}}$" RESPECTIVELY AT 11C AND 11D TO CAUSE "T=D" TO BECOME TRUE IMMEDIATELY UPON ENTERING A LEVEL WITH A DELAY OF "ONE" SELECTED.

15. "$\overline{\text{T D}}$", "$\overline{\text{T=D}}$", AND "$\overline{\text{T D}}$" ARE CLOCKED THROUGH 12A TO BECOME "$\overline{\text{OLD T=D}}$", "$\overline{\text{OLD T=D}}$", AND "$\overline{\text{OLD T D}}$".

    THESE THREE SIGNALS ALSO MUST BE PRESENT AT 11B, 11C, AND 11D TO INSURE PROPER CYCLING OF THE DELAY CONDITION BITS.

16. THE 10164 MULTIPLEXERS AT 12C AND 12F PROVIDE ACCESS FOR THE MPU TO DETERMINE RECORD CONTROL STATUS AND FOR SELF-DIAGNOSTICS.

G. THE MPU INTERFACE IS SHOWN ON SHEET 9 OF THE SCHEMATIC.

1. THE 74S85 AT 13H DECODES THE ADDRESS BUS TO ENABLE THE INTERFACE ONLY WHEN THE CONTROL BOARD IS ADDRESSED.

2. 11H, 8J, 7J, 3J, AND 10H PROVIDE TTL TO ECL LEVEL TRANSLATION FOR THE 16 LINE ADDRESS/DATA BUS.

3. THE READ DATA FROM THE CONTROL BOARD IS MULTIPLEXED DOWN TO ONLY FOUR LINES.

   THESE ARE TRANSLATED FROM ECL TO TTL LEVELS BY 12H.

4. THE 10161 DEMULTIPLEXER AT 13G DECODES ADDRESS LINES A1, A2, AND A3 ALONG WITH $\overline{WE}$ FROM THE MPU TO PROVIDE "LOAD" SIGNALS FOR THE MPU PROGRAMMABLE HOLDING REGISTERS, WORD DETECTION RAMS AND THE CONTROL RAMS.

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0114-0122	PWB				FAB
2						1	3700-0057	RES PAK	RP71		2.2K 8PIN SIP	
3						1	1800-0105	IC	14G	74LS00		
4						1	1800-0254	IC	13H	74LS85		
5						1	1800-0349	IC	12H	74368A		
6						1	6000-0307	HEADER, BARE			20 PIN RT ANGLE	
7						1	7000-0120	CARD EJECTOR				
8						2	1850-0103	IC	12G, 14J	10125		
9						1	-0097		5A	10231		
10						5	-0104		3J, 7J, 8J, 10H, 11H	10124		
11						6	-0099		4C, 12C, 12D, 12E, 12F, 13J	10164		
12						1	-0106		4A	10117		
13						1	-0111		11A	10103		
14						4	-0114		13C, 13D, 13E, 13F	10016		
15						12	-0098		1H, 2H, 2J, 3H, 4H, 6H 7H, 8H, 9H, 6A, 7A, 12A	10176		
16						9	-0077		1D, 3D, 4D, 5F, 7D 8D, 9B, 9D, 11D	100101		
17						11	-0078		1C, 3C, 4J, 5C, 5D, 7C, 8C, 9C, 11B, 11C, 11F	100102		
18						1	1850-0079	IC	11G	100112		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PRE PILOT REL ERN # 0101	2-11-81	NB		
B	PILOT REL ERN # 0130	4-8-81	[illegible]	JL	
C	REVISED PER ECO № 1725	6-26-81	SR	RD	
D	REVISED PER ECO № 1726	6-26-81	SR	RD	
E	REVISED PER ECO № 1891	8-13-81	NB	RD	
E	PROD REL PER ERN # 0207	1/29/82	NB	RD	

DASH NO.	NUMBER	QTY
-10	0114-0002	1

NEXT ASSEMBLY

		DATE
DRAWN	J W CARROLL	5-19-81
CHECKED	[illegible]	1/22/82
ENGINEER	[illegible]	1-7-82
MANUFACTURING	[illegible]	1/7/82
QUALITY ASSURANCE	[illegible]	1/7/82

LIST OF MATERIAL
ASSEMBLY – CONTROL BOARD

MODEL K101-D

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CODE		REV
B	0114-0120	E

SHEET 1 OF 3

HISTORY COPY

FEB 12 1982

REFERENCE PRINT

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						12	1850-0088	IC	1F,1G,3F,3G,4F,4G, 7F,7G,8F,8G,9F,9G	10422		
20						10	1850-0089-10	IC	1B-8B, 8A, 9A		F10145ADC	
21						7	1850-0089-20	IC	5H,5J,13A,14C-14F		HD10145	
22						3	1850-0091		12B, 14B, 5G	100155		
23						1	1850-0100	IC	13G	10161		
24						122	4010-0103	CAP	C3-21,24-119,122, 123,126,128-131		.01uf, 100V	
25						9	4400-0043	CAP	C1,2,22,23,120, 121,124,125,127		47uf, 6V	
26						1	1400-0019	TRANSISTOR	Q1	2N3906		
27												
28						6	3700-0088	RES PAK	RP 65,67,69,70, 72,74		3K/6.2K, 8 PIN SIP	
29						25	3700-0091	RES PAK	RP1-4,6,7,27,28,40-42 51-53,56-64,66,68		68 Ω, 8 PIN SIP	
30						44	3700-0092	RES PAK	RP5,8-26,29-39,76 43-50,54,55,73,75		68Ω, 10 PIN SIP	
31						1	3000-2001	RESISTOR	R1		2K, 1/4W 5%	
32						1	-2006		R2		20Ω	
33						1	-1800		R3		180Ω	
34						1	-3300		R4		330Ω	
35						1	3000-5106	RESISTOR	R5		51Ω, 1/4W 5%	
36						12	6100-0137	SOCKET	ALL 10422		24 PIN (.4")	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY –
CONTROL BOARD

MODEL K101-D

biomation

B 0114-0120 REV E

CODE

SHEET 2 OF 3

FEB 12 1987

REFERENCE PRINT

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						1	0112-0228-01	EJECTOR, STAMPED			"A1"	
38						17	6100-0120	SOCKET	ALL 10145		16 PIN	
39						6	9000-0054	GND WIRE	GND 1-6			
40												
41						1	6100-0119	SOCKET	X14H		14 PIN	
42												
43						1	1800-0280	IC	14H		74$37	
44												
45												
46												
47												
48												
49												
50												
51												
52												
53												
54												

SSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY,
CONTROL BOARD

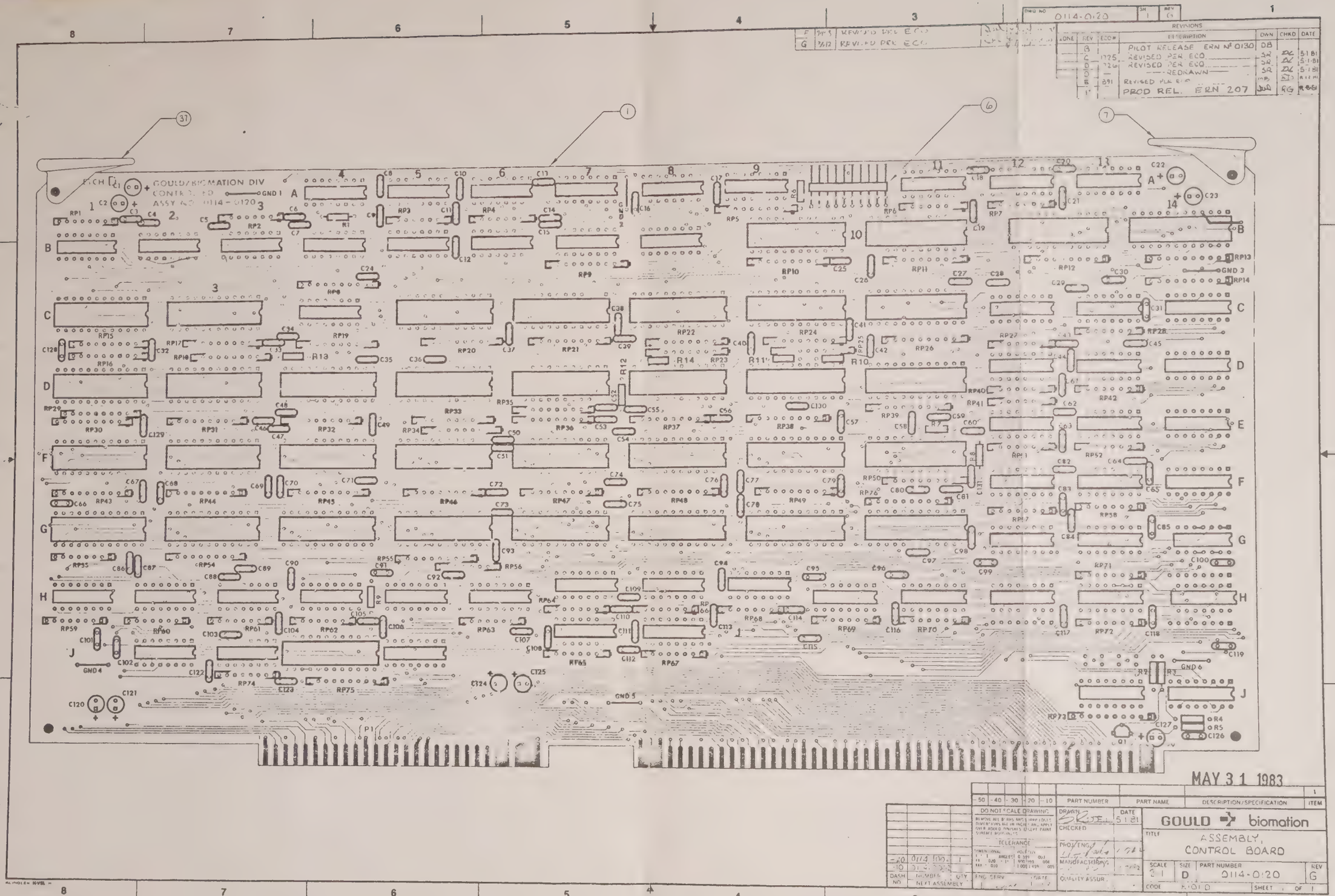
biomation

B	0114-0120	REV E

MODEL K101-D | CODE | SHEET 3 OF 3

FEB 12 1982

REFERENCE PRINT



DWG NO 0114-0120
SH 1
REV G
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
B PILOT RELEASE ERN Nº 0130 DB
C 1725 REVISED PER ECO SR DC 5-1-81
D 726 REVISED PER ECO SR DC 5-1-81
D — REDRAWN SR DC 5-1-81
E 891 REVISED PER ECO
F PROD REL. ERN 207 RG
F 3/13 REVISED PER ECO
G 3/12 REVISED PER ECO
GOULD/BIOMATION DIV
CONTROL BD
ASSY NO 0114-0120
GND 1
GND 2
GND 3
GND 4
GND 5
GND 6
MAY 31 1983
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
DATE 5-1-81
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QUALITY ASSUR
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PART NAME
DESCRIPTION/SPECIFICATION
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GOULD biomation
TITLE ASSEMBLY, CONTROL BOARD
SCALE 2:1
SIZE D
PART NUMBER 0114-0120
REV G
CODE
SHEET 1 OF 1
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1					1	1	0114-0122	PWB				FAB
2					1	1	3700-0057	RES PAK	RP71		2.2K 8PIN SIP	
3					1	1	1800-0105	IC	14G	74LS00		
4					1	1	1800-0254	IC	13H	74LS85		
5					1	1	1800-0349	IC	12H	74368A		
6					1	1	6000-0307	HEADER, BARE			20 PIN RT ANGLE	
7					1	1	7000-0120	CARD EJECTOR				
8					2	2	1850-0103	IC	12G, 14J	10125		
9					1	1	-0097		5A	10231		
10					5	5	-0104		3J, 7J, 8J, 10H, 11H	10124		
11					6	6	-0099		4C, 12C, 12D, 12E, 12F, 13J	10164		
12					1	1	-0106		4A	10117		
13					1	1	-0111		11A	10103		
14					4	4	-0114		13C, 13D, 13E, 13F	10016		
15					12	12	-0098		1H, 2H, 2J, 3H, 4H, 6H 7H, 8H, 9H, 6A, 7A, 12A	10176		
16					9	9	-0077		1D, 3D, 4D, 5F, 7D 8D, 9B, 9D, 11D	100101		
17					11	11	-0078		1C, 3C, 4J, 5C, 5D, 7C, 8C, 9C, 11B, 11C, 11F	100102		
18					1	1	1850-0079	IC	11G	100112		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PRE PILOT REL ERN # 0101	2-11-81	MB		
B	PILOT REL ERN # 0130	4-8-81	[illegible]	JL	
C	REVISED PER ECO Nº 1725	6-2-81	SR	RD	
D	REVISED PER ECO Nº 1726	6-26-81	SR	RD	
E	REVISED PER ECO Nº 1891	8-13-81	MB	RD	
E	PROD REL PER ERN #0207	1/29/82	MB	RD	
F	REVISED PER ECO # 2453	12/10/82	J.G.	[illegible]	

DASH NO.	NUMBER	QTY
-20	0114-1002	1
-10	0114-0002	1

NEXT ASSEMBLY

		DATE
DRAWN	J W CARROLL	5-19-81
CHECKED	[signature]	1/22/82
ENGINEER	[signature]	1-7-82
MANUFACTURING	[signature]	1/7/82
QUALITY ASSURANCE	[signature]	1/7/82

LIST OF MATERIAL
ASSEMBLY – CONTROL BOARD

biomation

MODEL K101-D

CODE B

0114-0120 REV G

SHEET 1 OF 3

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19					—	12	1850-0088	IC	1F,1G,3F,3G,4F,4G, 7F,7G,8F,8G,9F,9G	10422		
20					10	10	1850-0089-10	IC	1B-8B, 8A, 9A		F10145ADC	
21					7	7	1850-0089-20	IC	5H,5J,13A,14C-14F		HD10145	
22					3	3	1850-0091		12B, 14B, 5G	100155		
23					1	1	1850-0100	IC	13G	10161		
24					122	122	4010-0103	CAP	C3-21, 24-119, 122, 123, 126, 128-131		.01uf, 100V	
25					9	9	4400-0043	CAP	C1,2,22,23,120, 121,124,125,127		47uf, 6V	
26					1	1	1400-0019	TRANSISTOR	Q1	2N3906		
27					8	-	1850-0088	IC	4F,4G,7F,7G,8F 8G,9F,9G	10422		
28					6	6	3700-0093	RES PAK	RP 65,67,69,70, 72,74		3K/6.2K, 8 PIN SIP	
29					25	25	3700-0091	RES PAK	RP1-4,6,7,27,28,40-42 51-53,55-64,66,68		68 Ω, 8 PIN SIP	
30					44	44	3700-0092	RES PAK	RP5,8-26,29-39,76 43-50,54,55,73,75		68Ω, 10 PIN SIP	
31					1	1	3000-2001	RESISTOR	R1		2K, 1/4W 5%	
32					1	1	-2006		R2		20Ω	
33					1	1	-1800		R3		180Ω	
34					1	1	-3300		R4		330Ω	
35					1	1	3000-5106	RESISTOR	R5		51Ω, 1/4W 5%	
36					12	12	6100-0137	SOCKET	ALL 10422		24 PIN (.4")	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	REVISED PER ECO # 03512	12-15-82	J.G.	[illegible]	

DRAWN		DATE	
CHECKED			
ENGINEER			
MANUFACTURING			
QUALITY ASSURANCE			

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
ASSEMBLY - CONTROL BOARD

MODEL K101-D

biomation

B	0114-0120	REV G
CODE		SHEET 2 OF 3

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37					1	1	0112-0228-01	EJECTOR, STAMPED			"A1"	
38					17	17	6100-0120	SOCKET	ALL 10145		16 PIN	
39					6	6	9000-0054	GND WIRE	GND 1-6			
40												
41					1	1	6100-0119	SOCKET	X14H		14 PIN	
42					1	1	3000-1002	RESISTOR	R14		10K, 1/4W, 5%	
43					1	1	1800-0280	IC	14H		74S37	
44												
45					6	6	3000-6806	RESISTOR	R6,9 TO 13		68Ω, 1/4W, 5%	
46					2	2	3000-6800	RESISTOR	R7,8		680Ω, 1/4W, 5%	
47												
48												
49												
50												
51												
52												
53												
54												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

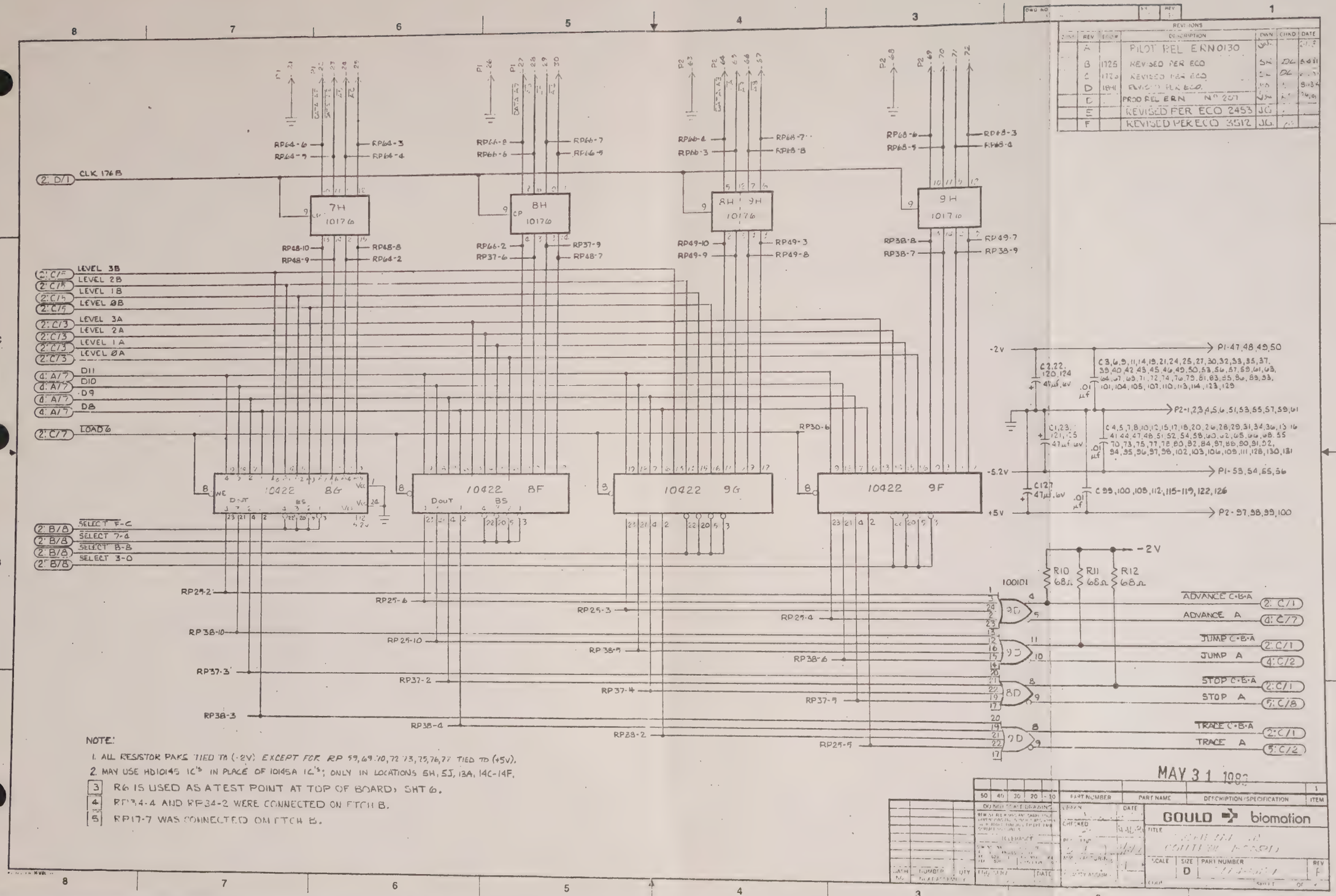
	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

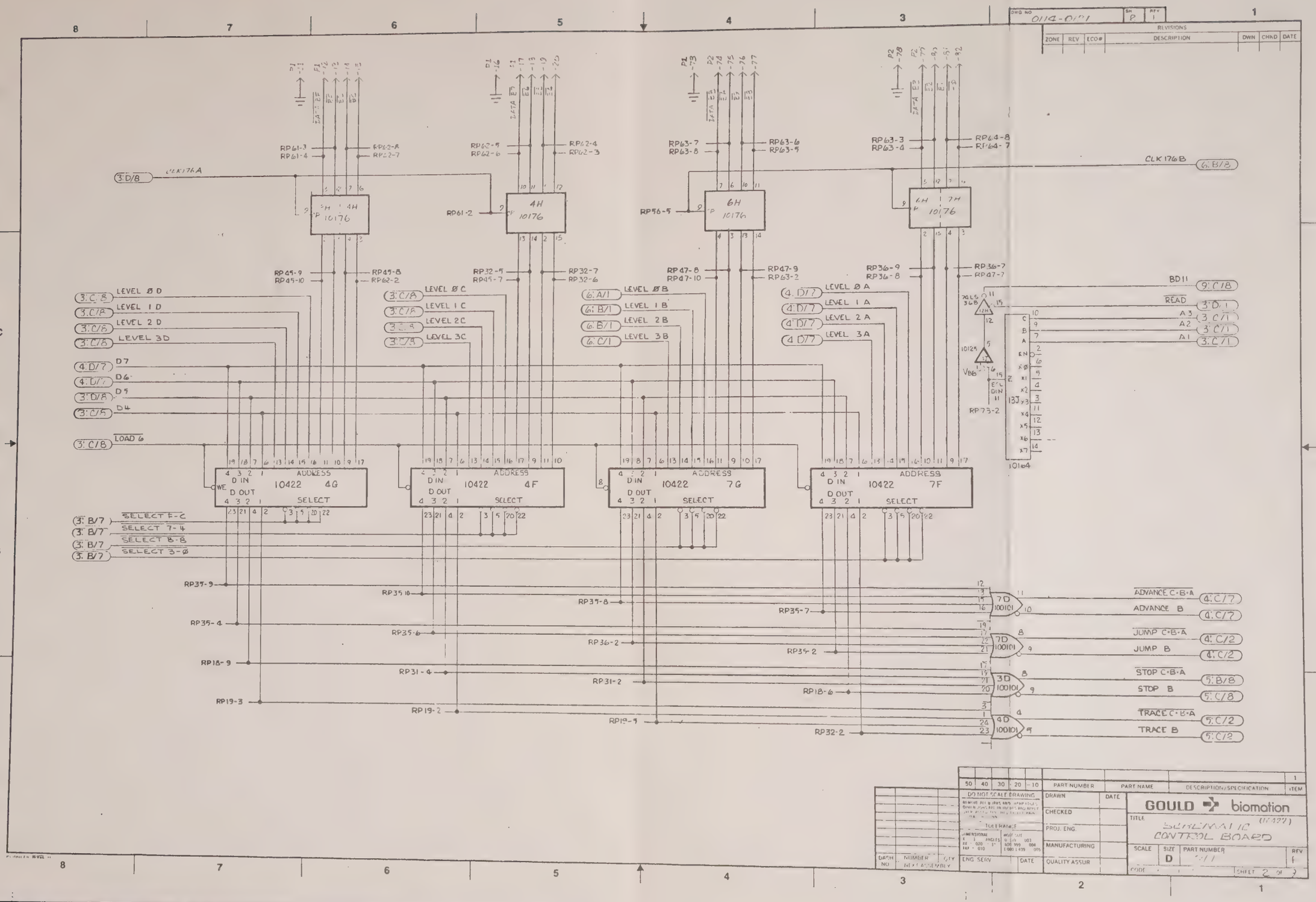
LIST OF MATERIAL
ASSEMBLY,
CONTROL BOARD

MODEL K101-D

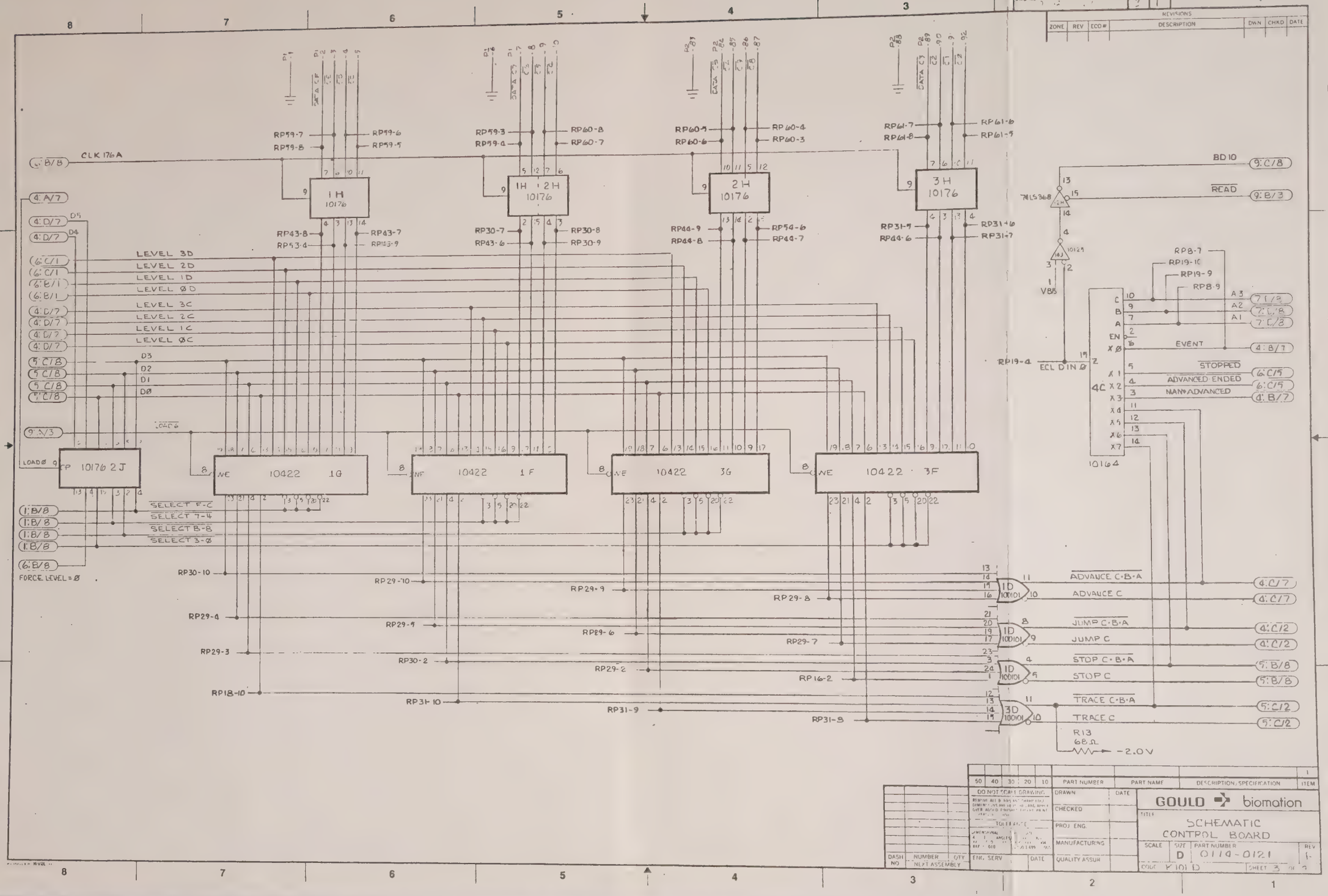
biomation

B	0114-0120	REV G
CODE		SHEET 3 OF 3

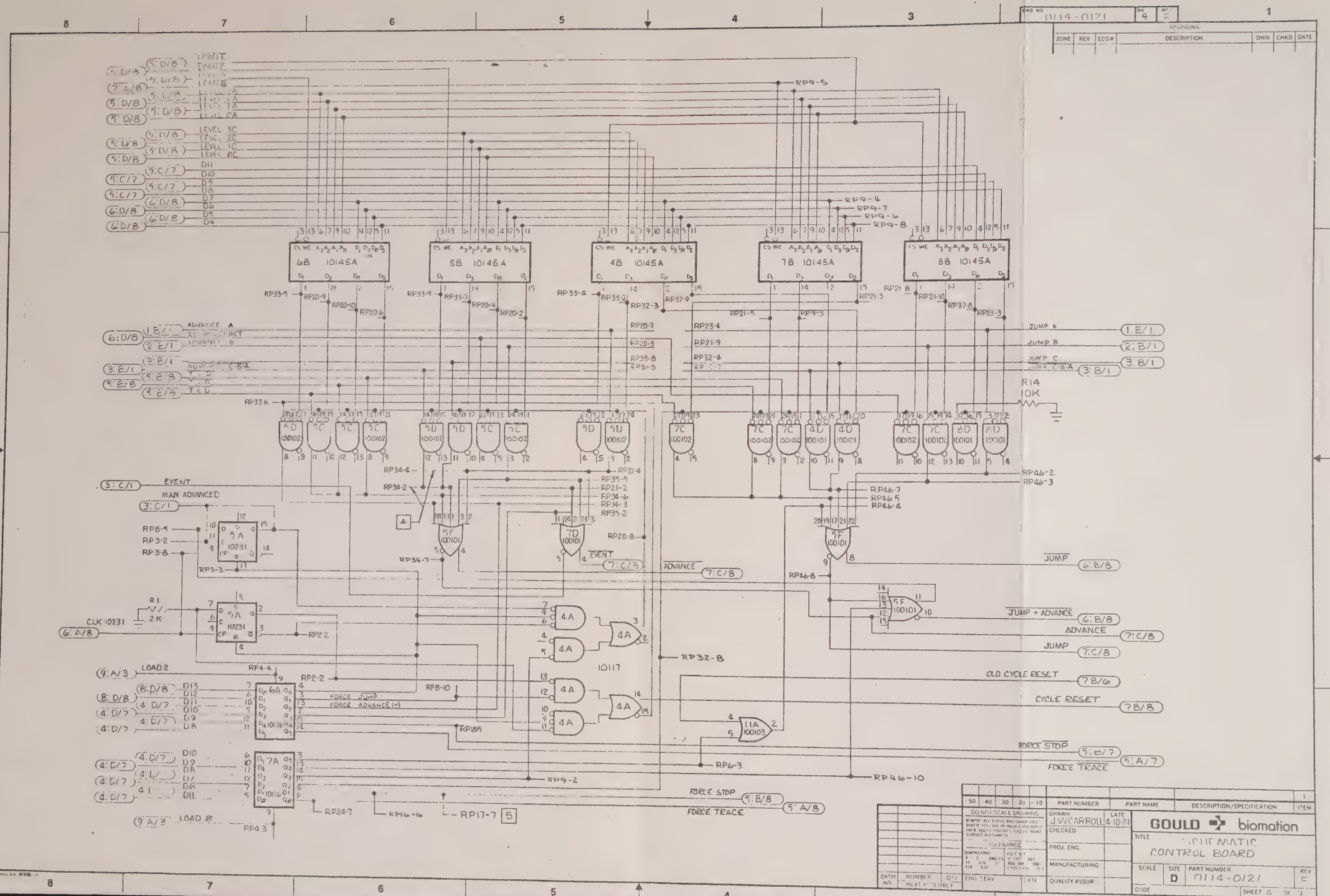

REVISIONS
REV DESCRIPTION DWN CHKD DATE
A PILOT REL ERN0130
B 1125 REVISED PER ECO
C 1126 REVISED PER ECO
D 1841 REVISED PER ECO
D PROD REL ERN No 207
E REVISED PER ECO 2453 JG
F REVISED PER ECO 3512 JG
CLK 176B
7H 10176
8H 10176
8H 9H 10176
9H 10176
LEVEL 3B
LEVEL 2B
LEVEL 1B
LEVEL ØB
LEVEL 3A
LEVEL 2A
LEVEL 1A
LEVEL ØA
D11
D10
D9
D8
LOAD 6
10422 8G
10422 8F
10422 9G
10422 9F
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-0
-2V
P1-47,48,49,50
P2-1,2,3,4,5,6,51,53,55,57,59,61
-5.2V
P1-53,54,55,56
+5V
P2-97,98,99,100
100101
R10 68Ω
R11 68Ω
R12 68Ω
ADVANCE C-B-A
ADVANCE A
JUMP C-B-A
JUMP A
STOP C-B-A
STOP A
TRACE C-B-A
TRACE A
NOTE:
1. ALL RESISTOR PAKS TIED TO (-2V) EXCEPT FOR RP 59,69,70,72,73,75,76,77 TIED TO (+5V).
2. MAY USE HD10145 IC'S IN PLACE OF 10145A IC'S; ONLY IN LOCATIONS 5H, 5J, 13A, 14C-14F.
3. R6 IS USED AS A TEST POINT AT TOP OF BOARD, SHT 6.
4. RP34-4 AND RP34-2 WERE CONNECTED ON PITCH B.
5. RP17-7 WAS CONNECTED ON PITCH B.
MAY 31 1983
GOULD biomation
SCALE SIZE PART NUMBER REV
D F

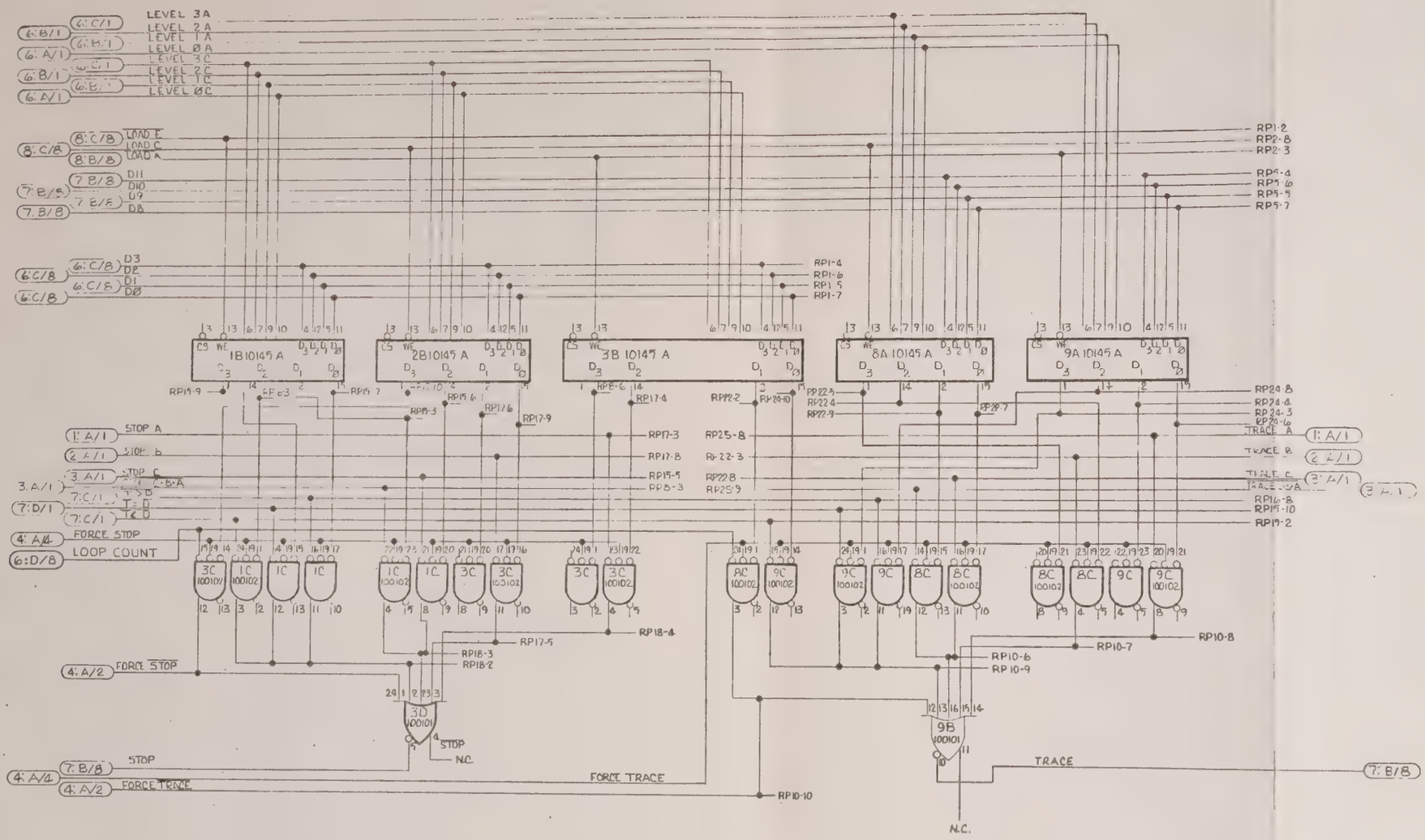


DWG NO 0114-0171
SH 2
REV 1
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
CLK176A
CLK176B
3:D/8
6:B/8
4H 10176
6H 10176
7H 10176
RP61-3
RP61-4
RP62-8
RP62-7
RP62-5
RP62-6
RP62-4
RP62-3
RP63-7
RP63-8
RP63-6
RP63-5
RP63-3
RP63-4
RP64-8
RP64-7
RP61-2
RP56-5
RP45-9
RP45-10
RP45-8
RP62-2
RP32-5
RP45-7
RP32-7
RP32-6
RP47-8
RP47-10
RP47-9
RP63-2
RP36-9
RP36-8
RP36-7
RP47-7
LEVEL Ø D
LEVEL 1 D
LEVEL 2 D
LEVEL 3D
LEVEL Ø C
LEVEL 1 C
LEVEL 2C
LEVEL 3C
LEVEL Ø B
LEVEL 1 B
LEVEL 2 B
LEVEL 3 B
LEVEL Ø A
LEVEL 1 A
LEVEL 2 A
LEVEL 3 A
D7
D6
D5
D4
LOAD 6
BD11
READ
A3
A2
A1
ADDRESS
D IN
D OUT
SELECT
10422 4G
10422 4F
10422 7G
10422 7F
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-Ø
RP35-9
RP35-10
RP35-8
RP35-7
RP35-4
RP35-6
RP36-2
RP35-2
RP18-9
RP31-4
RP31-2
RP18-6
RP19-3
RP19-2
RP19-5
RP32-2
7D 100101
3D 100101
4D 100101
ADVANCE C·B·A
ADVANCE B
JUMP C·B·A
JUMP B
STOP C·B·A
STOP B
TRACE C·B·A
TRACE B
13J
10164
RP73-2
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC
CONTROL BOARD
SCALE
SIZE D
PART NUMBER
REV
SHEET 2 OF 3



CLK 176A
1H 10176
1H 2H 10176
2H 10176
3H 10176
LEVEL 3D
LEVEL 2D
LEVEL 1D
LEVEL ØD
LEVEL 3C
LEVEL 2C
LEVEL 1C
LEVEL ØC
10176 2J
10422 1G
10422 1F
10422 3G
10422 3F
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-Ø
FORCE LEVEL = Ø
BD10
READ
EVENT
STOPPED
ADVANCED ENDED
MAN ADVANCED
ECL DIN Ø
10164
ADVANCE C·B·A
ADVANCE C
JUMP C·B·A
JUMP C
STOP C·B·A
STOP C
TRACE C·B·A
TRACE C
R13 68Ω
-2.0V
GOULD biomation
SCHEMATIC CONTROL BOARD
D 0114-0121


DWG NO 0114-0121
SH 4
REV F
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
6B 10145A
5B 10145A
4B 10145A
7B 10145A
8B 10145A
JUMP A
JUMP B
JUMP C
R14 10K
EVENT
MAN ADVANCED
CLK 10231
R1 2K
LOAD 2
LOAD Ø
FORCE JUMP
FORCE ADVANCE (-)
10117
ADVANCE
JUMP
JUMP + ADVANCE
OLD CYCLE RESET
CYCLE RESET
FORCE STOP
FORCE TRACE
DO NOT SCALE DRAWING
DRAWN J W CARROLL 4-10-81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
CONTROL BOARD
SCALE
SIZE D
PART NUMBER 0114-0121
REV F
CODE
SHEET 4 OF 7



DWG. NO	SH	R
0114-0121	5	F

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

-50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND ARE AFTER OVER ALLOWED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± .1°; XXX = .010

HOLE SIZE: 0 .1 .001; 0 .1 .999 .004; 1 .999 1.499 .005

ENG SERV | DATE

DRAWN: J.W. CARROLL | DATE: 4-2-81

CHECKED

PROJ. ENG

MANUFACTURING

QUALITY ASSUR

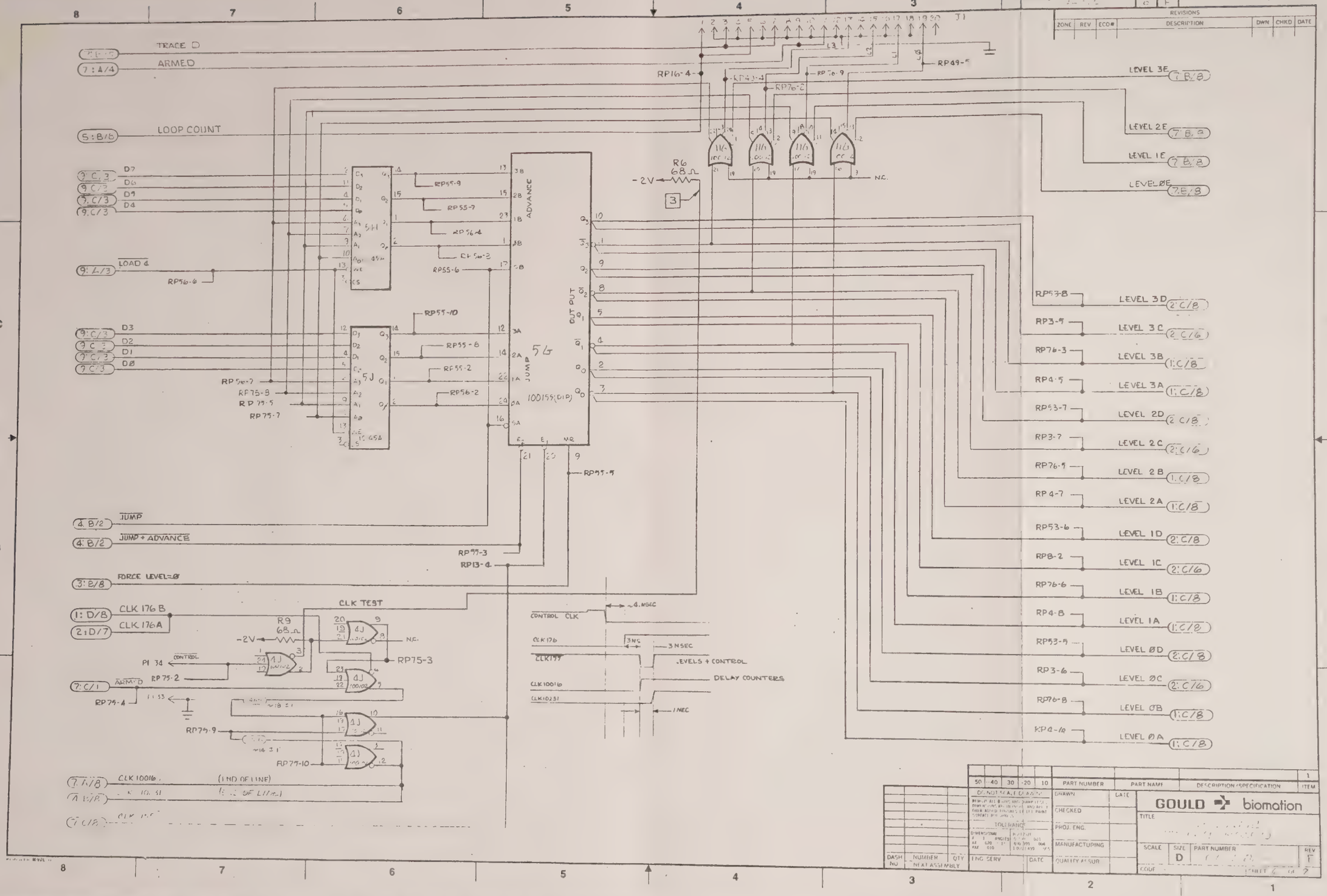
GOULD biomation

TITLE: SCHEMATIC CONTROL BOARD

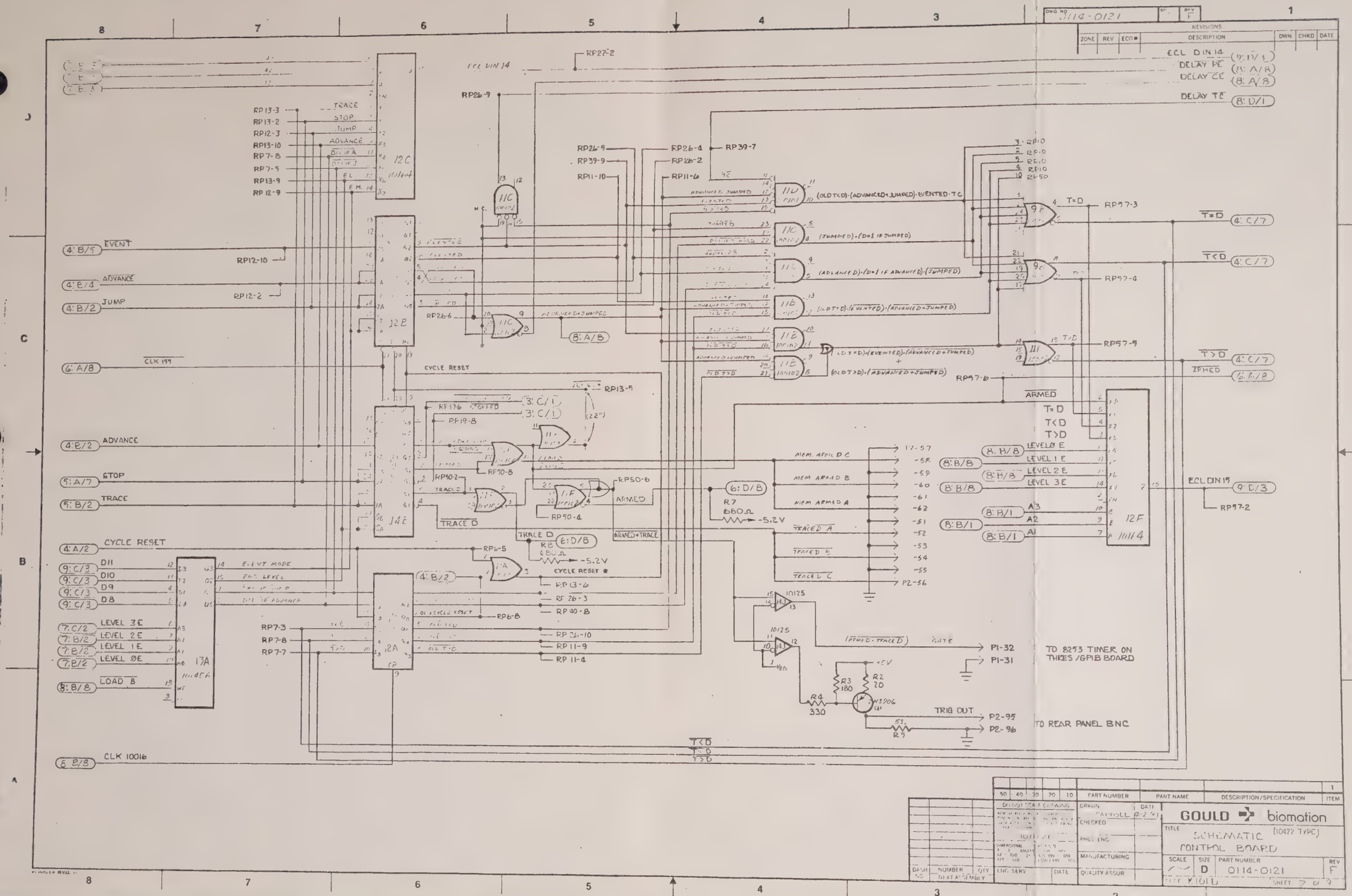
SCALE | SIZE: D | PART NUMBER: 0114-0121 | REV: F

CODE: K 01 D | SHEET 5 OF 9

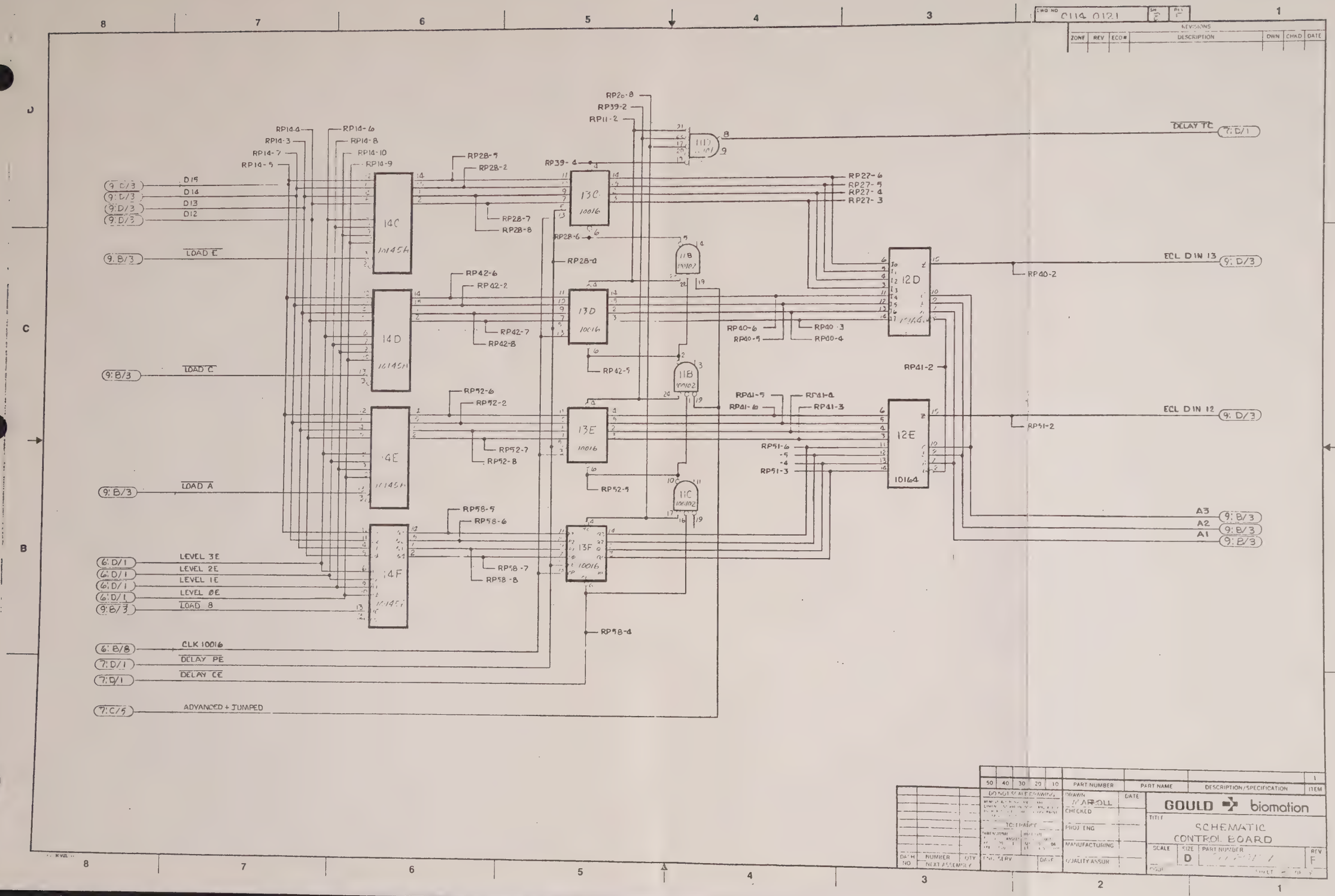
DASH NO | NUMBER | QTY | NEXT ASSEMBLY



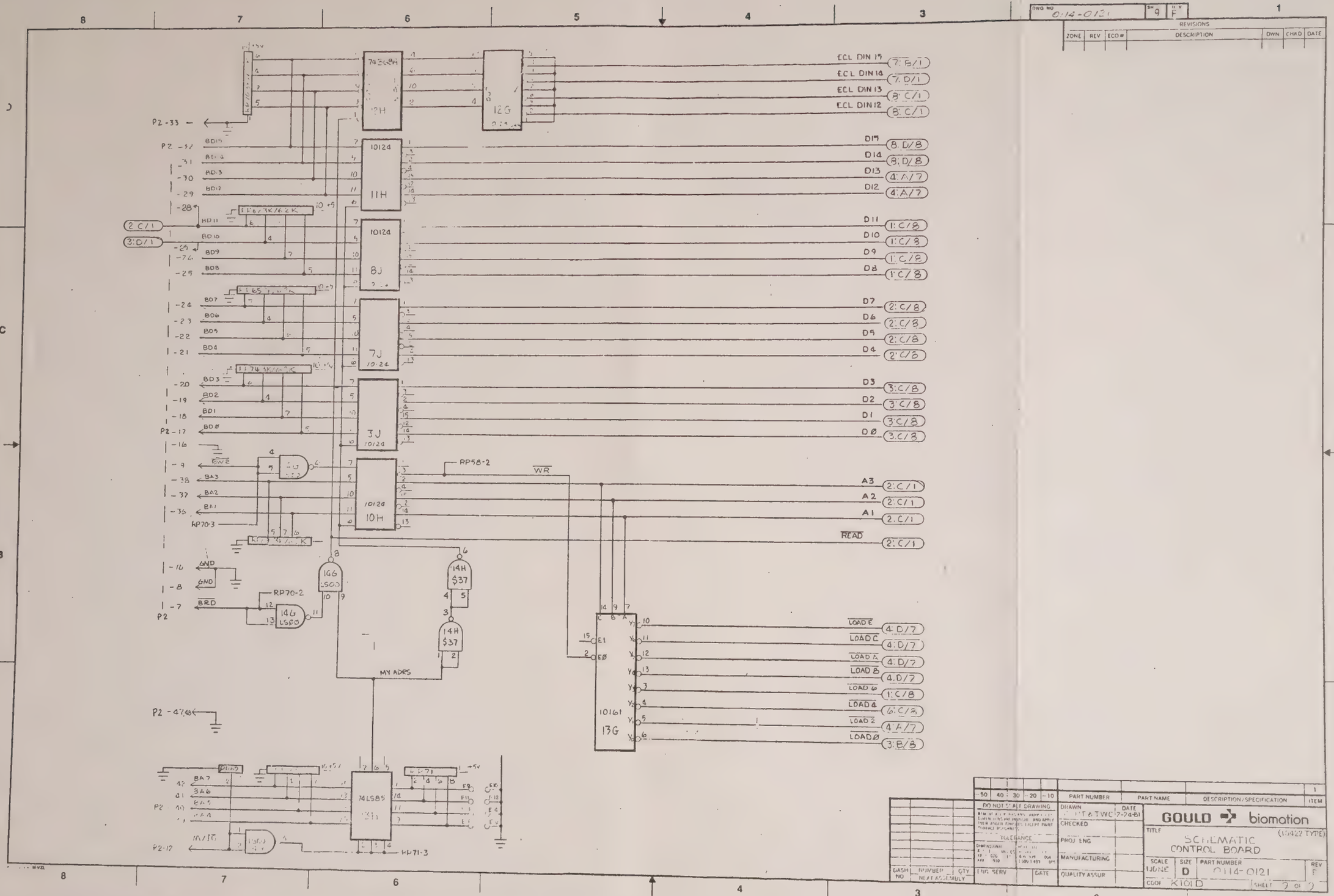
TRACE D
ARMED
LOOP COUNT
LOAD 4
JUMP
JUMP + ADVANCE
FORCE LEVEL=Ø
CLK 176 B
CLK 176A
CLK TEST
CLK 10016
(END OF LINE)
ADVANCE
JUMP
OUT PUT
5G
5H
5J
100159(DIP)
R6 68Ω
R9 68Ω
-2V
N.C.
LEVEL 3E
LEVEL 2E
LEVEL 1E
LEVEL ØE
LEVEL 3D
LEVEL 3C
LEVEL 3B
LEVEL 3A
LEVEL 2D
LEVEL 2C
LEVEL 2B
LEVEL 2A
LEVEL 1D
LEVEL 1C
LEVEL 1B
LEVEL 1A
LEVEL ØD
LEVEL ØC
LEVEL ØB
LEVEL ØA
CONTROL CLK
CLK 176
CLK 177
CLK 10016
CLK 10231
LEVELS + CONTROL
DELAY COUNTERS
3 NSEC
1 NEC
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCALE
SIZE
D
PART NUMBER
REV
F
CODE
SHEET 6 OF 7



DWG NO 0114-0121
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
ECL DIN 14
DELAY PE
DELAY CE
DELAY TC
EVENT
ADVANCE
JUMP
CLK 155
CYCLE RESET
STOP
TRACE
CYCLE RESET
D11
D10
D9
D8
LEVEL 3E
LEVEL 2E
LEVEL 1E
LEVEL 0E
LOAD 8
CLK 10016
ECL DIN 15
ARMED
T=D
T<D
T>D
MEM ARMED C
MEM ARMED B
MEM ARMED A
TRACED A
TRACED B
TRACED C
LEVEL 0 E
LEVEL 1 E
LEVEL 2 E
LEVEL 3 E
TRIG OUT
TO 8253 TIMER ON THRES /GPIB BOARD
TO REAR PANEL BNC
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD (10422 TYPE)
SCALE SIZE D PART NUMBER 0114-0121 REV F
SHEET 2 OF 9



DWG NO C114 0121
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
D15
D14
D13
D12
LOAD E
LOAD C
LOAD A
LEVEL 3E
LEVEL 2E
LEVEL 1E
LEVEL ØE
LOAD 8
CLK 10016
DELAY PE
DELAY CE
ADVANCED + JUMPED
DELAY TC
ECL D IN 13
ECL D IN 12
A3
A2
A1
14C 10145A
14D 10145A
14E 10145A
14F 10145A
13C 10016
13D 10016
13E 10016
13F 10016
11B 100102
11C 100102
11D 100101
12D 10164
12E 10164
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
SCHEMATIC
CONTROL BOARD
SCALE
SIZE D
PART NUMBER
REV F
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE

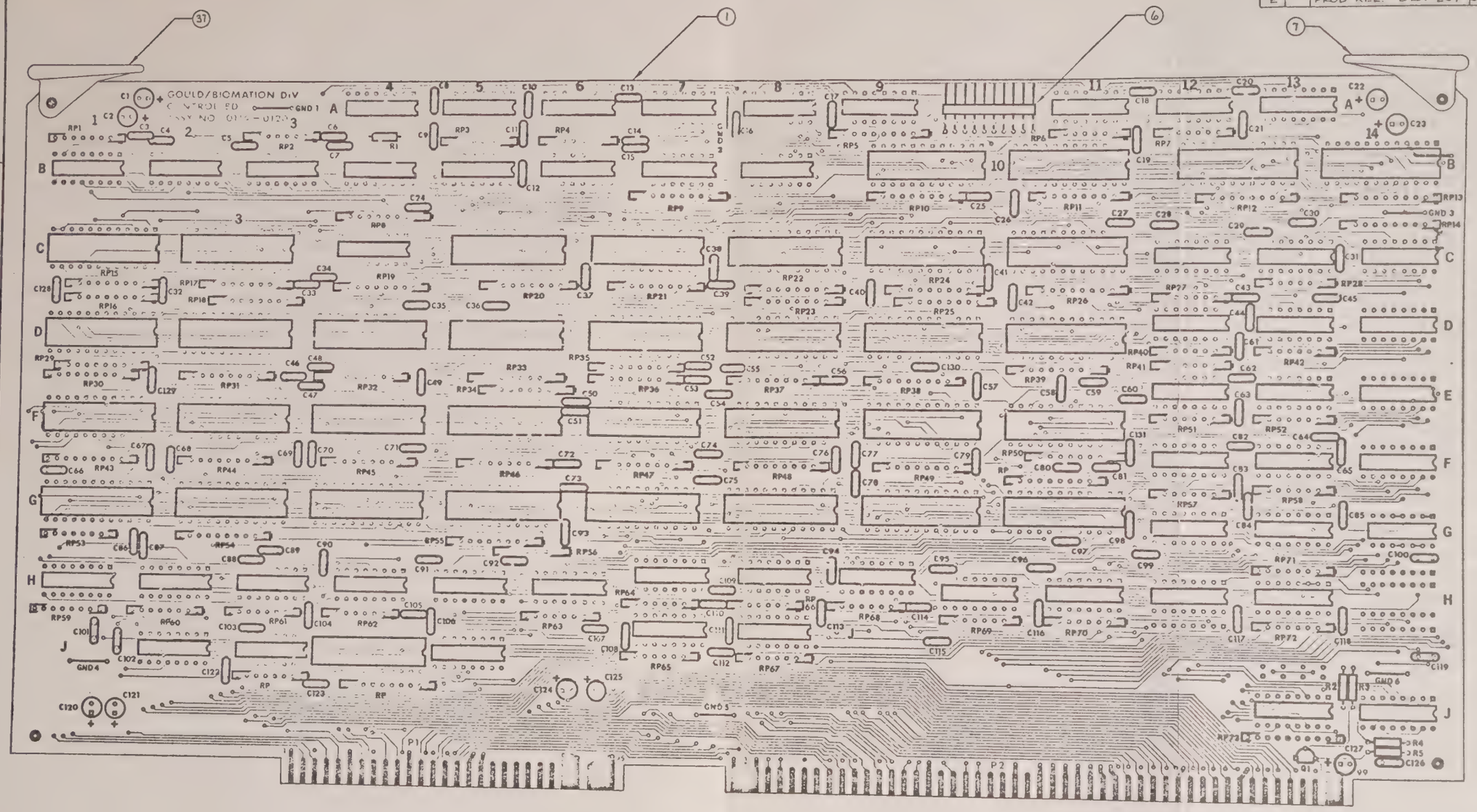


DWG NO 0114-0121
SH 9
REV F
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
ECL DIN 15 (7:B/1)
ECL DIN 14 (7:D/1)
ECL DIN 13 (8:C/1)
ECL DIN 12 (8:C/1)
D15 (8:D/8)
D14 (8:D/8)
D13 (4:A/7)
D12 (4:A/7)
D11 (1:C/8)
D10 (1:C/8)
D9 (1:C/8)
D8 (1:C/8)
D7 (2:C/8)
D6 (2:C/8)
D5 (2:C/8)
D4 (2:C/8)
D3 (3:C/8)
D2 (3:C/8)
D1 (3:C/8)
DØ (3:C/8)
A3 (2:C/1)
A2 (2:C/1)
A1 (2:C/1)
READ (2:C/1)
LOAD E (4:D/7)
LOAD C (4:D/7)
LOAD A (4:D/7)
LOAD B (4:D/7)
LOAD 6 (1:C/8)
LOAD 4 (6:C/8)
LOAD 2 (4:A/7)
LOAD Ø (3:B/8)
74368A 12H
12G
10124 11H
10124 8J
7J 10-24
3J 10124
10124 10H
RP58-2
WR
14G LS00
14H $37
MY ADRS
10161 13G
74LS85 13H
RP71-3
P2-33
P2-47,48
P2-17
P2-12
GND
BRD
RP70-2
RP70-3
2:C/1
3:D/1
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE 7-24-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD (10422 TYPE)
SCALE NONE
SIZE D
PART NUMBER 0114-0121
REV F
CODE K101D
SHEET 9 OF 9

DWG. NO 0114-0120 SH 1 REV

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B		PILOT RELEASE ERN Nº 0130	DB		
	C	1775	REVISED PER ECO	SR	DL	5 1 81
	D	1726	REVISED PER ECO	SR	DL	5 1 81
	D	—	REDRAWN	SR	DL	5 1 81
	E	1891	REVISED PER ECO	MB	DL	5 1 81
	E		PROD REL. ERN 207	[illegible]	RG	[illegible]



HISTORY COPY

FEB 12 1982

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ROUND FINISHES. EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL ± 1 ANGLES ± .020 1 FRACTIONS ± .010

HOLE SIZE .001 .005 .004 .005 .010 .005

DRAWN [illegible] DATE 5 1 81

CHECKED

PROJ ENG [illegible] 1/7/82

MANUFACTURING [illegible] 1/7/82

QUALITY ASSUR [illegible] 1/7/82

ENG SERV [illegible] DATE 1/7/82

DASH NO	NUMBER	QTY
-10	0114-0002	1

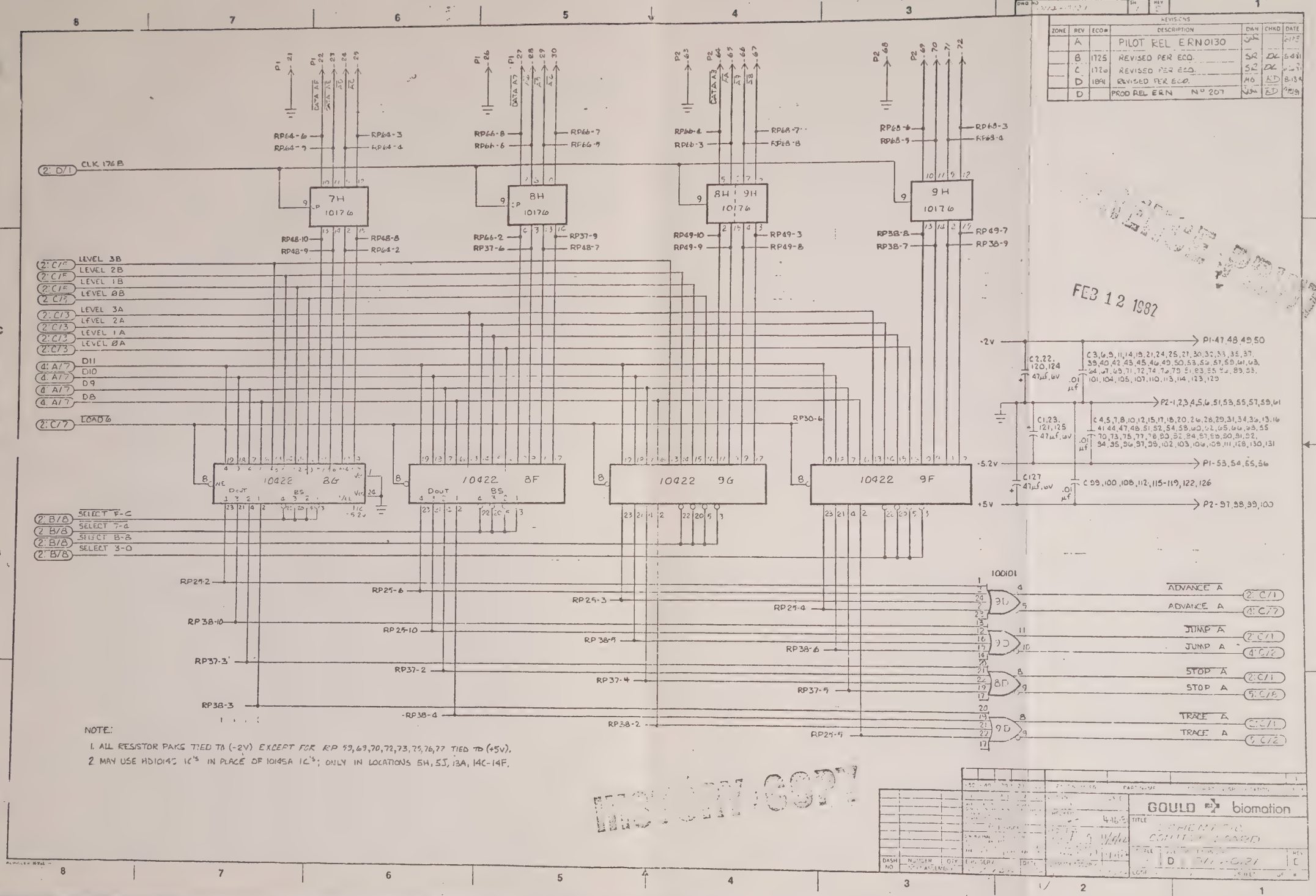
NEXT ASSEMBLY

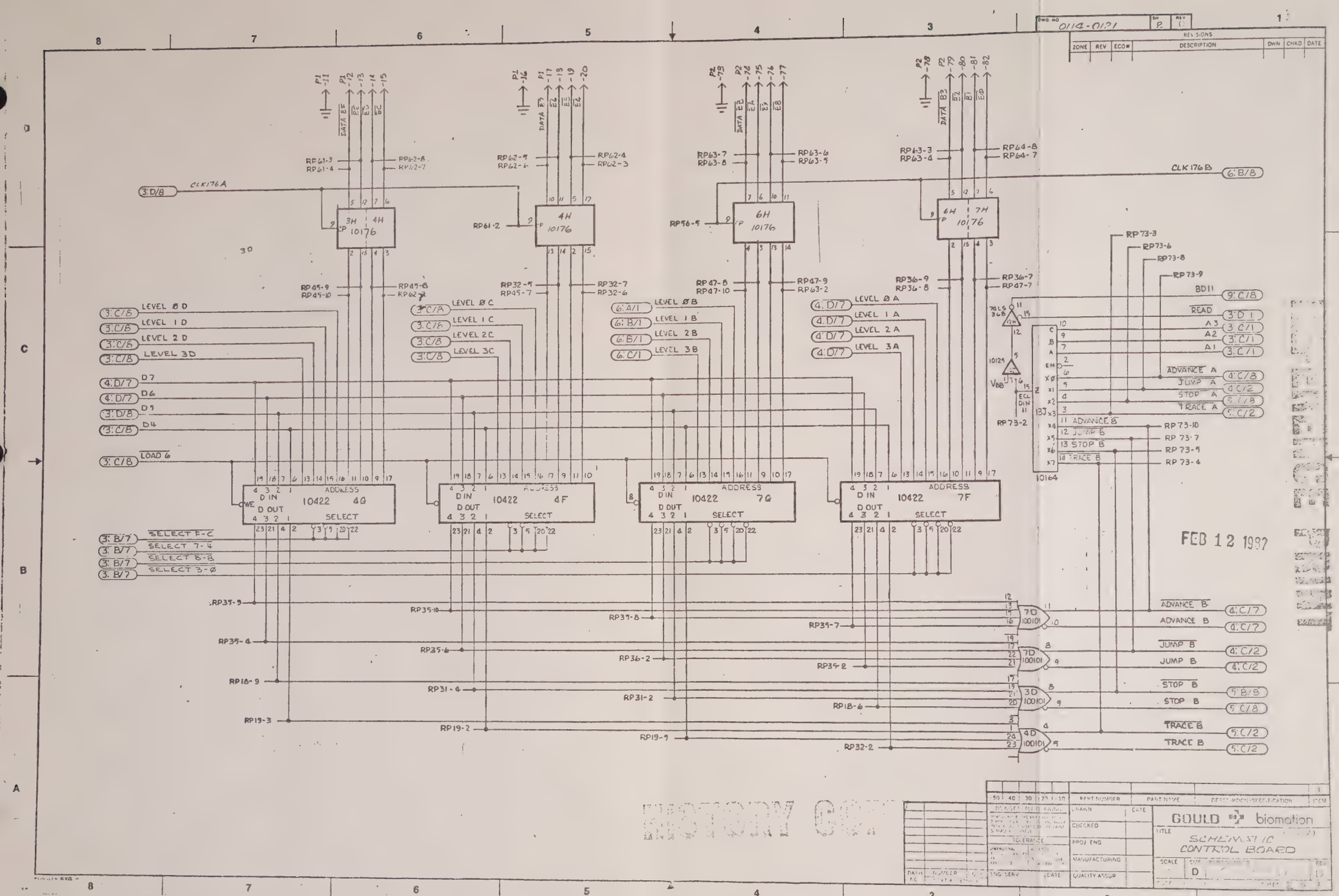
GOULD biomation

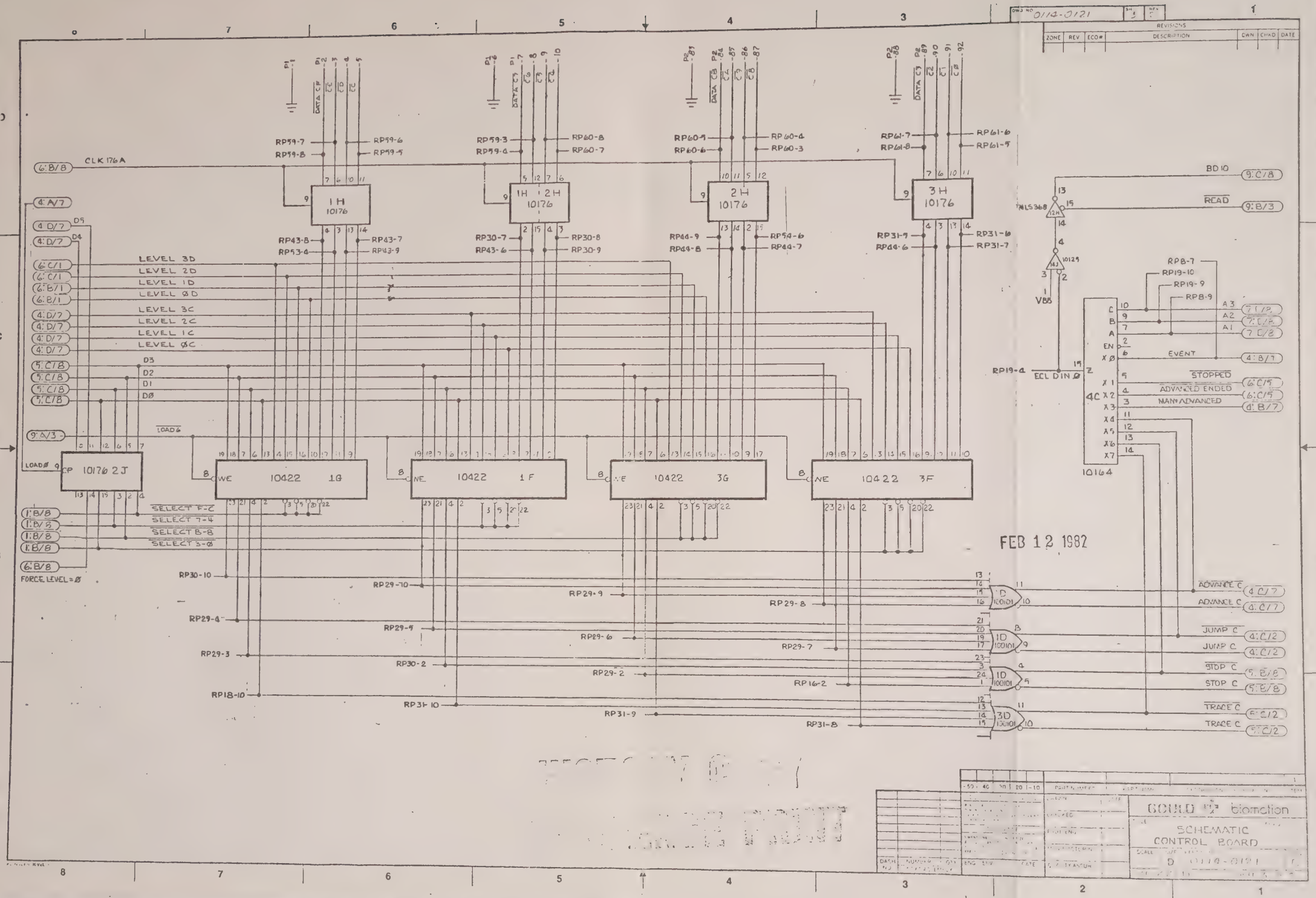
TITLE ASSEMBLY, CONTROL BOARD

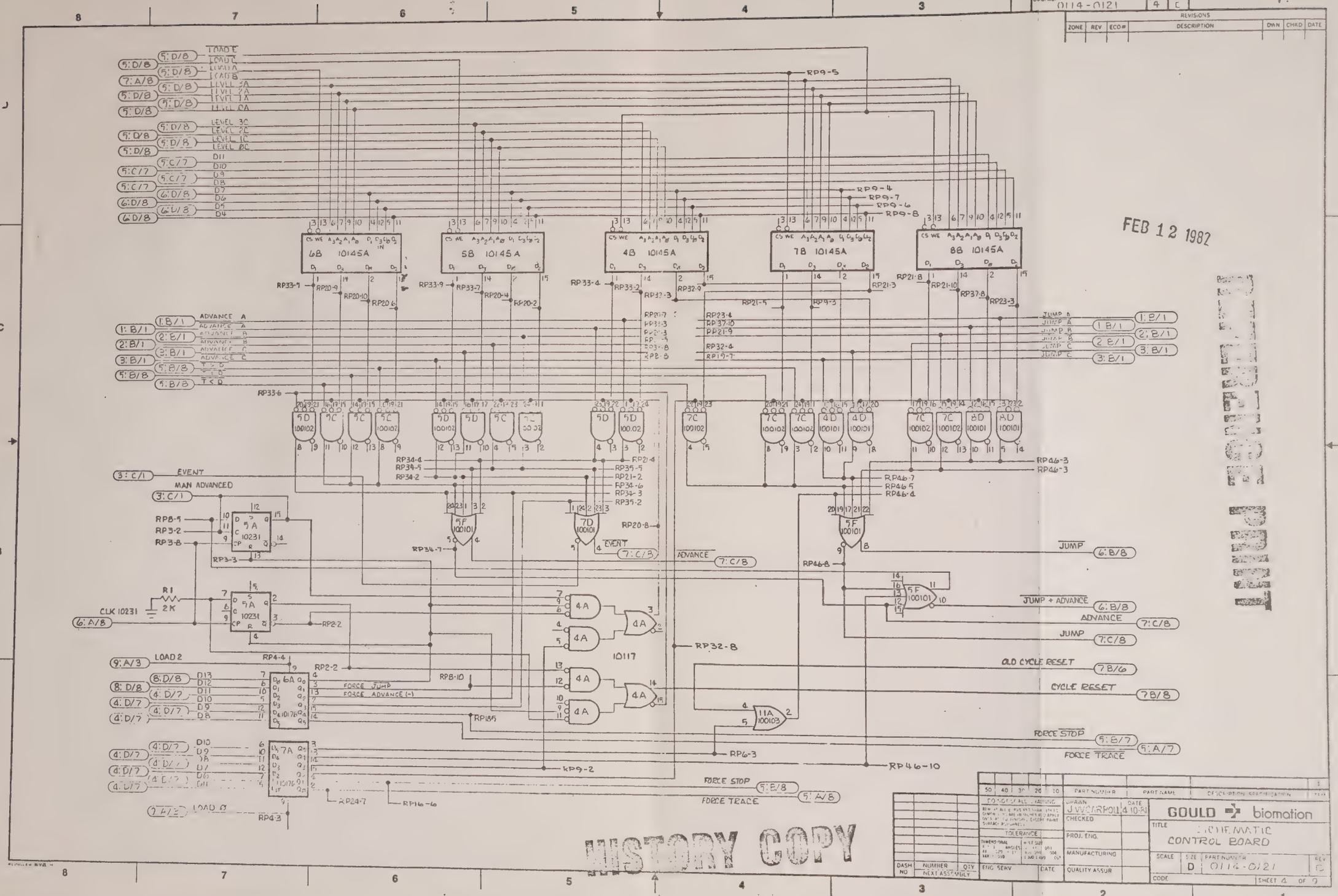
SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0120	E

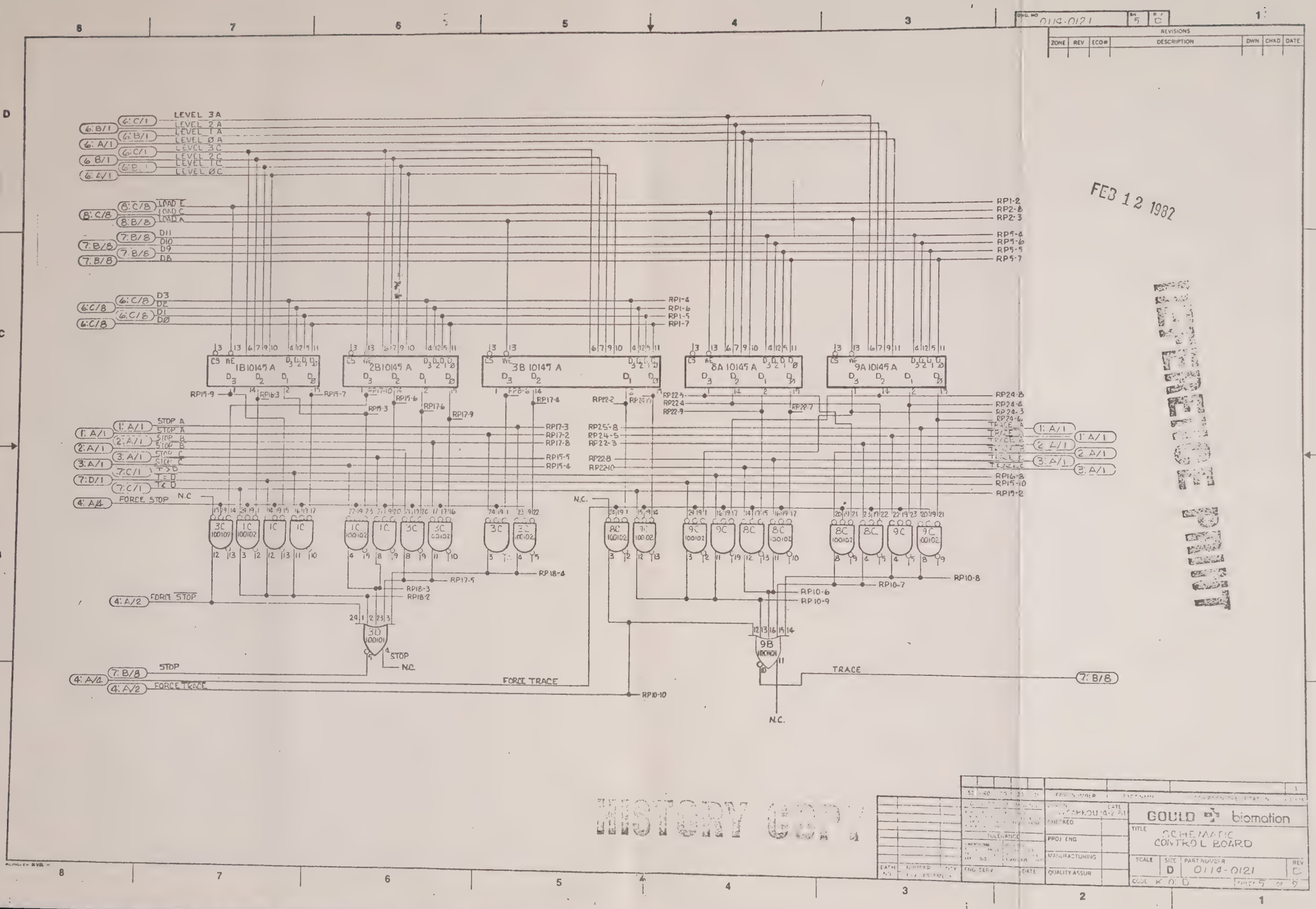
CODE K101-D SHEET 1 OF 1


REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A PILOT REL ERN 0130
B 1725 REVISED PER ECO.
C 1726 REVISED PER ECO.
D 1894 REVISED PER ECO.
D PROD REL ERN Nº 207
7H 10176
8H 10176
8H 9H 10176
9H 10176
10422 8G
10422 8F
10422 9G
10422 9F
CLK 176 B
LEVEL 3B
LEVEL 2B
LEVEL 1B
LEVEL ØB
LEVEL 3A
LEVEL 2A
LEVEL 1A
LEVEL ØA
D11
D10
D9
D8
LOAD 6
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-0
100101
ADVANCE A
JUMP A
STOP A
TRACE A
+2V
-5.2V
+5V
P1-47,48,49,50
P2-1,2,3,4,5,6,51,53,55,57,59,61
P1-53,54,55,56
P2-97,98,99,100
NOTE:
1. ALL RESISTOR PAKS TIED TO (-2V) EXCEPT FOR RP 59,63,70,72,73,75,76,77 TIED TO (+5V).
2. MAY USE HD10145 IC'S IN PLACE OF 10145A IC'S; ONLY IN LOCATIONS 5H, 5J, 13A, 14C-14F.
FEB 12 1982
GOULD biomation


DWG. NO 0114-0121
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
CLK176A
CLK176B
3H 4H 10176
4H 10176
6H 10176
6H 7H 10176
LEVEL Ø D
LEVEL 1 D
LEVEL 2 D
LEVEL 3D
LEVEL Ø C
LEVEL 1 C
LEVEL 2C
LEVEL 3C
LEVEL Ø B
LEVEL 1 B
LEVEL 2 B
LEVEL 3B
LEVEL Ø A
LEVEL 1 A
LEVEL 2 A
LEVEL 3A
D7
D6
D5
D4
LOAD 6
SELECT F-C
SELECT 7-4
SELECT 8-8
SELECT 3-Ø
ADDRESS
D IN
D OUT
SELECT
10422 4G
10422 4F
10422 7G
10422 7F
BD11
READ
A3
A2
A1
ADVANCE A
JUMP A
STOP A
TRACE A
ADVANCE B
JUMP B
STOP B
TRACE B
10164
7D 100101
3D 100101
4D 100101
FEB 12 1982
GOULD biomation
SCHEMATIC CONTROL BOARD
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
TOLERANCE
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
SCALE
SIZE
D


DWG NO 0114-0121
REVISIONS
ZONE REV ECO# DESCRIPTION CHN CHKD DATE
CLK 176A
1H 10176
2H 10176
3H 10176
LEVEL 3D
LEVEL 2D
LEVEL 1D
LEVEL ØD
LEVEL 3C
LEVEL 2C
LEVEL 1C
LEVEL ØC
LOAD6
LOADØ
CP 10176 2J
WE 10422 1G
WE 10422 1F
WE 10422 3G
WE 10422 3F
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-Ø
FORCE LEVEL = Ø
BD 10
READ
EVENT
STOPPED
ADVANCED ENDED
MANY ADVANCED
ECL DIN Ø
10164
ADVANCE C
JUMP C
STOP C
TRACE C
FEB 12 1982
GOULD biomation
SCHEMATIC
CONTROL BOARD
D 0114-0121


DWG. NO 0114-0121
SH 4
REV C
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
FEB 12 1982
6B 10145A
5B 10145A
4B 10145A
7B 10145A
8B 10145A
LOAD E
LOAD D
LEVEL A
LOAD B
LEVEL 3A
LEVEL 2A
LEVEL 1A
LEVEL 0A
LEVEL 3C
LEVEL 2C
LEVEL 1C
LEVEL 0C
D11
D10
D9
D8
D7
D6
D5
D4
ADVANCE A
ADVANCE B
ADVANCE C
T & D
T & D
T & D
EVENT
MAN ADVANCED
CLK 10231
LOAD 2
LOAD 0
FORCE JUMP
FORCE ADVANCE (-)
10117
JUMP A
JUMP B
JUMP C
JUMP
JUMP + ADVANCE
ADVANCE
OLD CYCLE RESET
CYCLE RESET
FORCE STOP
FORCE TRACE
GOULD biomation
KINEMATIC CONTROL BOARD
SCALE D
PART NUMBER 0114-0121
REV C
SHEET 4 OF 9
DRAWN J.W.O.&R.POLL 4-10-81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION
TOLERANCE
HISTORY COPY

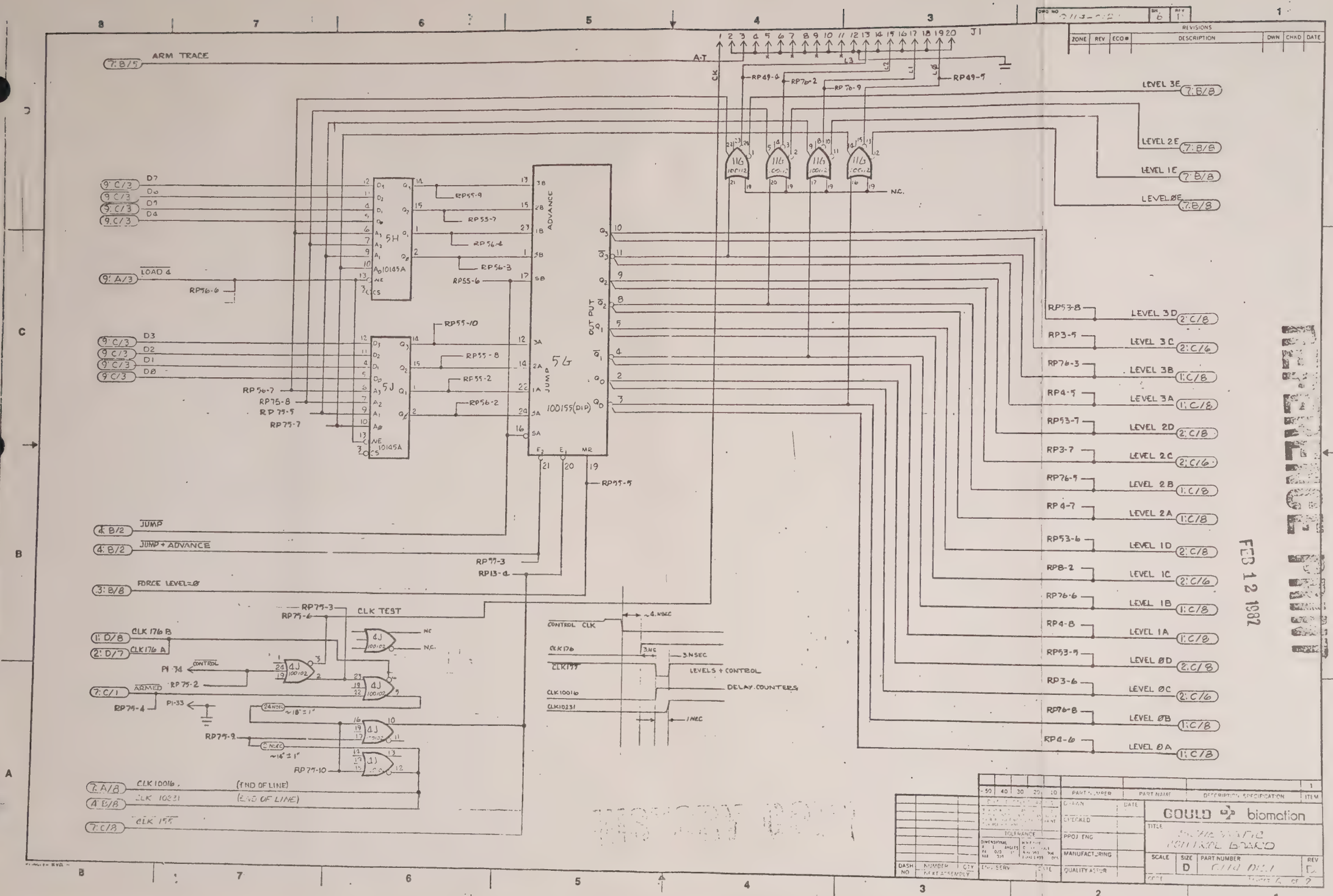


FEB 12 1982

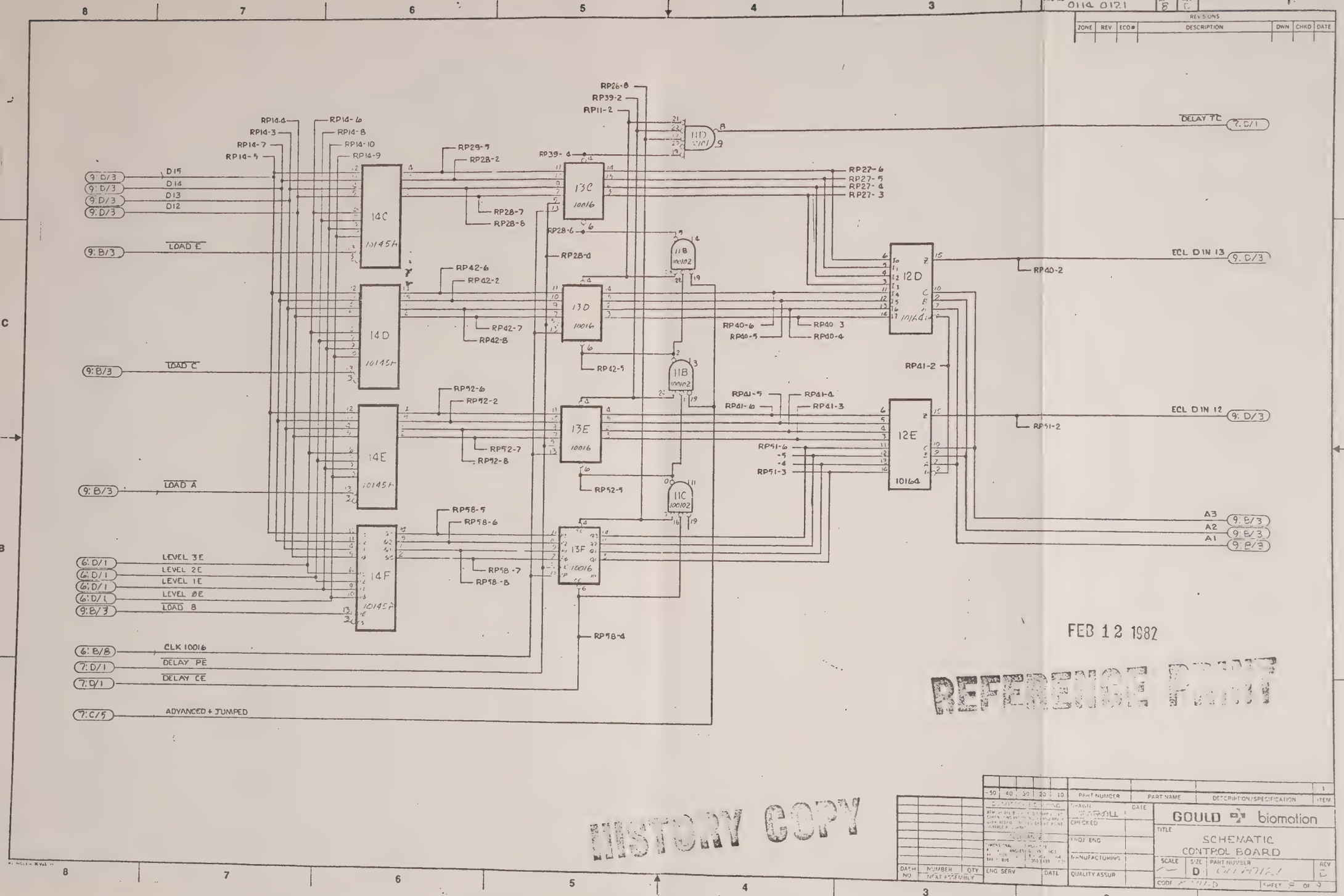
REFERENCE PRINT

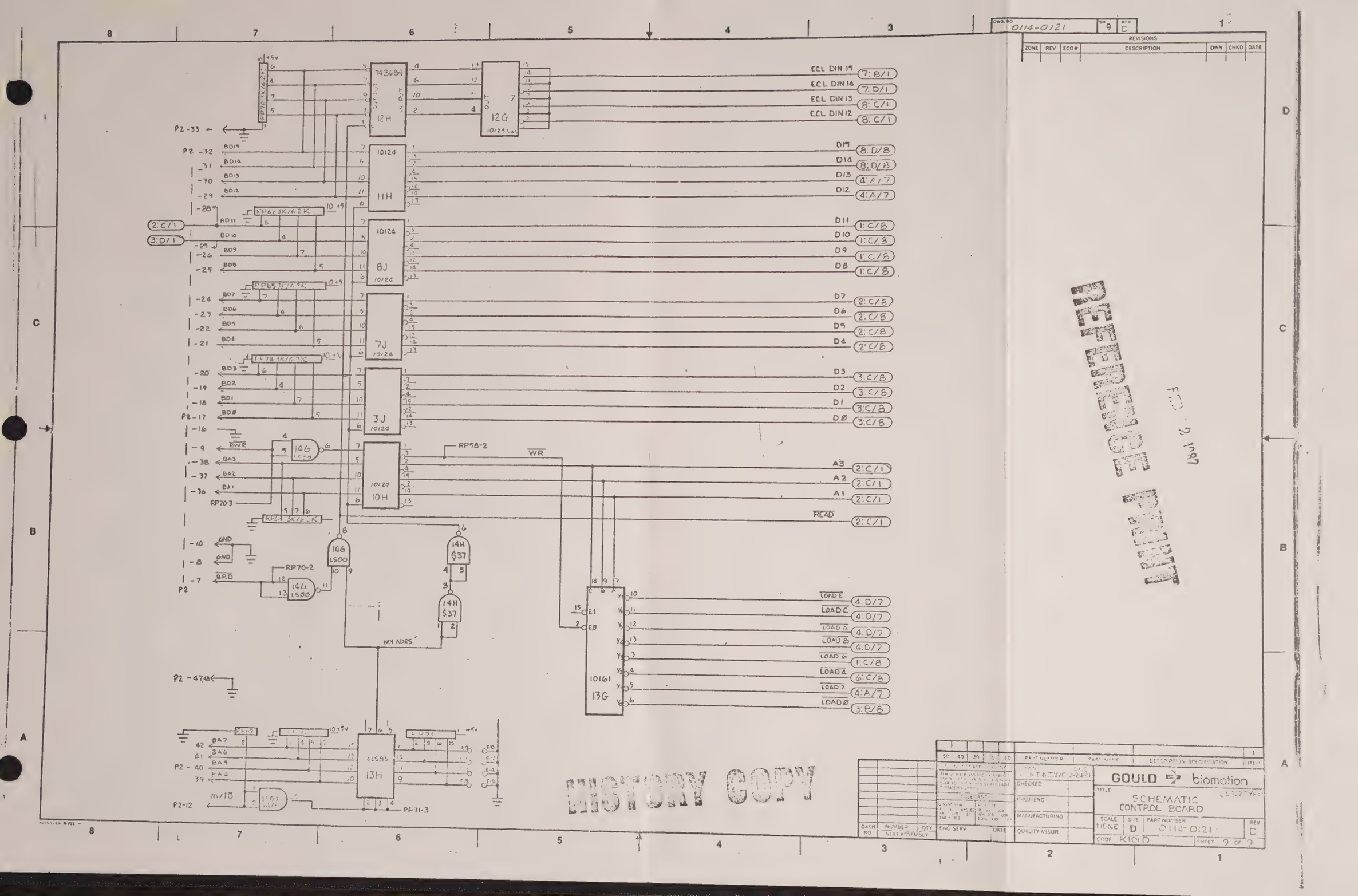
HISTORY COPY

GOULD biomation			
TITLE SCHEMATIC CONTROL BOARD			
SCALE	SIZE D	PART NUMBER 0114-0121	REV D
CODE K.O.D		SHEET 5 OF 9	



ARM TRACE
7:B/5
A-T
J1
RP49-4
RP76-2
RP76-9
RP49-5
LEVEL 3E 7:B/8
LEVEL 2E 7:B/8
LEVEL 1E 7:B/8
LEVEL ØE 7:B/8
N.C.
9:C/3 D7
9:C/3 D6
9:C/3 D5
9:C/3 D4
9:A/3 LOAD 4
RP56-6
5H
10145A
RP55-9
RP55-7
RP56-4
RP56-3
RP55-6
ADVANCE
5G
JUMP
100155(DIP)
OUT PUT
RP55-10
RP55-8
RP55-2
RP56-2
9:C/3 D3
9:C/3 D2
9:C/3 D1
9:C/3 DØ
RP56-7
RP75-8
RP75-5
RP75-7
5J
10145A
RP55-5
RP53-8 LEVEL 3D 2:C/8
RP3-5 LEVEL 3C 2:C/6
RP76-3 LEVEL 3B 1:C/8
RP4-5 LEVEL 3A 1:C/8
RP53-7 LEVEL 2D 2:C/8
RP3-7 LEVEL 2C 2:C/6
RP76-5 LEVEL 2B 1:C/8
RP4-7 LEVEL 2A 1:C/8
RP53-6 LEVEL 1D 2:C/8
RP8-2 LEVEL 1C 2:C/6
RP76-6 LEVEL 1B 1:C/8
RP4-8 LEVEL 1A 1:C/8
RP53-5 LEVEL ØD 2:C/8
RP3-6 LEVEL ØC 2:C/6
RP76-8 LEVEL ØB 1:C/8
RP4-6 LEVEL ØA 1:C/8
4:B/2 JUMP
4:B/2 JUMP + ADVANCE
RP55-3
RP13-4
3:B/8 FORCE LEVEL=Ø
RP75-3
RP75-6
CLK TEST
1:D/8 CLK 176 B
2:D/7 CLK176 A
P1-34 CONTROL
RP75-2
7:C/1 ARMED
RP75-4
P1-33
24NSEC ~18"±1"
RP75-9
2NSEC ~14"±1"
RP75-10
7:A/8 CLK 10016 (END OF LINE)
4:B/8 CLK 10231 (END OF LINE)
7:C/8 CLK 155
CONTROL CLK
CLK176
CLK155
CLK10016
CLK10231
~4NSEC
3NSEC
LEVELS + CONTROL
DELAY COUNTERS
1NEC
FEB 12 1982
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD
SCALE D
PART NUMBER
REV D


DWG NO 0114 0121
SH 8
REV C
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
DELAY TC
ECL DIN 13
ECL DIN 12
A3
A2
A1
D15
D14
D13
D12
LOAD E
LOAD C
LOAD A
LEVEL 3E
LEVEL 2E
LEVEL 1E
LEVEL ØE
LOAD B
CLK 10016
DELAY PE
DELAY CE
ADVANCED + JUMPED
14C 10145H
14D 10145H
14E 10145H
14F 10145A
13C 10016
13D 10016
13E 10016
13F 10016
11D 10101
11B 100102
11C 100102
12D 10164
12E 10164
FEB 12 1982
REFERENCE PRINT
HISTORY COPY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC
CONTROL BOARD
SCALE
SIZE D
PART NUMBER
REV C
CODE
SHEET 2 OF 9
DRAWN
CHECKED
ENGR ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY



DWG. NO 0114-0121
SH 9
REV D
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
ECL DIN 15 7: B/1
ECL DIN 14 7: D/1
ECL DIN 13 8: C/1
ECL DIN 12 8: C/1
D15 8: D/8
D14 8: D/8
D13 4: A/7
D12 4: A/7
D11 1: C/8
D10 1: C/8
D9 1: C/8
D8 1: C/8
D7 2: C/8
D6 2: C/8
D5 2: C/8
D4 2: C/8
D3 3: C/8
D2 3: C/8
D1 3: C/8
DØ 3: C/8
A3 2: C/1
A2 2: C/1
A1 2: C/1
READ 2: C/1
LOAD E 4: D/7
LOAD C 4: D/7
LOAD A 4: D/7
LOAD B 4: D/7
LOAD 6 1: C/8
LOAD 4 6: C/8
LOAD 2 4: A/7
LOADØ 3: B/8
74368A 12H
12G 10125
10124 11H
10124 8J
10124 7J
10124 3J
10124 10H
14G LS00
14H $37
10161 13G
MY ADRS
RP58-2
WR
RP70-3
RP70-2
P2-33
P2-47,48
P2-12
P2-40
P2-17
P2-32
P2-31
P2-30
P2-29
P2-28
P2-26
P2-25
P2-24
P2-23
P2-22
P2-21
P2-20
P2-19
P2-18
P2-17
P2-16
P2-10
P2-8
P2-7
P2-40
P2-12
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BDØ
BWR
BA3
BA2
BA1
GND
BRD
BA7
BA6
BA5
BA4
MV10
PP71-3
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD
SCALE NONE
SIZE D
PART NUMBER 0114-0121
REV D
CODE K101D
SHEET 9 OF 9
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
REFERENCE PRINT
FEB 2 1987
HISTORY COPY

SWITCHING POWER SUPPLY
OPERATING THEORY

REFERENCE SCHEMATIC # 0285-0010

THE SWITCHING POWER SUPPLY PROVIDES FIVE VOLTAGES:

-5.2 V	AT	32 A
-2.0 V	AT	22 A
+5.0 V	AT	10 A
+15 V	AT	1.5 A
-15 V	AT	1.5 A

A. THE SWITCHING REGULATOR CONTROLS THE -5.2 V DIRECTLY AND PROVIDES THE RAW DC VOLTAGES FOR LINEAR REGULATORS WHICH CONTROL THE OTHER OUTPUTS.

B. REFERRING TO SHEET 1 OF THE SCHEMATIC, THE LINE VOLTAGE IS FILTERED AND APPLIED TO; AN OUTPUT PLUG WHICH DRIVES TWO FANS, TRANSFORMER T1, AND TO RECTIFIER CR35.

   1. THE SECONDARY OUTPUT OF T1 IS RECTIFIED AND REGULATED BY Q1 AND VR1 TO SUPPLY ±15 V TO POWER THE INTERNAL CONTROL CIRCUITS OF THE SUPPLY. (THESE ARE NOT OUTPUT VOLTAGES)

C. SWITCH S3 PROVIDES 110/220 V SWITCHING FOR T1 AND THE FAN OUTPUT.

   1. S3 ALSO CONTROLS THE OPERATION OF THE OUTPUT FILTERS ON CR35.

      WHEN S3 IS IN THE 110 V POSITION (OPEN) CR35, C12 AND C13 ARE CONNECTED AS A VOLTAGE DOUBLER TO PROVIDE ±150 VDC UNREGULATED.

      WITH S3 CLOSED, C12 AND C13 SIMPLY PEAK FILTER THE RECTIFIED LINE OUTPUT FROM CR35.

D. RT 1 AND RT 2 ARE THERMISTORS.

1. THEIR HIGH RESISTANCE WHEN COLD SLOWS THE SURGE OF CURRENT TO CHARGE C12 AND C13 AT TURN-ON.

2. UNDER NORMAL OPERATING CONDITIONS, C12 AND C13 DISCHARGE VERY SLOWLY AFTER POWER-DOWN.

3. WHEN THE COVER IS REMOVED FOR MAINTENANCE, S2 OPENS, ENABLING Q4 WHICH ACTS AS A FAST DISCHARGE PATH WHEN POWER IS TURNED OFF.

4. OPTO-ISOLATOR U14 HOLDS Q4 OFF WHEN POWER IS ON.

5. THIS FAST DISCHARGE IS FOR PROTECTION OF SERVICE PERSONNEL.

E. CR4 AND CR5 ARE "TRANSORBS" WHICH PROTECT THE SWITCHING TRANSISTORS FROM LINE TRANSIENTS.

1. IF THE UNIT IS PLUGGED INTO 220 V WHEN S3 IS IN THE 110 V POSITION, THE "TRANSORBS" WILL SHORT, BLOWING THE FUSE, BUT PROTECTING THE SWITCHING TRANSISTORS.

F. THE SWITCHING REGULATOR IS AT LOCATION U8, A TL 494.

1. AN INTERNAL 40 KHZ OSCILLATOR ALTERNATELY PULSES THE OUTPUTS AT U8 PINS 8 AND 11.

   THESE PULSES ARE THE BASE DRIVE SIGNALS FOR SWITCHING TRANSISTORS Q7 AND Q8.

2. U8 VARYS THE OUTPUT PULSE WIDTH (AND THUS THE "ON TIME" OF Q7 & Q8) TO MAINTAIN CONSTANT FEEDBACK VOLTAGE FROM THE -5.2 VDC OUTPUT OF THE T6 SECONDARY RECTIFIERS.

3. Q5, Q6, T4, T5 AND ASSCOCIATED COMPONENTS SHAPE AND COUPLE THE DRIVE SIGNALS TO THE BASES OF Q7 AND Q8.

4. Q7 AND Q8 SWITCH THE PRIMARY OF T6 BETWEEN PLUS AND MINUS 150 VDC AT A 20 KHZ RATE.

THIS HIGH FREQUENCY ALLOWS T6 TO BE RELATIVELY SMALL COMPARED TO A 60 HZ TRANSFORMER AND ALLOWS FOR PHYSICALLY SMALLER COMPONENTS FOR FILTERING THE RECTIFIED OUTPUTS.

5. T7, CR6, CR7, R17, R18, AND C14 ACT AS A SENSOR FOR PRIMARY CURRENT.

6. THE VOLTAGE ON C14 IS PROPORTIONAL TO THE AVERAGE CURRENT IN THE PRIMARY WINDING.

7. T6 HAS THREE SECONDARY WINDINGS WHO'S OUTPUTS ARE RECTIFIED AND FILTERED TO PROVIDE 5 DC VOLTAGES:

- 5.20 V	REGULATED
+ 6.00 V	UNREGULATED
- 3.00 V	UNREGULATED
-17.00 V	UNREGULATED
+17.00 V	UNREGULATED

8. THE REGULATED -5.2 V OUTPUT IS FED TO THE OUTPUT OF THE SUPPLY VIA THE FILTER BOARD AFTER PASSING THROUGH R90, A 1.2 MILLI-OHM RESISTOR.

9. R90 AND R95 ACT AS A CURRENT SENSOR.

   THE VOLTAGE DIFFERENCE BETWEEN THE BOTTOM OF R95 AND THE OUTPUT SIDE OF R90 IS PROPORTIONAL TO THE CURRENT DRAWN FROM THE -5.2 V SUPPLY.

10. THE 4 UNREGULATED VOLTAGES FROM THE SECONDARY RECTIFIERS GO TO LINEAR REGULATORS, SHOWN ON SHEET 3 OF THE SCHEMATIC, WHICH PROVIDES +5.0 V, -2.0 V, AND ±15 VDC.

11. THE OUTPUTS OF THE REGULATORS ARE ROUTED THROUGH CURRENT SENSE NETWORKS SIMILAR TO THE ONE ON THE -5.2 V SUPPLY AND THEN TO THE OUTPUTS ON THE FILTER BOARD.

G. THE <u>POWER SUPPLY PROTECTION CIRCUITS</u> ARE SHOWN ON <u>SHEET 4</u> OF THE SCHEMATIC.

1. THE SUPPLY IS DESIGNED TO TURN ITSELF OFF IN CASE OF OVER TEMPERATURE, HIGH OR LOW LINE VOLTAGE, PRIMARY OVER CURRENT, OR OVER CURRENT ON ANY OF THE 5 OUTPUT VOLTAGES.

2. THE OUTPUTS OF U3 AND U4 WILL GO HIGH ANY TIME THE CURRENT THROUGH THE SENSE RESISTORS ON THE REGULATED SUPPLIES EXCEEDS THE PRESET THRESHOLDS.

   THIS HIGH IS LATCHED IN U2 AND THEN U5 BY THE 40 KHZ CLOCK FROM THE TL494.

3. U5 PIN 13 GOING HIGH RESETS U6, CAUSING U6 PIN 8 TO GO HIGH FOR .4 SECONDS

4. A HIGH ON ANY OF THE INPUTS OF U11 CAUSES "SUPPLY ENABLE" TO GO FALSE, SHUTTING OFF THE TL494 OUTPUTS.

5. AFTER THE .4 SECOND PULSE GOES AWAY, THE SUPPLY WILL ATTEMPT TO RE-START BUT WILL SHUT DOWN AGAIN IF THE FAILURE STILL EXISTS.

6. WHEN A PRIMARY OVER-CURRENT CONDITION IS DETECTED, U9-1 GOES HIGH SETTING U5-13 HIGH RESETTING U6 WHICH AGAIN ALLOWS THE SUPPLY TO ATTEMPT A RE-START AFTER .4 SEC.

7. U9 PINS 8 & 7 GO LOW FOR INPUT OVER AND UNDER VOLTAGE, RESPECTIVELY.

   EITHER OF THESE GOING HIGH CAUSES U10-3 TO GO HIGH.

8. U10-3 DRIVES U-11 DIRECTLY AS DOES THE OVERTEMPERATURE SENSOR, S1.

   THUS, THERE IS NO AUTOMATIC RE-START ATTEMPT FOR THESE FAILURE CONDITIONS.

H. U10, Q10 AND THEIR ASSCOCIATED COMPONENTS PROVIDE A RESET SIGNAL TO THE MPU IN THE K101 EACH TIME THE SUPPLY SHUTS OFF OR TURNS ON AND WHEN THE POWER IS TURNED OFF.

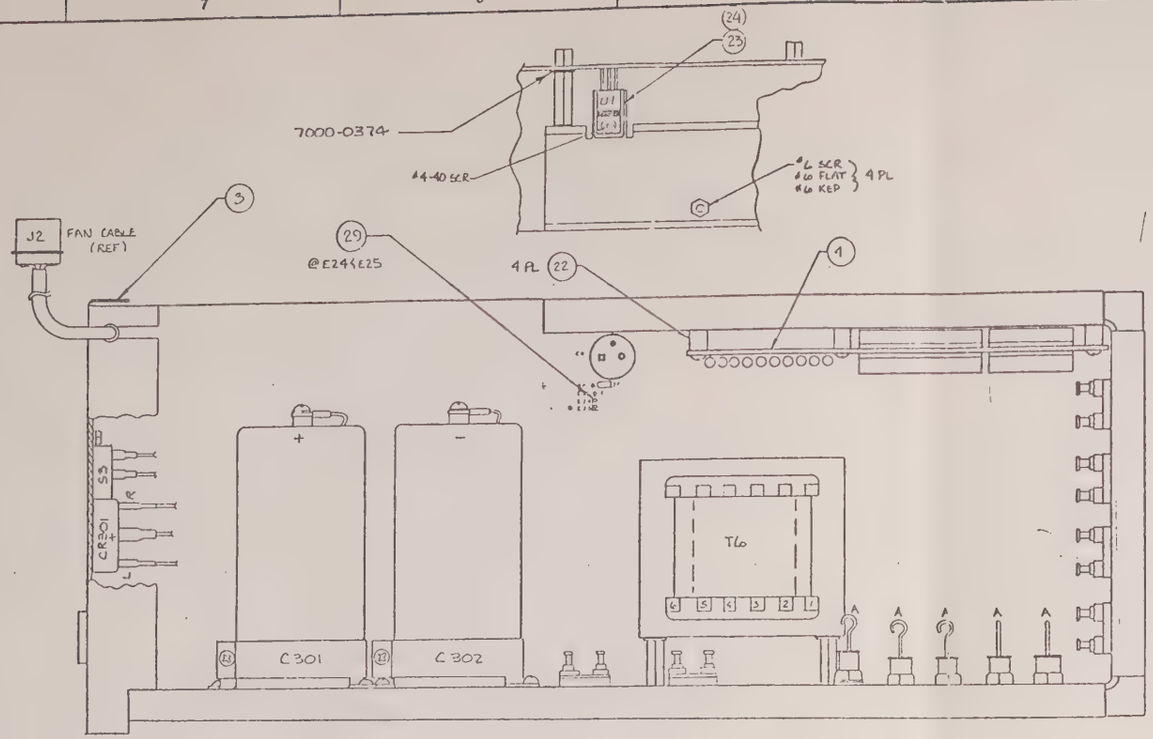
THE K500 DOES NOT USE THIS SIGNAL.

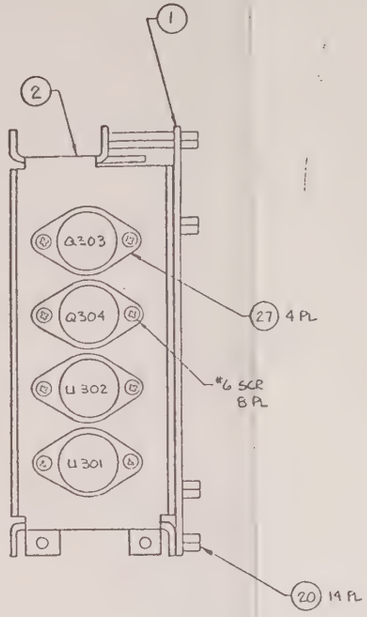
THE K101 USES THE POWER-DOWN RESET TO FASCILITATE SAVING THE CURRENT INSTRUMENT STATUS ON TURN-OFF.

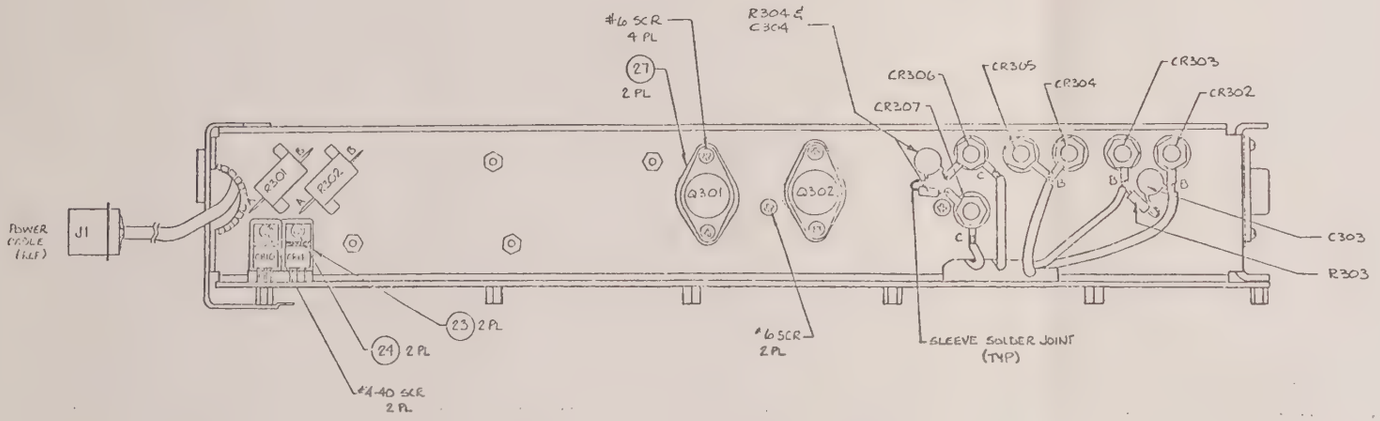
DWG NO	SH	REV
0114-0320	1	G

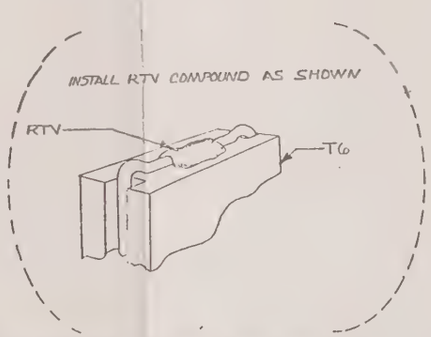
REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B	~	PILOT REL PER ERN 0197	AS	[illegible]	[illegible]
	C	2236	REVISED PER ECO.	AS	RD	[illegible]
	D	2234	REVISED PER ECO.	AR	[illegible]	[illegible]
	E	2327	REVISED PER ECO #	SL	[illegible]	[illegible]
	F	3510	REVISED PER ECO#	JNC	T.J.	[illegible]
	G	4601	REVISED PER ECO	JNC	T.J.	[illegible]









JUL 12 1982

REFERENCE PRINT

CHASSIS ASSY DETAIL

(SEE SHEET 2 FOR COVER ASSY & WIRING)

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
-10	0114-0335	1						
-10	[illegible]	1						
-10	[illegible]	1						

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIM'N ARE AFTER FINISH. DIM'N AND TOLERANCES EXCEPT FINISH SURFACE ROUGHNESS.

TOLERANCE: DIMENSIONAL X = ± ANGLES; XX = ±0.01" ± 1°; XXX = ±0.005"; SURFACE FINISH 125 RMS

DRAWN AS — DATE 9-2-81
CHECKED — DATE
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV — DATE

GOULD biomation

TITLE: TOP ASSY K101/K500 PWR SUPPLY

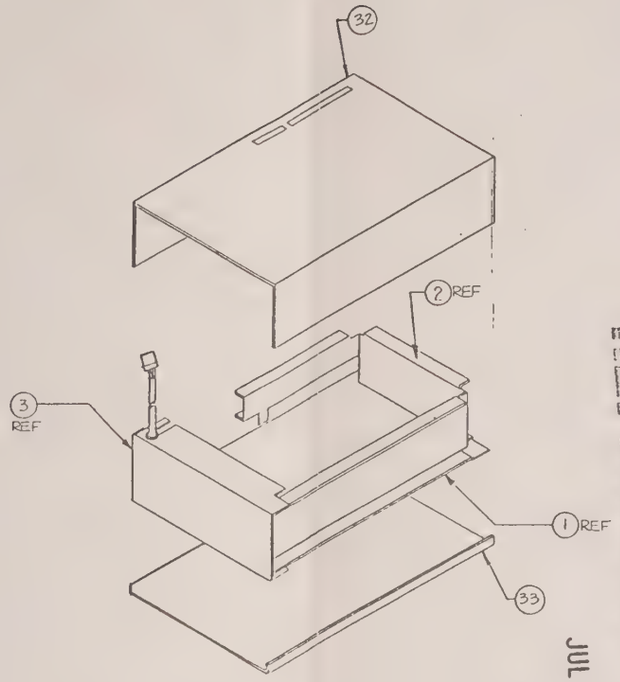
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0320	G

CODE — SHEET 1 OF 2

DWG NO. 0114-0320 SH 2 REV C

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



WIRE LIST

WIRE NO	FROM	TO	DESCRIPTION
1	S3-5	E7 PWR SUPP PWA	BLU/BLK PART OF
2	S3-8	E8	BLU/BLK ITEM 3
3	S3-4	E9	WHT/BRN
4	S3-7	E10	WHT/BRN
5	S3-1	E14	BLK
6	S3-2	E13 PWR SUPP PWA	GRY
7	J1-2	E18 PWR SUPP PWA	WHT/BRN PART OF
8	J1-4	E17 PWR SUPP PWA	BLU/BLK ITEM 3
9	E54 PWR SUPP PWA	CR301 +	YEL
10	E55	CR301 -	BLK PART OF
11	E6	CR301-R (AC)	ORG ITEM 1
12	E15 PWR SUPP PWA	CR301-L (AC)	VIO
13	E50 PWR SUPP PWA	R301-A	BRN
14	E51	R301-B	BRN PART OF
15	E52	R302-A	WHT ITEM 1
16	E53 PWR SUPP PWA	R302-B	WHT
17	E19 PWR SUPP PWA	C301-	BRN PART OF
18	E20	C301+	RED ITEM 1
19	E21	C302-	BRN
20	E22 PWR SUPP PWA	C302+	RED
21	E36 PWR SUPP PWA	CR306-A	WHT/BLK. SOLDER SAME
	E36 PWR SUPP PWA	CR307-A	WIRE 2 PL AS A BRIDGE.
22	E38 PWR SUPP PWA	CR304-B	YEL. SOLDER LUGS {
	E38 PWR SUPP PWA	CR305-B	WIRE AS SINGLE JOINT.
23	E40 PWR SUPP PWA	CR303-A	WHT/RED. SOLDER SAME
	E40 PWR SUPP PWA	CR302-A	WIRE 2 PL AS A BRIDGE.
24	E14 FILTER PWA	E62 PWR SUPP PWA	BRN
25	E13	E66	RED ITEM 10
26	E12 FILTER PWA	E65 PWR SUPP PWA	ORG
27	E9 FILTER PWA	E41 PWR SUPP PWA	BLK
28	E10	E42	BLK
29	E7	E43	BRN ITEM 9
30	E8	E37	YEL
31	E11 FILTER PWA	E44 PWR SUPP PWA	LT BLU
32	E1 FILTER PWA	E33 PWR SUPP PWA	BRN
33	E2	E30	RED
34	E3	E31	ORG
35	E4	E32	YEL ITEM 11
36	E5	E34	LT BLU
37	E6 FILTER PWA	E35 PWR SUPP PWA	GRN
38	T6 (-2V LEAD)	CR303-B	-2V LEADS ARE EITHER
39	T6 (-2V LEAD)	CR302-B	OF TWO FLYING LEADS FROM BOTTOM SIDE OF T6
40	T6 (-5V LEAD)	CR306-C	-5V LEADS ARE EITHER
41	T6 (-5V LEAD)	CR307-C	OF TWO FLYING LEADS FROM TOP SIDE OF T6
42	FILTER-G	E16	GRN. MTD ON FACE PLATE FILTER
43			
44			
45			
46			

PART OF ITEM 1

50	40	30	20	10	SAP NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN 7-7-81 DATE
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
ENG. SERV DATE

GOULD biomation

TITLE TOP ASSY
K101/K500 POWER SUPPLY

SCALE | SIZE D | PART NUMBER 0114-0320 | REV C

CODE SHEET 2 OF 2

JUL 12 1982

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0114-0090	PWR SUPPLY PWA				LM
2						1	0114-0330	HEATSINK ASSY				LM
3						1	0114-0340	FACE PLATE ASSY				LM
4						1	0114-0360	FILTER PWA				LM
5												
6												
7												
8												
9						1	0114-0366	WIRE ASSY			DIGITAL	LM
10						1	0114-0367	WIRE ASSY			ANALOG	LM
11						1	0114-0368	WIRE ASSY			LED	LM
12												
13						2	1400-0039	TRANSISTOR	Q303, Q304		2N4276	
14						1	1700-0089	IC	U302		LM337K	
15						1	1700-0090	IC	U301		LM317K	
16						2	1500-0020	TRANSISTOR	Q301, Q302		HPWR6501/HPWR6502	
17												
18												

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	6-26-81	[illegible]		
B	PILOT REL PER ERN 0197	9/29/81	[illegible]	RG	
C	REVISED PER ECO #2236	12/7/81	MR	RD	
D	REVISED PER ECO # 2234	12/15/81	MR	[illegible]	
E	REVISED PER ECO # 2327		[illegible]	VRD	
F	REVISED PER ECO No 2519	[illegible]	[illegible]	T.J.	
G	REVISED PER ECO No 2607	[illegible]	[illegible]	T.J.	

DASH NO.	NUMBER	QTY
-10	0950-0003	1
-10	0114-0003	1

NEXT ASSEMBLY

		DATE
DRAWN	M Butro	6-26-81
CHECKED	J. Weldon	10-15-81
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
TOP ASSEMBLY
POWER SUPPLY
K101/K500

biomation

B 0114-0320 REV G

MODEL K101-K500 CODE SHEET 1 OF 2

REFERENCE PRINT

JUL 12 19[illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						2	3050-1206	RESISTOR	R303, 304		12Ω ½W 5%	
20						14	7000-0423	STANDOFF			M/F, HEX, 6-32 x ¼	
21						2	4000-0049	CAPACITOR	C303, 304		.01, 1KV ± 20%	
22						4	7000-0152	SPACER			#6 x 5/16 LG	
23						3	7000-0221	SHOULDER WASHER	@ CR10, 11, U1		#4	
24						3	7000-0017	INSULATOR	@ CR10, 11, U1			
25												
26												
27						6	7200-0016	INSULATOR	@ Q301, 302, 303 Q304, U301, U302		TO-3	
28												
29						1	6000-0329	SHORTING PLUG	@ E24 & E25		2 POSITION	
30												
31												
32						1	0114-0327	TOP COVER				FAB
33						1	0114-0328	BOTTOM COVER				FAB
34												
35												
36												

REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN	BS	DATE 6-22-81
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
TOP ASSEMBLY
POWER SUPPLY
K101/K500

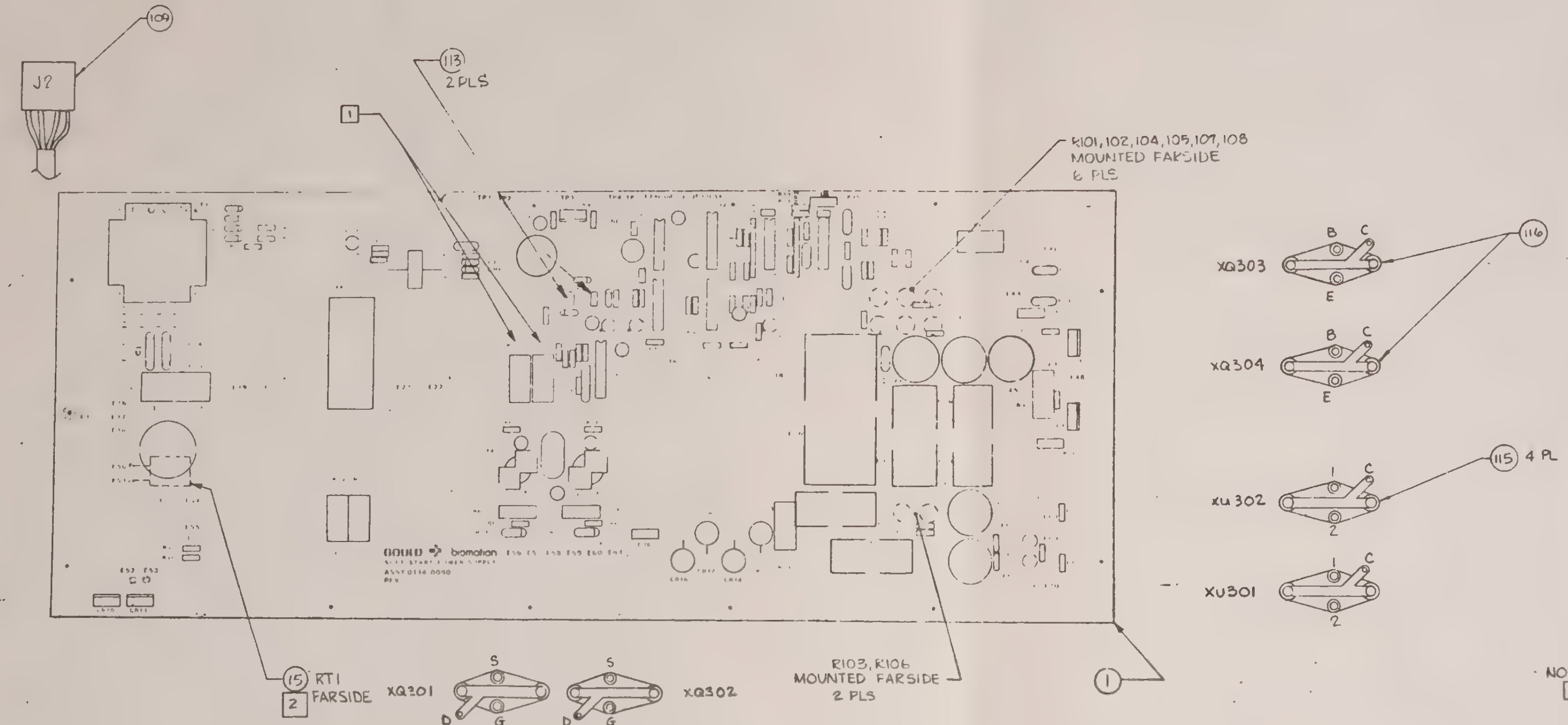
MODEL NOTED

biomation

B	0114-0320	REV G

CODE _____ SHEET 2 OF 2

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	A		[illegible]			
	B		[illegible] PER ERN 0197			
	C		[illegible]			
	D	[illegible]	REVISED PER ECO			
	E	[illegible]	REVISED PER ECO NO			
	F	[illegible]	[illegible]			
	G	[illegible]				
	H	[illegible]	- VOID -			
	J	[illegible]				
	K	[illegible]				
	L	[illegible]				
	M	[illegible]	REVISED PER ECO No			
	N	[illegible]	REVISED PER ECO No	DWC	[illegible]	[illegible]
	P	[illegible]	REVISED PER ECO No	MW	DGW	[illegible]
	R	534	REVISED PER ECO	MW	DGW	[illegible]



NOTES:

1. R8, R9 ARE TO BE MOUNTED WITH 1/4" CLEARANCE BETWEEN RESISTOR BODY AND PCB.
2. WRAP BODY OF RT1 WITH KAPTON TAPE. INSTALL ON SOLDER SIDE FLUSH AGAINST PCB.

NEW ISSUE
DATE JUN 1 1981

FROM	TO	COLOR	AWG	REMARKS	ITEM NO.
E56	XU301-S	ORG	18	3.0"	93
E57	XQ301-G	YEL	18	3.0"	97
E58	XQ301-D	RED	18	2.5"	99
E59	XQ302-S	ORG	18	3.5"	93
E60	XQ302-G	YEL	18	3.0"	97
E61	XQ302-D	RED	18	3.25"	98
E63	XU301-2	VIO	18	2.75"	99
E69	XU301-1	RED	18	3.0"	100
E70	XU301-C	BRN	18	2.75"	91
E64	XU302-C	RED	18	4.0"	[illegible]
E67	XU302	[illegible]	18	[illegible]	[illegible]
E68	XU302-2	VIO	18	[illegible]	[illegible]

FROM	TO	COLOR	AWG	REMARKS	ITEM NO
E46	XQ303-C	[illegible]	12	2.5"	[illegible]
E47	XQ303-B	ORG	[illegible]	[illegible]	[illegible]
E39	XQ303-E	[illegible]	12	[illegible]	[illegible]
E48	XQ304-E	BLU	[illegible]	[illegible]	[illegible]
E49	XQ304-B	YEL	18	[illegible]	107
E45	XQ304-C	TAN	12	[illegible]	112
J2-1	E2	BLK	22		109
J2-2	E3	TAN	22		
J2-3	E4	BLK	22		
J2-4	E5	TAN	22		
E54	N.C.	YEL	18		[illegible]
E55	N.C.	BLK	18		[illegible]
E[illegible]	N.C.	ORG	18		[illegible]
E15	N.C.	[illegible]	18		105

FROM	TO	COLOR	AWG	REMARKS	ITEM NO.
E36	N.C.	WHT/BLK	[illegible]	[illegible]	96
E38		YEL	[illegible]	[illegible] 4/ [illegible]	95
E40		WHT	12	[illegible] 3	[illegible]
E50	N.C.				
E51	N.C.				
E52	N.C.	[illegible]	18	4.0"	92
E53	N.C.	[illegible]	18	[illegible]	94
E19	N.C.	[illegible]	18		102
E20	N.C.	[illegible]	18		
E21	N.C.	[illegible]	18		103
[illegible]	N.C.	[illegible]	18		

DO NOT SCALE DRAWING

GOULD biomation

TITLE: ASSY PCB [illegible]

SCALE | SIZE D | PART NUMBER 0114-0090 | REV R

1						1	0114-0092	PWB				FAB
2												
3						4	1000-0002	DIODE	CR 5,6,8,9		IN4152	
4												
5						2	1100-0046	" "	CR 14 & 15		P6KE22A	
6						4	1200-0001	" "	CR 1-4		IN 4002	
7						1	1100-0006	" "	CR7		IN758A	
8						4	1200-0042	RECTIFIER	CR16,17,18,19		MR821	
9												
10												
11						2	1300-0028	TRANSISTOR	Q 2 & 3		2N3904	
12												
13						2	1400-0026	TRANSISTOR	Q4, 5		2N6134	
14						1	1400-0019	TRANSISTOR	Q1		2N3906	
15						2	3600-0001	THERMISTOR	RT 1 & 2			
16						1	1700-0047	IC	U1		LM 340T-15	
17												
18						2	1700-0086	IC	U5 & 6		LM 324	

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
B	PILOT REL PER ERN 0197	9/27/81	RG	[illegible]	
C	REVISED PER ECO # 2234	1/15/82	[illegible]	[illegible]	1/15/82
D	REVISED PER ECO # 2421	3/16/82	[illegible]	[illegible]	
E	REVISED PER ECO Nº 2519	7-23-[illegible]	[illegible]	[illegible]	
F	REVISED PER ECO # 2568	4-2[illegible]	[illegible]	[illegible]	
G	" " " 2634	9-8-82	DGW	[illegible]	
H	-VOID- ECO 2666	9-8-82	DGW	[illegible]	

DASH NO.	NUMBER	QTY
-10	0114-0320	1

NEXT ASSEMBLY

		DATE
DRAWN	J.W. CARROLL	6-22-81
CHECKED	[illegible]	10-15-8
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

biomation

B 0114-0090 REV R

MODEL

CODE

SHEET 1 OF 7

19						1	1820 0034	IC	U4		74C1[illegible]		
20						1	1820-0007	IC	U3		14025		
21						2	1820-0022	IC	U7,8		14093		
22						1	1700-0095	IC	U2		TL494		
23						1	3000-4700	RESISTOR	R109		470Ω, 1/4W, 5%		
24						10	3000-1002	RESISTOR	R4,10,15,16,17,25 29,39,41,24		10K 1/4w 5%		
25						8	3000-1003	RES	R2,3,13,18,19, 20,22,23		100K		
26						3	3000-2200	RES	R40,53,55		22Ω		
27						2	3000-2006	RES	R61 & 64		20Ω		
28						2	3000-3900	RES	R63,66		390Ω		
29						1	3000-1802	RES	R30		18K 1/4W, 5%		
30						1	3100-1872	RES	R11		18.7K 1/8W, 1%		
31						4	3000-6804	RES	R5,32,33,34		6.8M 1/4W, 5%		
32						1	3000-4706	RES	R74		47Ω 1/4W, 5%		
33						2	3000-4701	RES	R7,38		4.7K 1/4W, 5%		
34						1	3000-5601	RES	R44		5.6K 1/4W, 5%		
35						1	3100-2002	RES	R12		20K 1/8W, 1%		
36						4	3000-5101	RES	R28,31,46,48		5.1K 1/4w 5%		

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	J	REVISED PER ECO 2709	9-8-82	DGW	[illegible]	
	K	" " " 2717	9-8-82	DGW	[illegible]	
	L	" " " 2741	9-8-82	DGW	[illegible]	
	M	" " " 2738	9-9-82	[illegible]	[illegible]	
	N	REVISED PER ECO No 3575	3-10-83	[illegible]	[illegible]	
	P	REVISED PER ECO No 3578A	3/31/83	[illegible]	DGW	3/31
	R	REVISED PER ECO 3734	4/31/83	[illegible]	DGW	4/1/83

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

PW ASSEMBLY

SOFT START POWER SUPPLY

biomation

MODEL	CODE	SHEET 2 OF 7
	B	0114-0090 REV R

37						1	3000-02	RES	R110		12K, 1/4 5%		
38						3	3000-1502	RES	R27, 36, 45		15K 1/4W 5%		
39						1	3000-1503	RES	R26		150K 1/4W 5%		
40						1	3150-2942	RES	R14		29.4K 1% 1/4W		
41						1	3000-9101	RES	R42		9.1K 1/4W 5%		
42						2	3000-2002	RES	21, 75		20K 1/4W 5%		
43						1	3000-1203	RES	R37		120K 1/4W 5%		
44						2	3070-4700	RES	R62, 65		470Ω 1W 5%		
45						1	3050-3306-10	RES	R6		33Ω 1/2W 5%		
46						2	3100-1581	RES	R70, 71		1.58K 1/8W 1%		
47						2	3100-1500	RES	R72, 73		150Ω 1/8W 1%		
48						1	3080-2706	RESISTOR	R49		27Ω 2W		
49						1	3080-5106	RESISTOR	R68		51Ω 2W		
50						1	3050-2006	RESISTOR	R52		20Ω 1/2W		
51						1	3050-8200	RESISTOR	R35		820. 1/2W 5%		
52						1	3050-1007	RESISTOR	R56		1Ω 1/2W		
53						2	3080-5602	RESISTOR	R59, 60		56K 2W 5%		
54						1	3080-2206	RESISTOR	R54		22Ω 2W		

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

biomation

B	0114-0090	REV R
MODEL	CODE	SHEET 3 OF 7

55						5	3300-0005	POT	R101, 102, 103, 106 108		200 Ω .W, 10%	
56						3	3300-0068	POT	R104, 105, 107		5K, 1/2W, 10%	
57						2	3080-3000	RESISTOR	R 8, 9		300 Ω 2W	
58						1	3700-0078	RESISTOR PAK	RP1		100K 8 PIN	
59						1	3700-0077	RESISTOR PAK	RP2		4.7K 8 PIN	
60						1	4000-0009	CAPACITOR	C4		.1 uf, 100V	
61						1	0114-0336-10	RESISTOR COIL	R50		3 mΩ	
62						1	0114-0336-20	RESISTOR COIL	R51		1.9 mΩ	
63						1	0114-0336-30	RESISTOR COIL	R43		1.2 mΩ	
64						1	4300-0028	CAPACITOR	C15		100uf 20V	
65						2	4000-0058	CAPACITOR	C1, C2		.01 UF, 3KV, 20%	
66						2	4000-0005	CAPACITOR	C5, 28		.01uf, 50V, 20%	
67						1	4100-0050	CAPACITOR	C33		3300pf, 500V, 5%	
68						7	4000-0025	CAPACITOR	C7, 8, 39, 40, 43, 23, 24		.1uf, 50V, 20%	
69						2	4300-0037	CAPACITOR	C41, 42		1.0, 35V, 20%	
70						7	4010-0104	CAPACITOR	C3, 14, 19, 22, 25, 16, 26		.1uf 50V, 10%	
71						1	4100-0018	CAPACITOR	C21		330 pf, 500V, 5%	
72						1	4200-0042	CAPACITOR	C45		22 uf 450V	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

biomation

B	0114-0090	REV R
MODEL	CODE	SHEET 4 OF 7

73						1	4000 .050	CAP	C36		.005µf 50V	
74						1	4100-0015	CAP	C11		.001µF 5% 100V	
75						1	4400-0055	CAP	C9		1500 µf 35V	
76						5	4300-0024	CAP	C12, 17, 18, 32, 35		4.7µf 50V	
77						3	4400-0054	CAP	C29, 30, 31		1000µf 15V	
78						3	4300-0015	CAP	C6, 13, 34		15 µf, 20 V	
79						2	4400-0052	CAP	C37, 38		470 µf 50V	
80						1	4200-0036	CAP	C44		6µF 200V	
81						1	9000-0108	ASSY OUTPUT INDUCTOR #2	L5		45µH (+6V)	LM
82						1	6400-0052	NEON LAMP	DS1		NE 2	
83						1	9000-0118	ASSY. MAIN TRANSFORMER	T6		"SOFT START"	LM
84						1	2500-000-20	TRANSFORMER	T1		LINE 110/220 PRI	
85						1	9000-0081	ASSY INPUT TRANSFORMER	T3		BALUN INPUT	LM
86						1	9000-0078	ASSY TRANSFORMER	T2		CURRENT SENSING XFMR	LM
87						1	9000-0079	ASSY OUTPUT INDUCTOR	L4		45uH (-3v)	LM
88						2	9000-0107	ASSY OUTPUT INDUCTOR #1	L2, 3		250µH (±17v)	LM
89						1	9000-0111	ASSY OUTPUT INDUCTOR #3	L1		20µH (-5.2v)	
90						2	9000-0109	TRANSFORMER	T4, 5		GATE DRIVE	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

biomation

B	0114-009	REV R
MODEL	CODE	SHEET 5 OF 7

91						AR	7150-001[illegible] 01	WIRE				BRN. 1[illegible]	AWG	—
92							7150-0018-09					WHT 18	AWG	—
93							7150-0018-03					ORN 18	AWG	—
94							7150-0012-15					WHT/RED 12	AWG	—
95							7150-0012-04					YEL 12	AWG	—
96							7150-0012-14					WHT/BLK 12	AWG	—
97							7150-0018-04					YEL 18	AWG	—
98							7150-0018-02					RED 18	AWG	—
99							7150-0018-07					VIO 18	AWG	
100							7150-0018-06					BLU 18	AWG	
101						AR	7150-0018-08	WIRE				GRY 18	AWG	
102						2	0114-0335-10	CAP CABLE ASSY				BRN		LM
103						2	0114-0335-20	" "				RED		LM
104						1	0114-0325-10	ASSY, BRIDGE WIRE				ORG		LM
105						1	0114-0325-20	" "				YEL		LM
106						1	0114-0325-30	" "				VIO		LM
107						1	0114-0325-40	" "				BLK		LM
108						AR	7150-0012-03	WIRE				ORG 12	AWG	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

biomation

B	0114-0090	PFV R
MODEL	CODE	SHEET 6 OF 7

109						1	0114-_-29	CABLE ASSY FAN	J2		BLK, JV	LM
110						AR	7150-0012-02	WIRE			RED 12 AWG	
111						AR	7150-0012-06	↓			BLUE 12 AWG	
112						AR	7150-0012-01	WIRE			BRN 12 AWG	
113						2	6000-0298	HEADER			3 PIN	
114						1	4010-0103	CAP.	C27		.01uf 50V 10%	
115						4	6100-0149	SOCKET	XQ301, XQ302 XU301, XU302		TO3 MOUNTING WITH .040 TERMINALS	
116						2	6100-0150	SOCKET	XQ303, XQ304		TO3 MOUNTING WITH .060 TERMINALS	
117												
118												
119						A/R	7200-0046	TEFLON TUBING	T2		20 AWG	
120						A/R	7100-0099	WIRE	T2		20 AWG	
121						1	4010-0563	CAP	C10		.056uF 50v 10%	
122												
123												
124												
125												
126												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

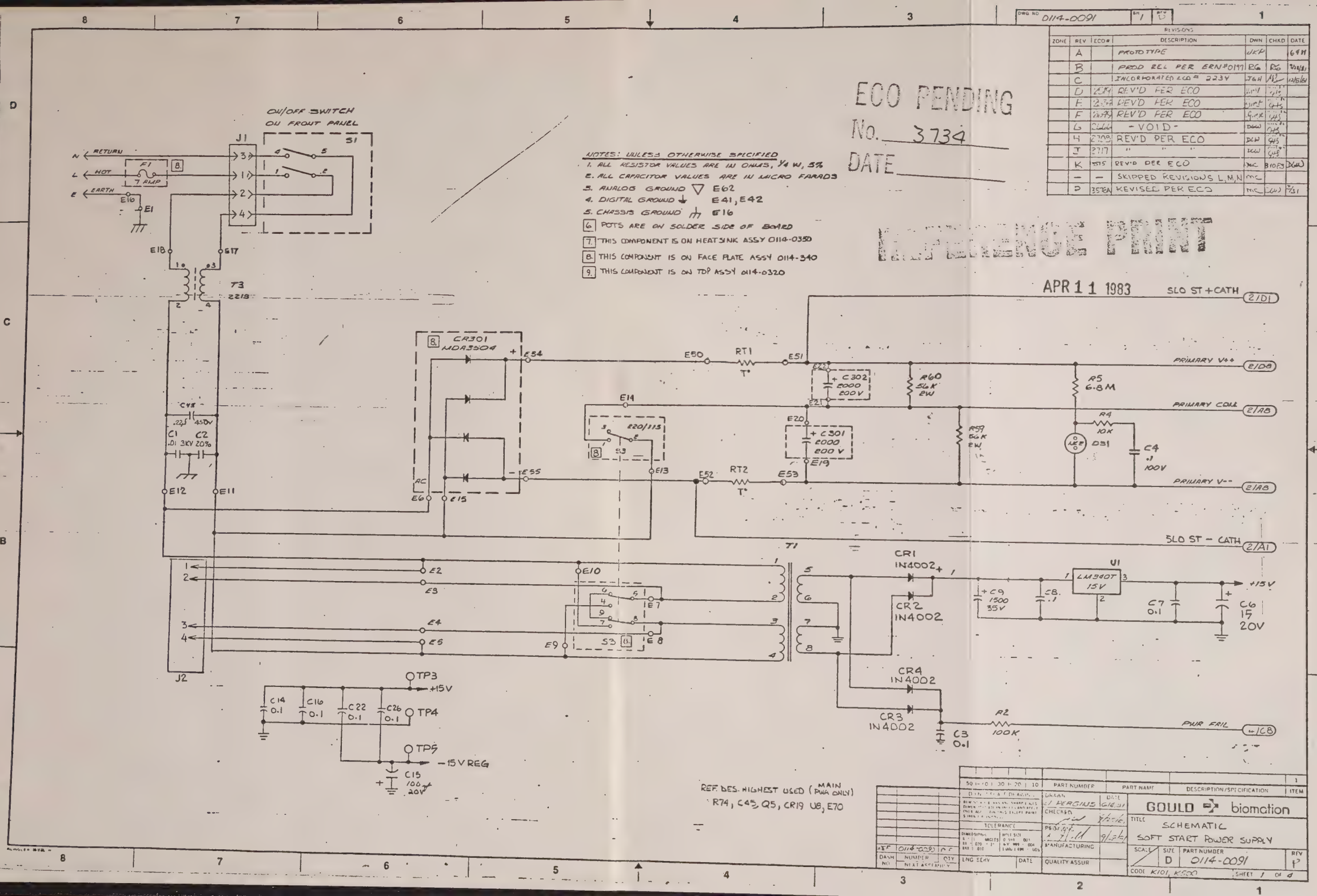
LIST OF MATERIAL

PW ASSEMBLY
SOFT START POWER SUPPLY

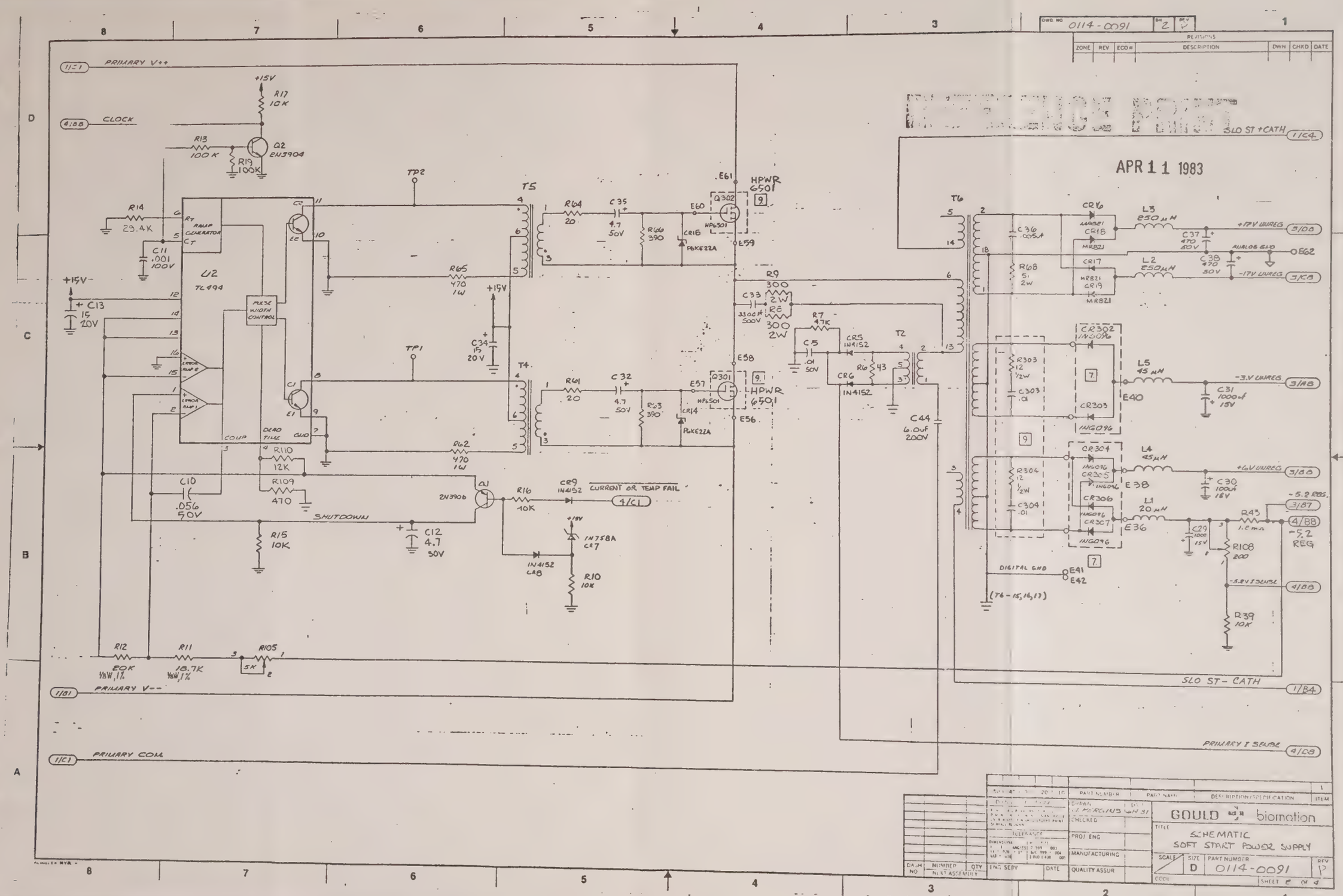
MODEL

biomation

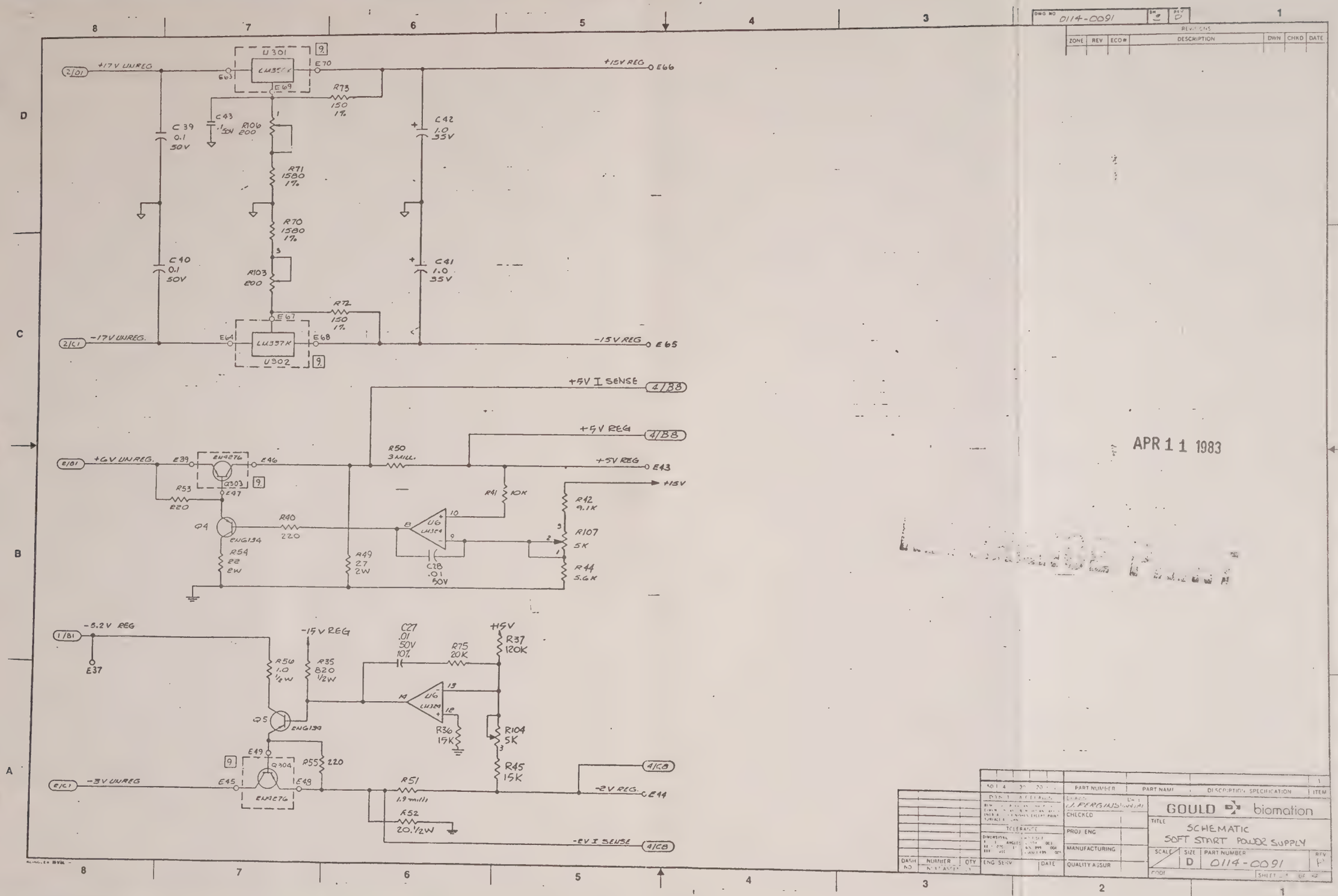
B	0114-0090	REV R
CODE		SHEET 7 OF 7



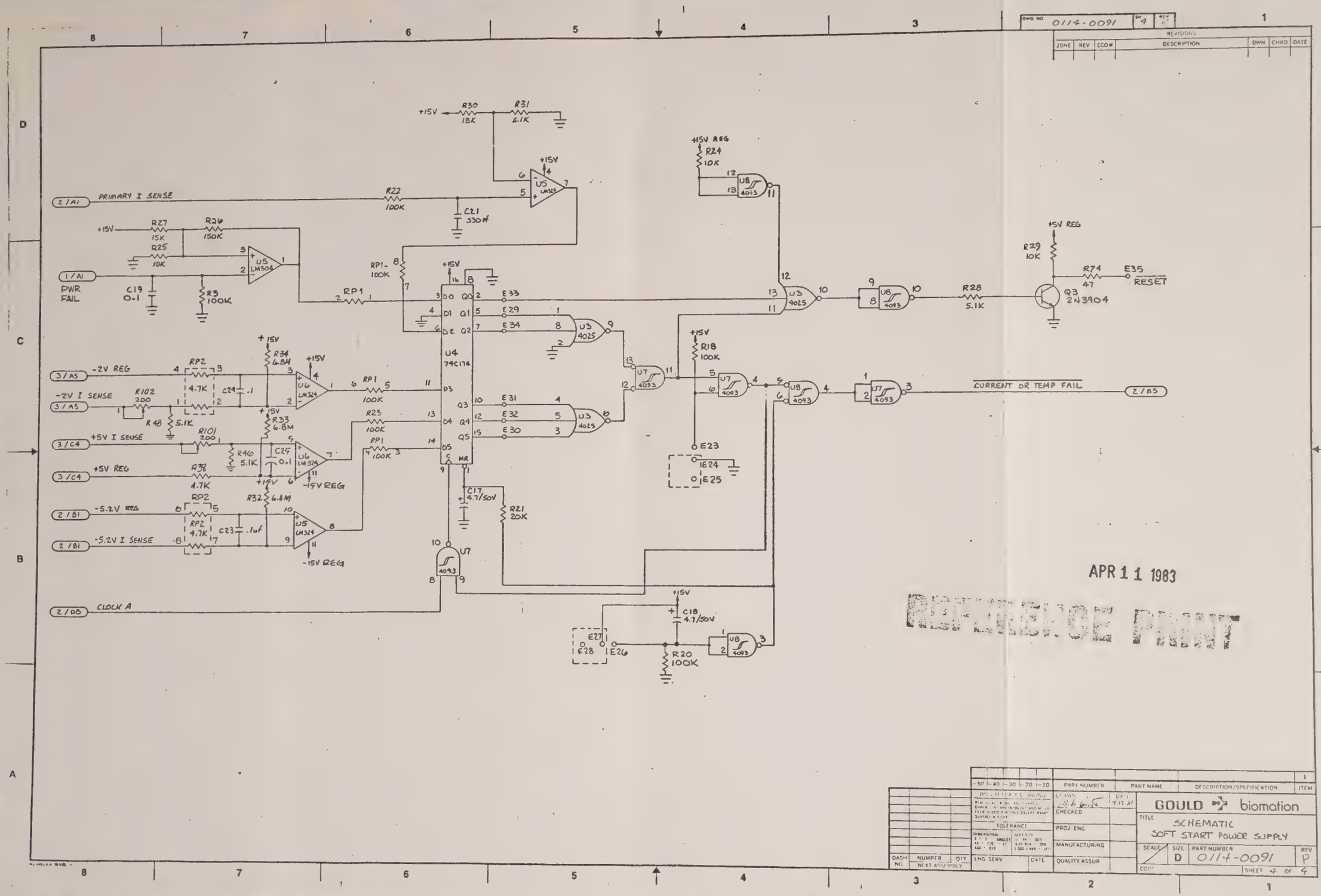
DWG NO 0114-0091
SH 1
REV D
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
A | PROTOTYPE | JKP | | 6/4/81
B | PROD REL PER ERN#0197 | RG | RG | 12/4/81
C | INCORPORATED ECO# 223Y | JGH | | 12/5/81
D | REV'D PER ECO
E | REV'D PER ECO
F | REV'D PER ECO
G | -VOID-
H | 2709 | REV'D PER ECO | DGW | GHS
J | 2717 | " " " | DGW | GHS
K | 3575 | REV'D PER ECO | MC | 810 83 | DGW
— | — | SKIPPED REVISIONS L,M,N | MC
P | 3576A | REVISED PER ECO | MC | DGW | 3/31
ECO PENDING
No. 3734
DATE
REFERENCE PRINT
APR 11 1983
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS
3. ANALOG GROUND E62
4. DIGITAL GROUND E41, E42
5. CHASSIS GROUND E16
6. POTS ARE ON SOLDER SIDE OF BOARD
7. THIS COMPONENT IS ON HEATSINK ASSY 0114-0350
8. THIS COMPONENT IS ON FACE PLATE ASSY 0114-340
9. THIS COMPONENT IS ON TOP ASSY 0114-0320
ON/OFF SWITCH ON FRONT PANEL
J1
S1
RETURN
HOT
EARTH
F1 7 AMP
T3 2218
CR301 MDA3504
220/115
S3
RT1
RT2
C302 2000 200V
C301 2000 200V
R60 56K 2W
R59 56K 2W
R5 6.8M
R4 10K
D31
C4 .1 100V
SLO ST + CATH 2/D1
PRIMARY V++ 2/D8
PRIMARY COM 2/A8
PRIMARY V-- 2/A8
SLO ST - CATH 2/A1
T1
CR1 1N4002
CR2 1N4002
CR3 1N4002
CR4 1N4002
U1 LM340T 15V
C9 1500 35V
C8 .1
C7 0.1
C6 15 20V
+15V
PWR FAIL 4/C8
J2
TP3 +15V
TP4
TP5 -15V REG
C14 0.1
C16 0.1
C22 0.1
C26 0.1
C15 100 20V
REF DES. HIGHEST USED (MAIN PWA ONLY)
R74, C45, Q5, CR19 U8, E70
DRAWN J. PERGINS
CHECKED
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC SOFT START POWER SUPPLY
SCALE
SIZE D
PART NUMBER 0114-0091
REV P
CODE K101, K500
SHEET 1 OF 4



DWG NO 0114-0091
SH 2
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
APR 11 1983
PRIMARY V++
CLOCK
SLO ST +CATH
PRIMARY V--
PRIMARY COM
PRIMARY I SENSE
SLO ST- CATH
+17V UNREG
-17V UNREG
-3.V UNREG
+6V UNREG
-5.2 REG
ANALOG GND
DIGITAL GND
CURRENT OR TEMP FAIL
SHUTDOWN
U2
TL494
PULSE WIDTH CONTROL
RAMP GENERATOR
ERROR AMP 2
ERROR AMP 1
COMP
DEAD TIME
GND
T5
T4
T6
T2
HPWR 6501
Q302
Q301
2N3904
2N3906
R17 10K
R13 100K
R19 100K
R14 29.4K
C11 .001 100V
C13 15 20V
C10 .056 50V
R15 10K
R12 20K
R11 18.7K
R105 5K
R110 12K
R109 470
C12 4.7 50V
R16 10K
R10 10K
R65 470 1W
R62 470 1W
C34 15 20V
R64 20
C35 4.7 50V
R66 390
R61 20
C32 4.7 50V
R63 390
R9 300 2W
R8 300 2W
C33 3300pf 500V
R7 4.7K
C5 .01 50V
R6 43
C44 6.0uf 200V
L3 250 μH
L2 250 μH
L5 45 μH
L4 45 μH
L1 20 μH
C37 470 50V
C38 470 50V
C31 1000uf 15V
C30 100uf 15V
C29 1000 15V
R43 1.2 mΩ
R108 200
R39 10K
R68 51 2W
C36 .005uf
R303 12 1/2W
C303 .01
R304 12 1/2W
C304 .01
CR16 MR821
CR18 MR821
CR17 MR821
CR19 MR821
CR302 1N6096
CR303 1N6096
CR304 1N6096
CR305 1N6096
CR306 1N6096
CR307 1N6096
E40
E38
E36
E41
E42
E61
E60
E59
E58
E57
E56
E62
(T6-15,16,17)
GOULD biomation
TITLE SCHEMATIC SOFT START POWER SUPPLY
SIZE D
PART NUMBER 0114-0091
REV P
SHEET 2 OF 4

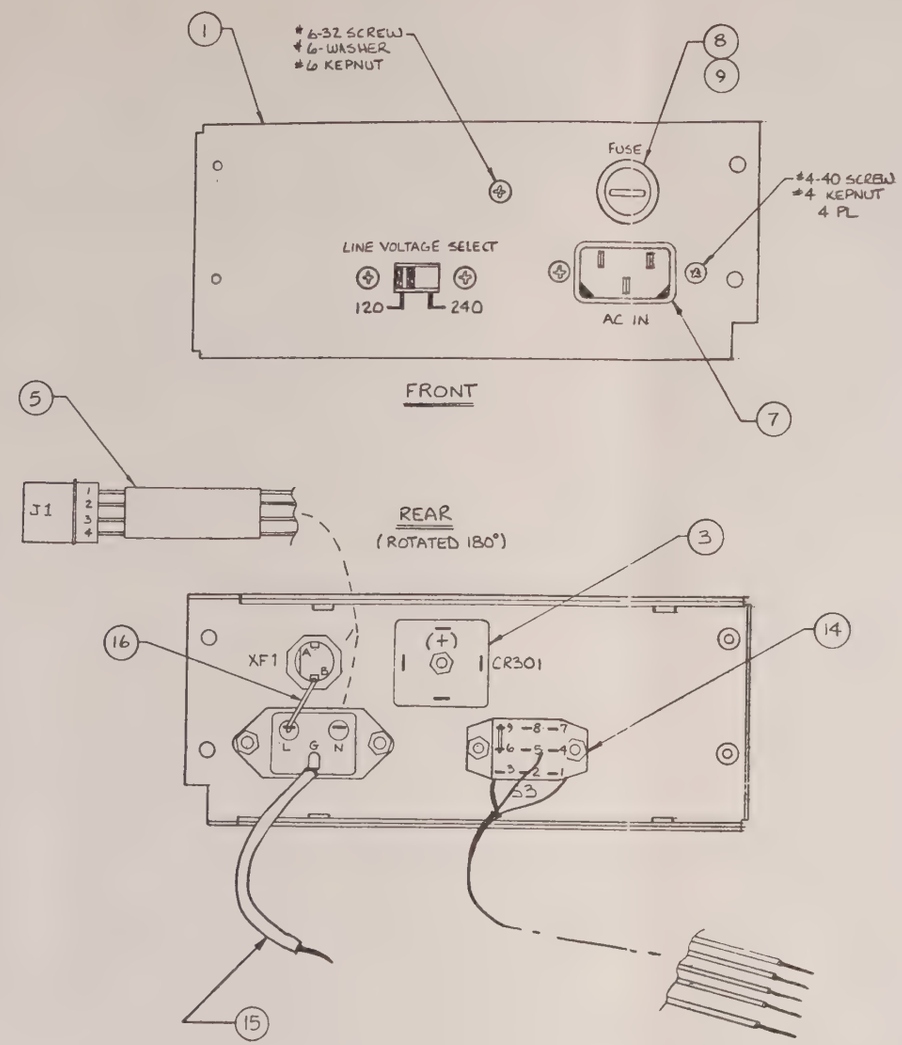


DWG NO 0114-0091
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
+17V UNREG
U301
LM350K
E70
E69
E63
+15V REG E66
R73 150 1%
C43 .1 50V
R106 200
C39 0.1 50V
C42 1.0 35V
R71 1580 1%
R70 1580 1%
C40 0.1 50V
C41 1.0 35V
R103 200
R72 150 1%
E67
-17V UNREG.
E64
LM337K
E68
U302
-15V REG E65
+5V I SENSE 4/B8
+5V REG 4/B8
+6V UNREG.
E39
2N4276
E46
Q303
E47
R50 3 MILL.
+5V REG E43
+15V
R53 220
R41 10K
R42 9.1K
Q4
2N6134
R40 220
U6 LM324
R107 5K
R54 22 2W
R49 27 2W
C28 .01 50V
R44 5.6K
-5.2V REG
E37
-15V REG
C27 .01 50V 10%
R75 20K
+15V
R37 120K
R56 1.0 1/2W
R35 820 1/2W
Q5
2N6134
R36 15K
R104 5K
E49
Q304
R55 220
R45 15K
-3V UNREG
E45
E48
2N4276
R51 1.9 mills
-2V REG. E44
4/C8
R52 20 1/2W
-2V I SENSE 4/C8
APR 11 1983
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
DRAWN J. FERGINS
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
TOLERANCE
DASH NO
NUMBER
QTY
GOULD biomation
TITLE
SCHEMATIC
SOFT START POWER SUPPLY
SCALE
SIZE D
PART NUMBER 0114-0091
REV F
CODE
SHEET



DWG NO 0114-0091
SH 4
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
PRIMARY I SENSE
PWR FAIL
-2V REG
-2V I SENSE
+5V I SENSE
+5V REG
-5.2V REG
-5.2V I SENSE
CLOCK A
CURRENT OR TEMP FAIL
RESET
U4 74C174
U5 LM324
U6 LM324
U3 4025
U7 4093
U8 4093
Q3 2N3904
APR 11 1983
REFERENCE PRINT
GOULD biomation
TITLE SCHEMATIC SOFT START POWER SUPPLY
SIZE D
PART NUMBER 0114-0091
REV P
SHEET 4 OF 4

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	–	PROTOTYPE	MB		
	B		PILOT REL PER ERN 0197	R	JGH	9/29/81



WIRING LIST

FROM	TO	COLOR		REMARKS
XF1-B	FILTER-L	BRN		ITEM 16
J1-1	XF1-A	WHT/BRN		ITEM 5
J1-3	FILTER-N	BLU/BLK		
J1-2	N.C.	WHT/BRN		
J1-4	N.C.	BLU/BLK		
S3-6	S3-9	BUSS		ITEM 10
S3-5	N.C.	BLU/BLK		ITEM 6
S3-8		BLU/BLK		
S3-4		WHT/BRN		
S3-7		WHT/BRN		
S3-1		BLK		
S3-2		GRY		
FILTER-G		GRN		ITEM 15

NOTES: UNLESS OTHERWISE SPECIFIED,

1. SLEEVE CONNECTIONS AS REQD.

DASH NO.	NUMBER	QTY
-20	0114-0320	1
-10	0114-0320	1

NEXT ASSEMBLY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X = .1 ANGLES; .XX = .020 ± 1°; .XXX = .010

HOLE SIZE: 0.599 - .003; 600.999 ± .004; 1.000-1.499 - .005

ENG. SERV. | DATE

DRAWN: [signature] | DATE: 3-10-81

CHECKED: [signature] | 10-15-81

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: FACE PLATE ASSY, PWR SUPPLY

SCALE: 1/1 | SIZE: C | PART NUMBER: 0114-0340 | REV: B

CODE | SHEET 1 OF 1

DWG NO 0114-0340 | SH 1 | REV B

KLINGLER K-VEL H

LIST OF MATERIAL

ITEM				QTY	QTY	PART NO.	NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
								CR301	[illegible]	400V 35A	
5				1	/	0114-0343	WIRE ASSY			POWER CABLE	LM
6				1	/	[illegible]	WIRE ASSY			LINE VOLTAGE SELECT	LM
7				1	/	6000-0047	PWR LINE FILTER				
8				1	/	7300-0011	FUSE HOLDER SOCKET	XF1			
9				1	/	7300-0019	BAYONET CAP				
10				AR	AR		WIRE, BUSS			22 AWG	
11				—	/	7300-0029		F1		7A-3AG-125 V	
12				1	—	7300-0020-10		F1		4A-3AG-250V	
13											
14				1	/	6700-0035	SWITCH, SLIDE	S3		3PDT	
15				AR	AR	7150-0018-05	WIRE			18 AWG GRN	
16				A/R	A/R	7150-0018-01	WIRE			18AWG BRN	
17											
18											

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	6-?-?			
B	PILOT REL PER ERN 0197	9/3/81	RG	JGH	

DASH NO.	NEXT ASSEMBLY NUMBER	QTY
-10	0114-0320	1

DRAWN MLS DATE 6-?-?
CHECKED [illegible] 10-15-81
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL

FACE PLATE ASSY POWER SUPPLY

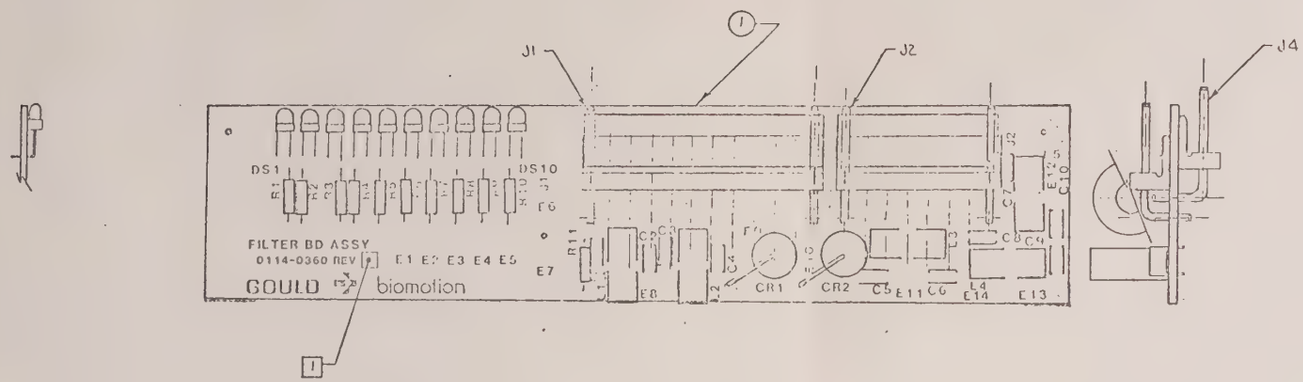
MODEL

biomation

CODE B — 0114-0340 — REV B

SHEET 1 OF 1

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	PROTO			
	B	—	PILOT REL. PER ERN #0197			
	C	7327	REVISED PER ECO#			
	D	2543	REVISED PER ECO			



NOTES: UNLESS OTHERWISE SPECIFIED-
1. MARK LATEST REVISION LETTER WHERE SHOWN.
2. SCHEMATIC REF: 0114-0361.

REFERENCE PRINT

APR 16 1982

DASH NO	NUMBER	QTY
-10	0114-0320	1

NEXT ASSEMBLY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: 0.599 ± .003, 630.999 ± .004, 1.000 ± .999 ± .005

ENG SERV. | DATE

DRAWN: WELDON | DATE: 8-6-82

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: ASSY, FILTER, BD, PWR SUPPLY

SCALE | SIZE: D | PART NUMBER: 0114-0360 | REV: D

CODE | SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0114-0362	FILTER PWB				FAB
2												
3						2	1200-0017	RECTIFIER	CR1, CR2		MR751	
4												
5						2	3000-4700	RESISTOR	R3,4		470Ω 1/4W 5%	
6						2	3000-1006	"	R5,11		10Ω 1/4W 5%	
7						5	3000-2701	"	R6,10		2.7K 1/4W 5%	
8						2	3000-1501	"	R1,2		1.5K 1/4W 5%	
9												
10						10	4000-0025	CAP	C1-10		.1uf CERAMIC 50V 20%	
11						2	6000-0351-08	HEADER	J2,4		8 PIN RT. ANGLE	
12						2	6000-0351-12	HEADER	J1,J3		12 PIN RT. ANGLE	
13						5	6400-0039	LED	DS6-10		RED	
14						5	6400-0041	LED	DS1-5		GREEN	
15												
16						5	9000-0074	INDUCTOR	L1-L5			LM
17												
18												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PROTOTYPE	6-26-81	MB		
	B	PROTOTYPE - REVISED	9-8-81	MB	JGH	9/29/81
	C	REVISED PER ECO 2327			RD	2/4/82
	D	REVISED PER ECO 2543	4-14-82	JCW		

DASH NO.	NUMBER	QTY
-10	0114-0320	1
	NEXT ASSEMBLY	

		DATE
DRAWN		6-26-81
CHECKED		10-15-81
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL
FILTER PW ASSY
POWER SUPPLY

biomation

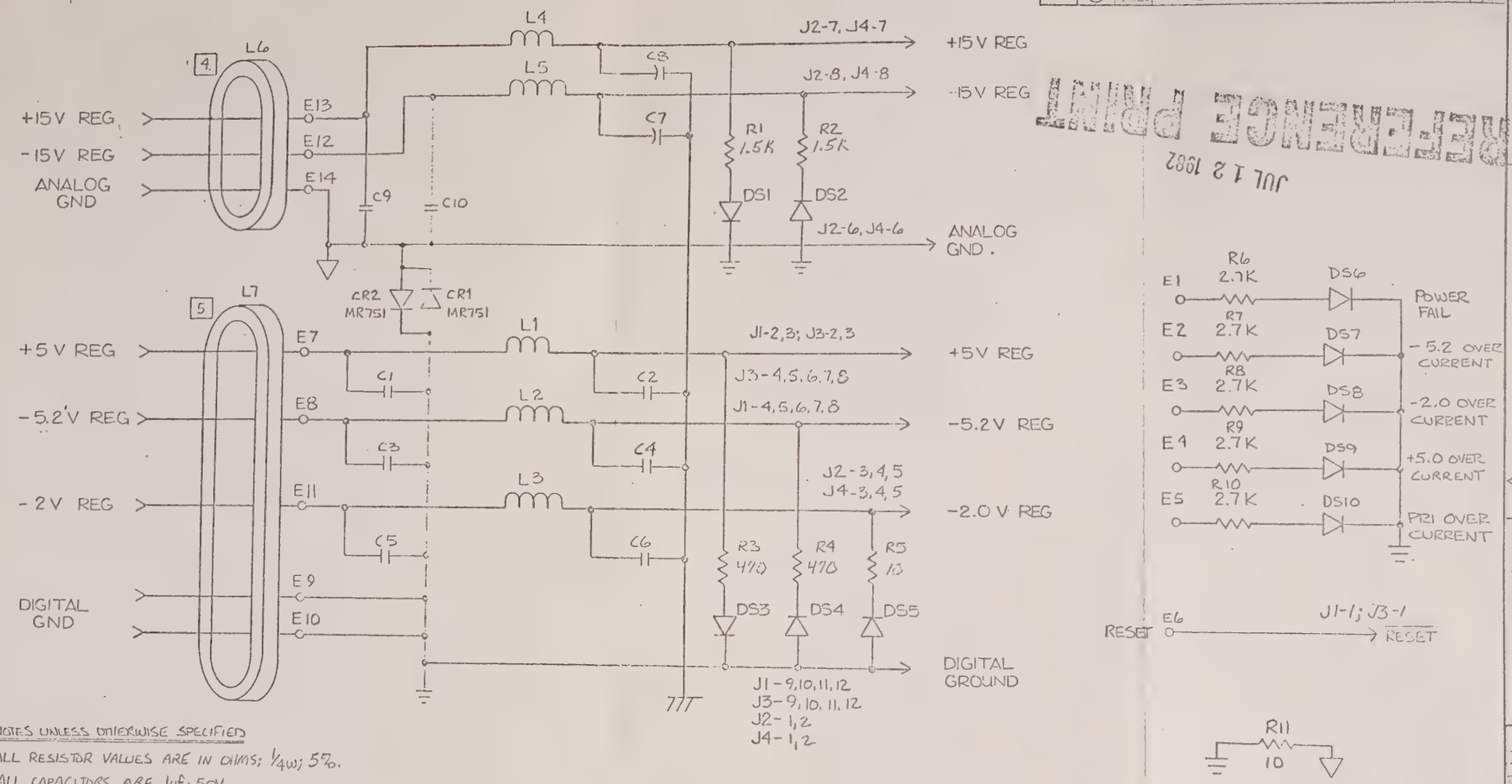
B	0114-0360	REV D.

MODEL K101-K500 | CODE | SHEET 1 OF 1

REFERENCE PRINT

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTOTYPE	[illegible]		[illegible]
	B		PILOT REL PER ERN 0197	[illegible]	[illegible]	[illegible]
	B	2625	REV'D PER ECO		T.J.	[illegible]

REFERENCE PRINT
JUL 12 1982



NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS; 1/4W; 5%.
2. ALL CAPACITORS ARE .1uf; 50V
3. LED'S DS1-5 ARE GREEN, DS6-10 ARE RED.
4. L6 IS ON ANALOG WIRE ASSY 0114-0367.
5. L7 IS ON DIGITAL WIRE ASSY 0114-0366.
6. ANALOG GROUND ▽ E14
7. DIGITAL GROUND ⏚ E9,10
8. CHASSIS GROUND ///

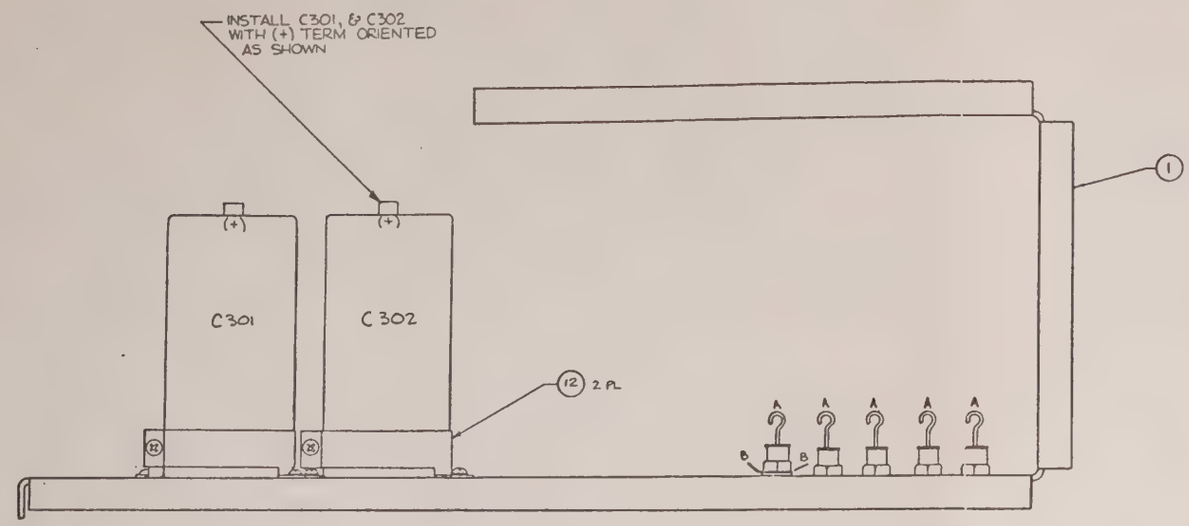
-50	40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION
DO NOT SCALE DRAWING					DRAWN	DATE	GOULD biomation
TOLERANCE					CHECKED		TITLE FILTER [illegible]
					PROJ. ENG.		
					MANUFACTURING		SCALE — SIZE C PART NUMBER 0114-0361 REV B
DASH NO.	NUMBER	QTY	ENG. SERV.	DATE	QUALITY ASSUR		CODE SHEET 1 OF 1
	NEXT ASSEMBLY						

NINHOP GRAPHICS ACCUPRESS REORDER NO A4-28

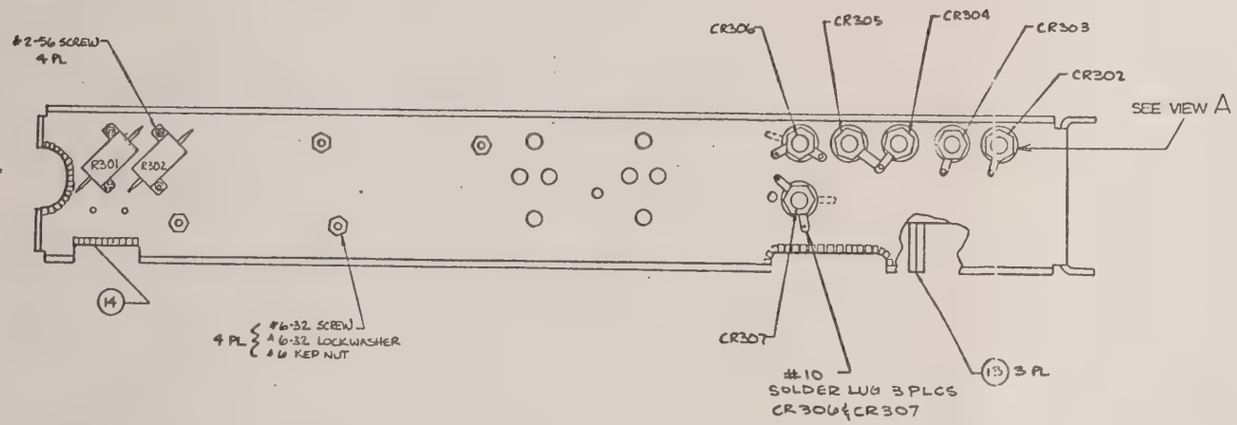
DWG NO 0114-0330 SH 1 REV C

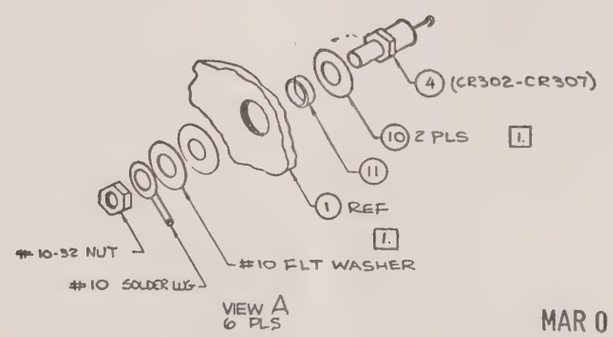
REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	-	PROTOTYPE	[illegible]		
	B	-	PILOT REL PER ERN 0197	[illegible]	[illegible]	[illegible]
	C	2236	REVISED PER ECO.	[illegible]	[illegible]	[illegible]



REFERENCE PRINT





NOTES:

1. USE OF THERMAL COMPOUND REQ'D BETWEEN MICA WASHER AND HEATSINK.

WIRE LIST

FROM	TO	AWG	DESCRIPTION
CR307-3	CR305-A	16	ORG 1 ½"
CR306-3	CR304A	16	BLK 1 ½"

MAR 0 8 1982

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

DIMENSIONAL: X = ± ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0.599 ± .003; 0.999 ± .004; 1.000 ± .999 ± .005

DRAWN [illegible] DATE 9 10 81

CHECKED [illegible] 12 15 81

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV. DATE

DASH NO	NUMBER	QTY
-10	0114-0320	1

NEXT ASSEMBLY

GOULD biomation

TITLE HEATSINK ASSEMBLY

SCALE	SIZE	PART NUMBER	REV
1/1	D	0114-0330	C

CODE SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0114-0326	HEATSINK				FAB
2												
3												
4						6	1200-0043	RECTIFIER	CR302-307		1N6096	
5						2	3250-0011	RESISTOR	R301, R302		20Ω 10W 3%	
6												
7												
8						2	4400-0046	CAP	C301, C302		2000uf 200V	
9												
10						12	7000-0442	MICA WASHER			#10	
11						6	7000-0441	SHOULDER WASH			.280 O.D. X .200 I.D.	
12						2	7000-0046	BRACKET	@ C301, C302			
13						3	7000-0421	STANDOFF, HEX			6-32 X 3/4	
14						A/R	7200-0044	FLEXIBLE GROMMET				
15												
16						A/R	7150-0016-10	WIRE			16 AWG BLK	
17						A/R	7150-0016-03	WIRE			16 AWG ORG	
18												

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	6-29-81	MB		
B	PILOT REL PER ERN 0197	9/21/81	MB	RG	
C	REVISED PER ECO #2236	11/5/81	MB	RD	

DASH NO.	NUMBER	QTY
-10	0114-0320	
	NEXT ASSEMBLY	

		DATE
DRAWN	MBS	6 29 81
CHECKED	J. Wilson	10-15-81
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

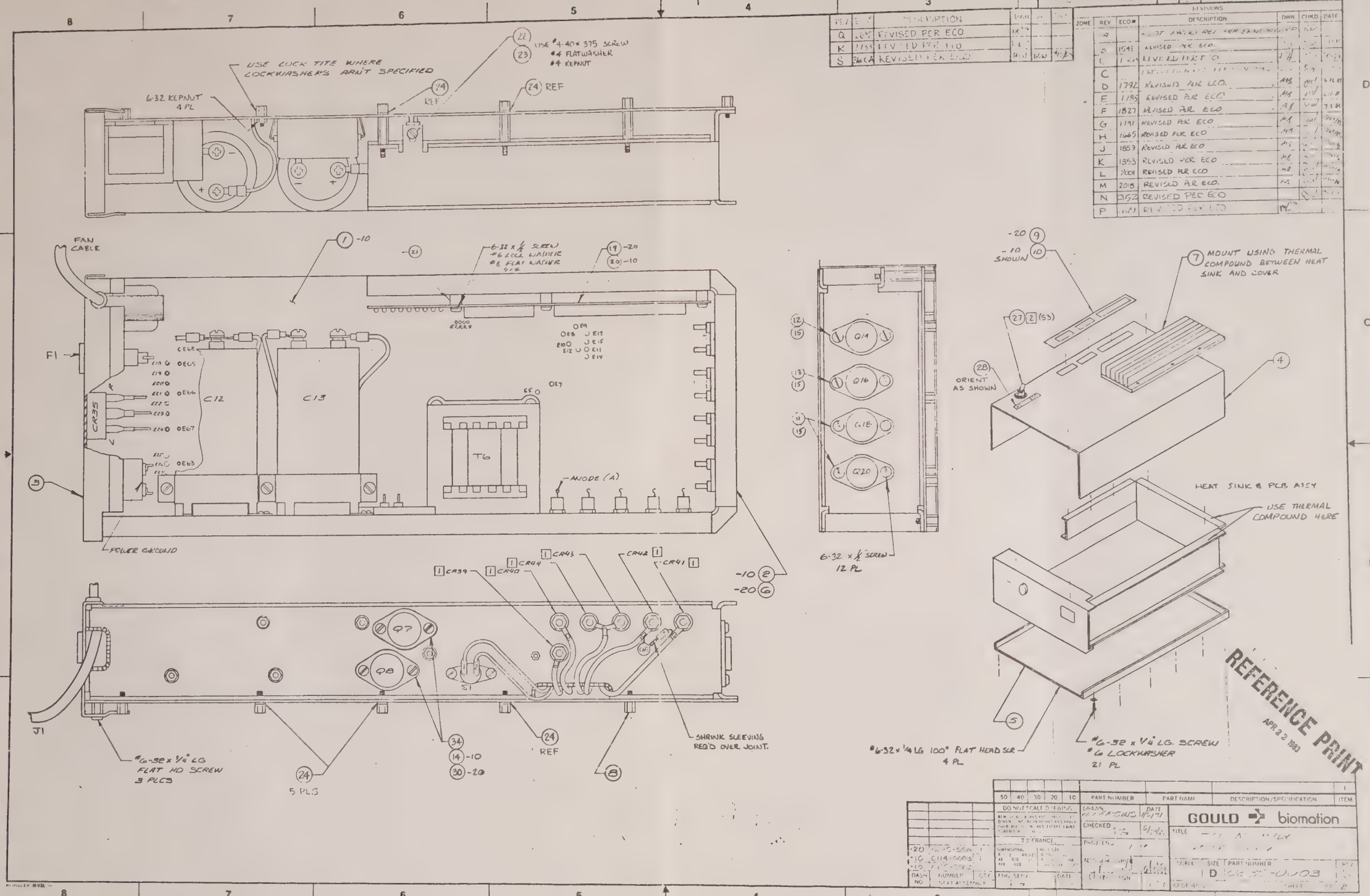
HEAT SINK ASSY

biomation

B	0114-0330	REV C

MODEL K101/K500 | CODE | SHEET 1 OF 1

REFERENCE PRINT



USE LOCK TITE WHERE LOCKWASHERS ARN'T SPECIFIED
6-32 KEPNUT 4 PL
USE #4-40 x 375 SCREW #4 FLATWASHER #4 KEPNUT
REF
FAN CABLE
6-32 x 1/2 SCREW #6 LOCK WASHER #6 FLAT WASHER
F1
CR35
C12
C13
T6
ANODE (A)
POWER GROUND
CR39
CR40
CR44
CR43
CR42
CR41
Q7
Q8
S1
J1
#6-32 x 1/4 LG FLAT HD SCREW 3 PLCS
5 PLS
SHRINK SLEEVING REQ'D OVER JOINT.
Q14
Q16
Q18
Q20
6-32 x 1/2 SCREW 12 PL
-20
-10 SHOWN
MOUNT USING THERMAL COMPOUND BETWEEN HEAT SINK AND COVER
ORIENT AS SHOWN
HEAT SINK & PCB ASSY
USE THERMAL COMPOUND HERE
#6-32 x 1/4 LG 100° FLAT HEAD SCR 4 PL
#6-32 x 1/4 LG. SCREW #6 LOCKWASHER 21 PL
REVISIONS
REV
ECO
DESCRIPTION
DWN
CHKD
DATE
Q
K
S
REVISED PER ECO
A
B
C
D
E
F
G
H
J
K
L
M
N
P
1792
1795
1827
1791
1665
1859
1853
2001
2018
2152
REFERENCE PRINT
APR 22 1983
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SIZE
D
SCALE
DASH NO
NEXT ASSEMBLY

DWG. NO	SH	REV
[illegible]	2	S

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

WIRE LIST

WIRE No.	FROM	TO	DESCRIPTION
1	E1 FILTER PWB.	E1 PS PWB	BRN
2	E2	E2	RED
3	E7	E7	ORG
4	E4	E4	YEL
5	E5	E5	LT BLU
6	—	—	
* 7	E14	E7	VIO
8	E6	E8	BRN
9	E7	E9	RED
10	E13	E10	ORG
11	E8	E11	YEL
12	E9	E12	LT BLU
13	E10	E13	BRN
14	E11	E14	RED
15	E12	E15	ORG
16	E16 P.S. PWB	S1-1 HEAT SINK	BRN
17	E17 P.S. PWB	S1-2 "	RED
18	E15 FILTER BD.	E70 P.S. PWB	VIO
20	E20 P.S. P.W.B.	CR35 (-)	BLK
21	E21	" (L)	VIO
22	E22	" (+)	YEL
23	E23	" (R)	ORG
24	—	—	
25	J1-2 FACE PLATE	E25 P PWB	WHT BRN
26	E26 P.S. PWB.	PWR GND	GRN/YEL
27	J1-4 FACE PLATE	E27 P.S. PWB	BLK/BLU
28	E28 P.S. PWB	C12 (-) HEAT SINK	RED
29	E29	C12 (+)	BRN
30	E30	C13 (-) "	RED
31	E31	C13 (+) "	BRN
38	T6	CR42 (C) HEAT SINK	BLK [3]
39	E39	CR40 (C)	ORG
40	E57	CR47 (A)	ORG
41	E40	CR31 (C)	RED
42	E60	CR44 (A)	RED
43	T6	CR31 (C)	BLK [3]
44	E42	CR39,40 (A)	BRN
45	E43	CR41,42 (A)	YEL
46	E44	CR43,44 (C)	WHT/RED
61	E61	S1-NO	BRN
62	E62	S1-COM	RED

* -20 ONLY

NOTES:

[1] SOLDER LUGS ON DIODES TO HAVE A MIN. OF .100 CLEARANCE TO HEAT SINK & TOP COVER.

[2] WIRES TO BE 7-10 INCHES LONG TO ALLOW FOR SERVICE LOOP. SHRINK TUBE ALL CONNECTIONS AT S3 TO PREVENT SHORTS.

[3] BLACK WIRES FROM T6 ARE INTERCHANGABLE.

S3 WIRE LIST AND DETAIL [2]

WIRING LIST (20 AWG WIRE)

FROM	TO
S3-1	E66
S3-2	E69
S3-3	S3-6
S3-4	E63
S3-5	E64
S3-7	E68
S3-8	E67

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

50 40 30 -20 -10

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDITIONS EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ±.1 ANGLE ±1°; .XX ±.020; .XXX ±.010

HOLE SIZE: 0.999 .003; 1.000 1.499 .004; 1.500 1.999 .005

ENG SERV | DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DRAWN | DATE

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE TPM ASSEMBLY
MAINFR TUNER

SCALE	SIZE	PART NUMBER	REV
NONE	D	02[illegible]3	S

CODE | SHEET 1 OF 2

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1												LM
2												LM
3					1		0285-0156	FACE PLATE ASSY				LM
4					1		0285-0175	TOP COVER				
5					1		0285-0174	LOWER COVER				
6					1		0285-0173-20	HEAT SINK ASSY				LM
7											TOP	FAB
8					14		7000-0423	M/F STANDOFF				
9					1		0285-0203-20	LABEL 4500				
10												
11					2		1400-0039	TRANSISTOR.	Q18,20	2N4276		
12					1		1300-0042	"	Q 14	2N5885		
13					1		1400-0030	"	Q 16	2N5883		
14												
15					6		7200-0016	INSULATOR	Q7,8,14,16,18,20	60-11-4996-1666		
16												LM
17											JUL 18 1983	LM
18												LM

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
P	REVISED PER ECO 2629	11-17-82	[illegible]	DGW	
Q	REVISED PER ECO 2632	11-17-82	[illegible]	DGW	
R	REVISED PER ECO 2733	11-17-82	[illegible]	DGW	
S	REVISED PER ECO 3600A	3/29/83	MW	DGW	4/5/83
D	REVISED PER ECO #1792	6-16-81	[illegible]	[illegible]	
E	REVISED PER ECO # 1785	6-11-81	[illegible]	[illegible]	
F	REVISED PER ECO # 1827	7-1-81	[illegible]	[illegible]	

DASH NO.	NUMBER	QTY
-20	0285-[illegible]	1
-10	0114-[illegible]	1
-10	0952-[illegible]	1

NEXT ASSEMBLY

		DATE
DRAWN	J. PERKINS	10/30/82
CHECKED	RG	5/29/81
ENGINEER		
MANUFACTURING	[illegible]	[illegible]
QUALITY ASSURANCE		[illegible]

LIST OF MATERIAL

POWER SUPPLY

TOP ASSEMBLY

biomation

MODEL 4500

B 0285-0005 REV S

CODE

SHEET 1 OF [illegible]

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -70	-60	-50	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19					1		0285-[illegible]	FILTER BOARD				LM
21					4		7000-0322	SPACER 1/4 #6				
22					1		7000-0319	SHOULDER WASHER	Q1		#4	
23					1		7000-0017-10	INSULATOR	Q1			
24					5		7000-0221	WASHER			#4	
25					1		0285-0195-20	WIRE ASSY				LM
26					1		0285-0196-20	WIRE ASSY				LM
27					1		6600-0129	SWITCH	S3			
28					1		0114-0321	LABEL				
29					1		0285-0010-20	PW ASSY				LM
30					2		1300-0054	TRANSISTOR	Q7, 8		2N6545	
31					1		0285-0010-20	PWB ASSY				LM
32												
33												

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	REVISED PER ECO #1791	8-24	MB	[illegible]	
	H	REVISED PER ECO #1665	8-24	MB	[illegible]	
	J	REVISED PER ECO #1859	8-24	MB	[illegible]	
	K	REVISED PER ECO #1853	8-24	MB	[illegible]	
	L	REVISED PER ECO #2001	8-24	MB	[illegible]	
	M	REVISED PER ECO #2018	10/22/80	MB	[illegible]	
	N	REVISED PER ECO #2152	11/12/81		[illegible]	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	[illegible]	2-2-81
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

POWER SUPPLY
TOP ASSEMBLY

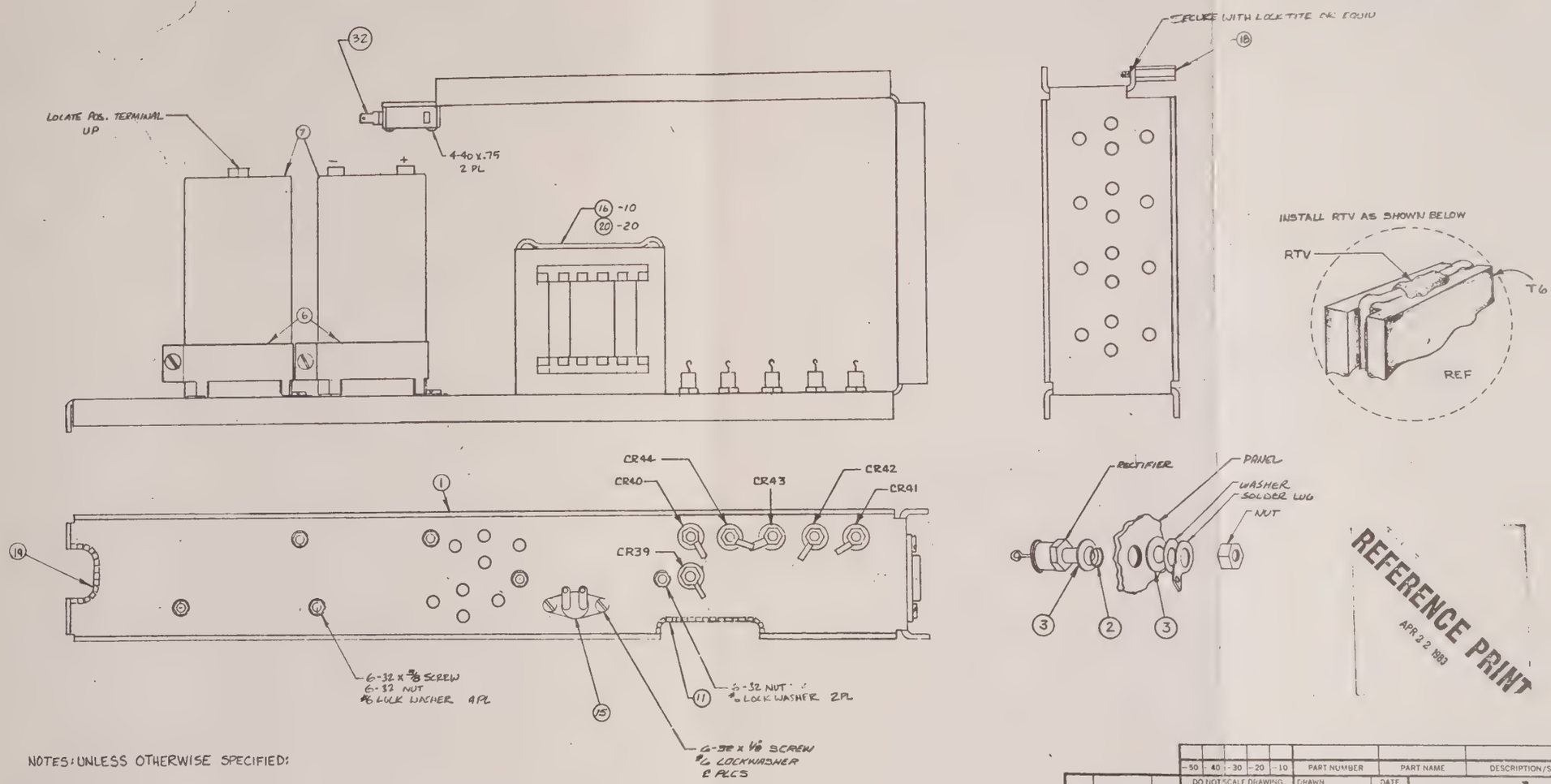
MODEL 4500

biomation

B	0285-[illegible]	REV S
CODE		SHEET [illegible] OF [illegible]

DWG. NO	SH	REV
0280-0173	1	Q

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	Q	3604	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	B	1472	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	C	1476	CANCELLED (NO CHANGE TO ASSY)	[illegible]	—	—
	D	1547	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	E	1527	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	F	1696	REVISED PER ECO	JWC	[illegible]	[illegible]
	F	ECN [illegible]	PRODUCTION RELEASE	[illegible]	[illegible]	[illegible]
	G	1784	NO CHANGE (ECO ERROR)	[illegible]		[illegible]
	H	1789	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	J	1834	REVISED PER ECO.	[illegible]	[illegible]	[illegible]
	K	1665	REVISED PER ECO	[illegible]	[illegible]	
	L	2418	REVISED PER ECO	[illegible]	[illegible]	
	M	2434	REVISED PER ECO NO	[illegible]	[illegible]	[illegible]
	N	2733	REVISED PER ECO NO	[illegible]	[illegible]	
	P	3583	REVISED PER ECO NO	JWC	[illegible]	3/5/83



REFERENCE PRINT
APR 22 1983

NOTES: UNLESS OTHERWISE SPECIFIED:

1. MYLAR TAPE, ITEM 21, TO BE PLACED ON CAPACITORS, ITEM 7, BEFORE BRACKETS, ITEM 6.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS EXPRESSED IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS.

TOLERANCE
DIMENSIONAL: X ± .1 FRACTIONS; XX ± .020; XXX ± .010
HOLE SIZE: 0-.99 BOLT; 1.0-1.99 TOOL; 1.0-2.499 TOOL

DRAWN	[illegible]	DATE	11 20 [illegible]
CHECKED	[illegible]		5/29/81
PROJ. ENG.	[illegible]		
MANUFACTURING	[illegible]		6/3/81
QUALITY ASSUR	[illegible]		

GOULD biomation

TITLE: ASSY, HEATSINK

SCALE	SIZE	PART NUMBER	REV
	D	0280-0173	Q

CODE [illegible] SHEET [illegible] OF 1

DASH NO	NUMBER NEXT ASSEMBLY	QTY

ENG. SERV [illegible] DATE [illegible]

KLINGLER 16-VEL H

									REF. DESIGNATION	VENDOR NO	DESCRIPTION	
1					1		0285-176	HEAT SINK				
2					6		7000-0441	BUSHING	CR39-43			
3					12		7000-0442	WASHER	CR39-43		MICA	
4												
5												
6					2		7000-0464	BRACKET				
7					2		4400-0046	CAP	C12, 13		2000MF 200V	
8					2		1200-0015	RECTIFIER	CR43, 44	IN5826		
9					4		1200-0036	RECTIFIER	CR39, 40, 41, 42	IN6095		
10												
11					A/R		7200-0044	FLEX GROMET		SPG2-2		
12												
13												
14					1		6600-0121	SWITCH	S2			
15					1		6600-0014	ELMWOOD SENSOR				
16												LM
17												
18					3		7000-0421	STAND-OFF			MALE/FEMALE	

ASSEMBLY TIME

REFERENCE PRINT
APR 22 1983

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN #0082		JKP		
P	REVISED PER ECO Nº 3583	3-15-83	[illegible]	DW	
Q	REVISED PER ECO Nº 3600A	3/[illegible]	[illegible]	DW	4/5/83
D	REVISED PER ECO 1547	3-20-81	[illegible]	[illegible]	
E	REVISED PER ECO 1567	3-20-81	[illegible]	SD	
F	REVISED PER ECO # 1696	4-30-81	[illegible]	ZD	
F	PROD REL. PER ERN Nº 0152	[illegible]	[illegible]	RG	

DASH NO.	NUMBER	QTY
-20	0285-0003-20	1
-10	0285-0003-10	1

NEXT ASSEMBLY

		DATE
DRAWN	J. PERGINS	3/9/81
CHECKED	RG	5/29/81
ENGINEER	K.U. Brink	6/5/81
MANUFACTURING	[illegible]	6/3/81
QUALITY ASSURANCE	[illegible]	6/3/81

LIST OF MATERIAL

HEAT SINK ASSY

biomation

B 0285-0173 REV Q

MODEL 4500 CODE SHEET 1 OF 2

		COST	COST

	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19												
20					1		9000-0100-20	TRANSFORMER ASSY				LM
21												
22												
23												
24												
25												
26												
27												
28												
29												
30												
31												
32												
33												
34												
35												
36												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	ECO 1784 NO CHANGE (ECO ERROR)	11/2/81	AS		
	H	REVISED PER ECO #1785	11/27/81	AS		
	J	REVISED PER ECO #1834	6/5/82	AS		
	K	REVISED PER ECO # 1665	3-22-82	[illegible]	ED	
	L	REVISED PER ECO # 2418	[illegible]		[illegible]	
	M	REVISED PER ECO No 2434	4-16-88	[illegible]	[illegible]	
	N	REVISED PER ECO 2733	11-17-88	[illegible]	DCW	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

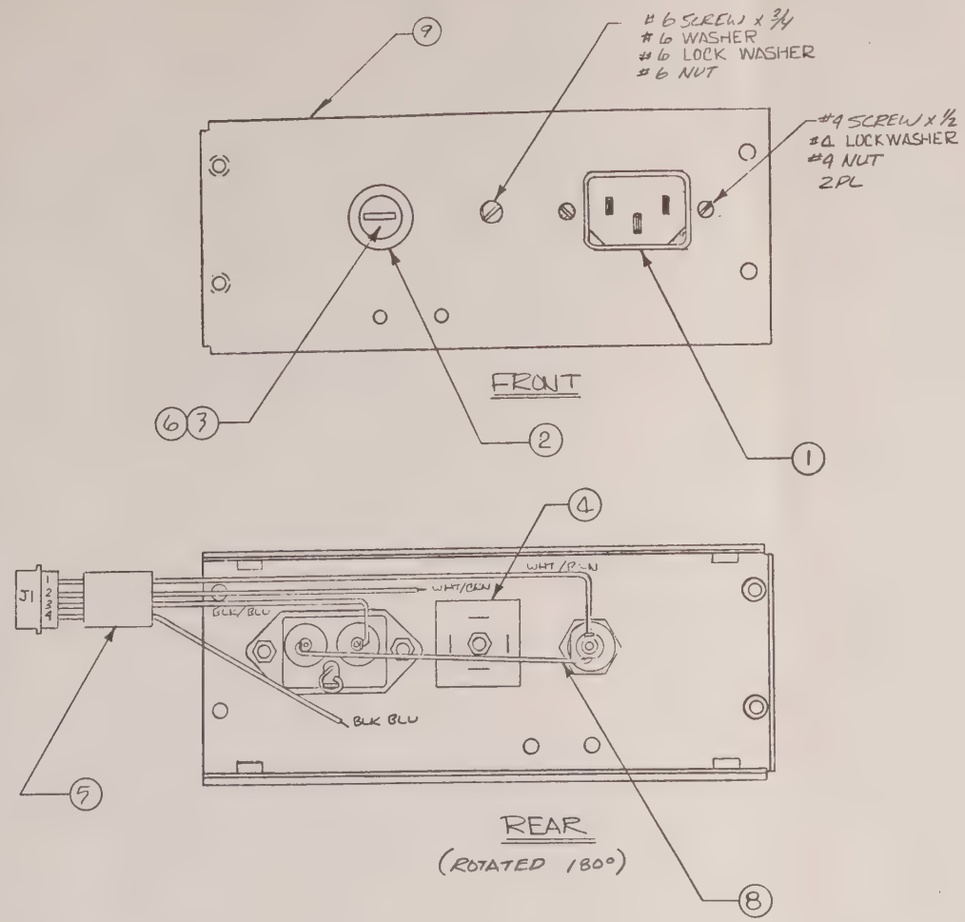
HEATSINK ASSY

biomation

B	0285-0173	REV Q

MODEL 4500 | CODE | SHEET 2 OF 2

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER ERN No 0082	SWC	RD	11-18-80
	B	1522	REVISED PER ECO.	ME	RD	5-11-81
	B		PROD REL PER ERN #0128	SR	RG	4-10-81
	C	1670	REVISED PER ECO	[illegible]	JL	4-20-81



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER	QTY
-10	[illegible]	1
-10	0285-0083-10	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0.539 .003; .600 .999 .004; 1.000 1.499 .005

ENG. SERV. P. Simpson — DATE 9/15/81

		DATE
DRAWN	SWCARROLL	11-18-80
CHECKED	[illegible]	4/15/81
PROJ. ENG.	[illegible]	4-15-81
MANUFACTURING	S. Charbin	4-10-81
QUALITY ASSUR	[illegible]	[illegible]

GOULD biomation

TITLE: ASSEMBLY FACE PLATE

SCALE	SIZE	PART NUMBER	REV
NONE	C	0285-0156	C

CODE 2850 [illegible] — SHEET 1 OF 1

DWG NO 0285-0156 — REV C

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4428

COMMENTS		TOTAL COST	UNIT COST

ITEM													
1						1	[illegible]	[illegible]					
2						1	[illegible]	[illegible]					
3						1	[illegible]	[illegible]					
4						1	[illegible]	[illegible]	[illegible]		[illegible]		
5						1	[illegible]	[illegible]					LM
6						1	7300-0028	FUSE			6AMP 3 AG		
7													
8						1	0285-0175	WIRE FAB					
9						1	0285-0172	FACE PLATE					
10													
11													
12													
13													
14													
15													
16													
17												JUL 1 8 1983	
18													

ASSEMBLY TIME

COMPONENT LEAD SPACING

REV	DESCRIPTION	DATE	DWN	CHK	APPD
A	[illegible]		[illegible]	[illegible]	
B	[illegible]	[illegible]	[illegible]	[illegible]	
B	[illegible] PER ECN #028	[illegible]	[illegible]	[illegible]	
C	[illegible] PER ECN #1670	[illegible]	[illegible]	[illegible]	

BASH NO	NEXT ASSEMBLY	QTY

DRAWN [illegible] DATE [illegible]

CHECKED [illegible]

LIST OF MATERIAL
ASSEMBLY
FACE PLATE

biomation

B 0285-0156 REV C

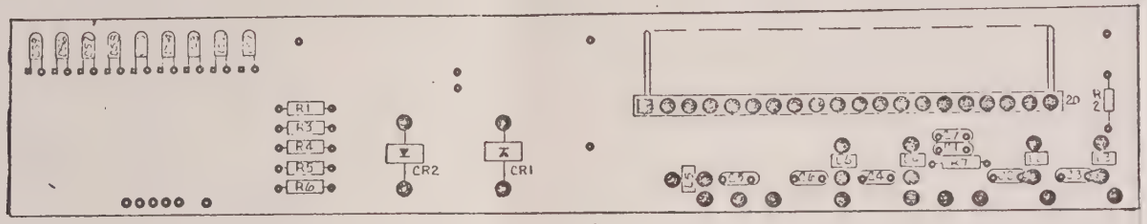
MODEL 2850 [illegible]

SHEET 1 OF 1

DWG NO 0285-0180 | SH 1 | REV F

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	ERN	CHKD	DATE
	B		PILOT REL PER ERN 0122		JL	
	C	1738	REVISED PER ECO N2	[illegible]	RG	[illegible]
	C		PROD REL PER ERN 0192	JWC	RG	[illegible]
	D	1946	REVISED PER ECO #	[illegible]	[illegible]	[illegible]
	E	2089	REVISED PER ECO	[illegible]	[illegible]	
	F	419	REVISED PER ECO N°	JWC	RD	4-1-82



REFERENCE PRINT

APR 07 1982

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0.599 - .003; .600 .999 - .004; 1.000 1.499 .005

DASH NO	NUMBER	QTY
-10	0285-0001	1
	NEXT ASSEMBLY	

ENG SERV RG | DATE 6/2/82

DRAWN JWC SANDELL | DATE 6-2-81

CHECKED RG | 6/2/81

PROJ. ENG. [illegible] | 6/3/81

MANUFACTURING [illegible] | 6/3/81

QUALITY ASSUR [illegible] | 6/3/81

GOULD biomation

TITLE ASSY POWER SUPPLY FILTER BD

SCALE 2/1 | SIZE D | PART NUMBER 0285-0180 | REV F

CODE 4500 | SHEET 1 OF 1

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0285-0162	PWB (FILTER)				FAB
2						5	9000-0074	INDUCTOR	L1-5			LM
3						2	1200-0017	RECTIFIER	CR1, 2			
4						7	4000-0025	CAP	C1-7		.1 µf 100v 10% CER.	
5						1	6000-0351-20	HEADER	J1		20 PIN	
6						1	6000-0351-10	HEADER	J2		10 PIN	
7						4	6400-0039	LED	DS6-9		RED	
8						5	6400-0046	LED	DS1-5		GRN	
9						1	3000-1006	RESISTOR	R7		10Ω, 1/4W, 5%	
10												
11												
12						2	3000-2701	RES	R1, 2		2.7K 1/4w 5%	
13						1	3000-3906		R3		39Ω "	
14						2	3000-1500		R4, 5		150Ω "	
15						1	3000-1801		R6		1.8K "	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL PER ERN 0282	11-80	DJS	RD	
B	REVISED PER ECO 1455	3-4-81	MB	RD	
C	REVISED PER ECO 1552	3-24-81	MB	RD	
D	REVISED PER ECO 1737	5-12-81	RJ	RD	
D	PRODUCTION REL PER ERN #0152	5-28-81	[illegible]	RG	
E	REVISED PER ECO Nº 1858	7-16-81	WC	MB	7-24-81
F	REVISED PER ECO #1945	9-15-81	RJ	RG	

DASH NO.	NUMBER	QTY
-10	0285-0003	1
	NEXT ASSEMBLY	

		DATE
DRAWN	SANUT LL	11 80
CHECKED	RG	5/29/81
ENGINEER	R O Bin[illegible]	6/5/81
MANUFACTURING	[illegible]	6/3/81
QUALITY ASSURANCE	[illegible]	6/3/81

LIST OF MATERIAL

ASSY, PWR SUPPLY
FILTER BOARD

biomation

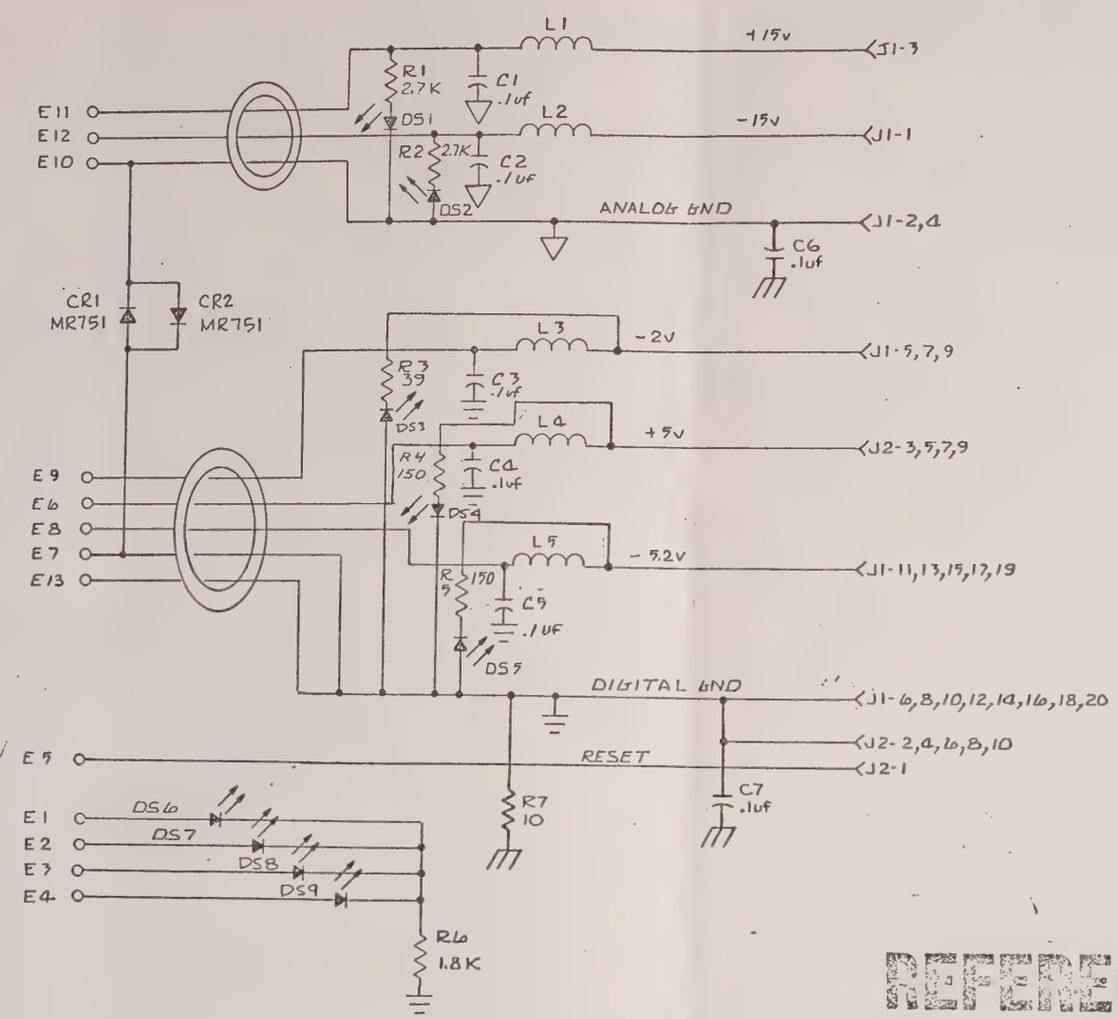
B	0285-0160	REV F

MODEL 2850, K101, K500 | CODE | SHEET / OF /

REFERENCE PRINT

MAR 0 8 1982

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PRTO TYPE			
	B		REDRAWN	SWC	RD	11-14-8
	C		REVISED PER ECO 1455 8-4-81		RD	3/1/81
	D	1552	REVISED PER ECO.		RD	5-14-81
	E	1737	REVISED PER ECO		RD	5/1/81
	E	—	PRODUCTION REL PER ERN#0152	SWC	RG	5-28-81



NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4w 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS
3. ANALOG GROUND
4. DIGITAL GROUND
5. CHASSIS GROUND

REFERENCE PRINT

MAR 0 9 1982

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010, ANGLES ± 1°

HOLE SIZE: 0 599 - .003, 600 999 - .004, 1 000 1 499 - .005

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-10	0285-0160	1

ENG. SERV. RG DATE 5/29/81

		DATE
DRAWN	S. WEARDULL	11-14-80
CHECKED	RG	5/29/81
PROJ. ENG.	K. Olivet	4/2/81
MANUFACTURING	J. Fleming	4/2/81
QUALITY ASSUR.		

GOULD biomation

TITLE SCHEMATIC POWER SUPPLY FILTER BD

SCALE	SIZE	PART NUMBER	REV
NONE	C	0285-0161	E

CODE K101 - K500 SHEET 1 OF 1

DWG NO. 0285-0161 SH 1 REV E

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4428

		COST	COST

	60	50	40	30	20	10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	
1					1		028[illegible]-0012	PWB				FAB
2												
3					15		1000-0002	DIODE	CR6-9, 24-30, 13,	37-39	1N4152	
4												
5					10		1200-0031	DIODE	CR10, 11, 16, 17,	19-23, 18	1N4937	
6												
7												
8					1		1200-0026	DIODE BRIDGE	CR1		VE18X	
9												
10					3		1200-0014	DIODE	CR14, 15, 46		1N4004	
11												
12					1		1100-0015	DIODE	CR 31		1N825	
13					2		1100-0043	DIODE	CR4, 5		1.5KE220	
14												
15					1		1000-0022	DIODE	VR1		1N5352	
16					4		1200-0035	DIODE	CR33, 34, 36, 45		MR820	
17												
18												

ASSEMBLY TIME | COMPONENT ...CING

REFERENCE PRINT
APR 22 1983

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE				
B	REDESIGNED	11-20-80	[illegible]	[illegible]	
C	PILOT REL PER ERN 0089			[illegible]	
D	CHANGED PER ECO # 1486	3-10-81	[illegible]	[illegible]	
E	UPDATED PER PILOT RUN ECO 1521	3-10-81	[illegible]	[illegible]	
F	ECO 1554	3-21-81	[illegible]	[illegible]	
G	ECO 1568	4-2[illegible]	[illegible]	[illegible]	

DASH NO.	NUMBER	QTY
-70	0285-0003	1

NEXT ASSEMBLY

		DATE
DRAWN	M [illegible]	11-20-80
CHECKED	R. [illegible]	6/5/81
ENGINEER	K O [illegible]	6/5/81
MANUFACTURING	[illegible]	6/3/81
QUALITY ASSURANCE	[illegible]	6/3/81

LIST OF MATERIAL
POWER SUPPLY
ASSY - PWA

biomation

B | 0285-0010 | REV KK

MODEL 4500 | CODE | SHEET 1 OF 13

19												
20					A/R		8300-0002	MYLAR TAPE				
21					1		1300-0006	TRANSISTOR	Q17.		2N2219	
22					5		1300-0028		Q5, 6, 10, 12, (Q13 -20 ONLY)		2N3904	
23					1		1300-0035		Q21		2N6131	
24					1		1400-0003		Q15		2N2905	
25					1		1400-0026	TRANSISTOR	Q19		2N6134	
26												
27					1		1400-0019	TRANSISTOR	Q11		2N3906	
28												
29												
30												
31												
32					1		1300-0056	TRANSISTOR	Q4		2N3439	
33												
34					1		1700-0047	IC.	Q1		LM340T	
35					1		3700-0078	RES PACK	RP1		100K	
36					1		3700-0077	RES PACK	RP2		4.7K	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	H	ECO 1621	4.28.81	R.H.	RD	
	J	ECO 1636	4.28.81	R.H.	RD	
	K	ECO 1650	4.28.81	R.H.	RD	
	L	ECO 1629	4.28.81	R.H.	RD	
	M	ECO 1683	5.6.81	R.H.	RD	
	N	ECO 1697	5.6.81	R.H.	RD	
	P	ECO 1728	5.6.81	R.H.	RD	

ASSEMBLY TIME

COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M BURTON — DATE 11.20.80

CHECKED

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LIST OF MATERIAL

POWER SUPPLY
ASSY PWA

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B 0285-0010 REV KK

MODEL 4500

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SHEET 2 OF 13

	60	50	40	30	20	10	[illegible]	PART NAME	REF. DESIGNATION	VENDOR NO.	[illegible]	[illegible]
37												
38												
39												
40					1		1700-0096	I.C.	U12		LM358	
41					3		1700-0086	I.C.	U3,4,9		LM324	
42												
43					1		1820-0073	CMOS	U6		14541	
44					1		-0066		U2		14175	
45					1		-0002		U11		14002	
46					1		-0004		U1		14012	
47					1		-0017		U5		14013	
48					1		-0072		U10		14093	
49					1		1300-0057	TRANSISTOR	U14		4N35	
50												
51					1		1700-0095	I.C	U8		TL494	
52												
53												
54												

	COST	COST

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
Q	ECO 1736	5-14-8[illegible]	R.H.	RD	
Q	PRODUCTION REL [illegible] ERN #0152	[illegible]	[illegible]	RG	
R	REVISED PER ECO #1781	8-24-81	MK	[illegible]	
S	REVISED; ECO #1785	6-10-81	[illegible]	[illegible]	
T	REVISED; ECO #1831	8-24-8[illegible]	ML	[illegible]	
U	REVISED; ECO# 1853	8-24-81	BB	[illegible]	
V	REVISED; ECO #1859	8-24-81	MB	[illegible]	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M Bart — DATE 11 20 80

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MODEL 4500

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SHEET 3 OF 13

								PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
55												
56					2		3000-1503	RESISTOR	R150, 151		150K 1/4W 5%	
57					2		3000-1000	RESISTOR	R39, 40,		100Ω 1/4W 5%	
58					12		-1002		R65, 70, 77, 86, 88,		10K	
59									93, 106-108, 110, 125, 144			
60					6		-1003		R1, 78, 84, 103, 104, 136		100K	
61					1		-2202		R142		22K	
62												
63					3		-2204		R105, 154, 153		2.2MEG	
64												
65					1		-4301		R97		4.3K	
66					8		-2201		R23, 24, 51, 101, 117-119, 152		2.2K	
67					2		-2200		R135, 137		220Ω	
68					1		-1501		R13		1.5K	
69					1		-1800		R50		180Ω	
70					1		-1803		R102		180K	
71												
72					1		3000-1101	RES	R121		1.1K, 1/4W, 5%	

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
W	REVISED; ECO #1980	8-24-81	[illegible]	[illegible]	
X	REVISED PER ECO #2018	[illegible]	[illegible]	[illegible]	
Y	REVISED PER ECO #2083	[illegible]	[illegible]	[illegible]	
Z	REVISED PER ECO #2152	[illegible]	MK	[illegible]	
AA	REVISED PER ECO #2199	3-[illegible]	[illegible]	[illegible]	
BB	REVISED PER ECO # 2420	3-26-[illegible]	[illegible]	[illegible]	
CC	REVISED PER ECO # 2433	[illegible]	[illegible]	[illegible]	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M BURTON — DATE 11-20-80

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73					1		3100 1962	RESISTOR	R85		19.6K, 1, 1%	
74					1		3000-4703	RESISTOR	R12		470K 1/4W 5%	
75												
76					5		-6804		R42-44, 47, 48		6.8MEG	
77					2		3000-5103		R55, 57		510K,	
78					1		3000-2401	RES	R 140		2.4K, 1/4W, 5%	
79					1		3000-2702	RES	R145		27K, 1/4W, 5%	
80					1		3000-4700	RESISTOR	R14		470Ω 1/4W 5%	
81					4		-4706		R27, 28, 126 (R115-20 ONLY)		47Ω	
82												
83					3		-4701		R18, 21, 22,		4.7K	
84					3		-5601		R15, 80, 112		5.6K	
85					3		-5101		R45, 46, 146		5.1K	
86					3		3000-2701	RESISTOR	R19, 20, 109,		2.7K 1/4W 5%	
87												
88					2		3000-3206	RESISTOR	R31, 32		82Ω 1/4W 5%	
89												
90					1		3000-3306	RESISTOR	R17		33Ω 1/4W 5%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
DD	REVISED PER ECO # 2538	[illegible]	[illegible]	[illegible]	
EE	REVISED PER ECO# 2629	[illegible]	[illegible]	[illegible]	
FF	REVISED PER ECO# 2632	[illegible]	[illegible]	[illegible]	
GG	REVISED PER ECO# 2722	[illegible]	[illegible]	[illegible]	
HH	REVISED PER ECO# 2733	[illegible]	[illegible]	[illegible]	
JJ	REVISED PER ECO #3516	2-28-8[illegible]	DGW	—	—
KK	REVISED PER ECO# 3600A	3/30/[illegible]	[illegible]	DGW	4/5/[illegible]

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	M Bx	11 20 80
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LIST OF MATERIAL

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91												
92					1		3000-4702	RESISTOR	R61		47K ¼w 5%	
93					1		-4707		R130		4.7Ω	
94					4		-1001		R66,67,138 (R116-20 ONLY)		1K	
95					2		-1302		R59, 62		13K	
96					1		-3302		R60		33K	
97					1		-1102		R79		11K	
98					2		3000-2002		R41,82		20K 1/4W 5%	
99					2		3100-2002		R83,122		20K 1/8W, 1%	
100					1		3000-8201	RESISTOR	R52		8.2K ¼W 5%	
101												
102					1		3000-1502	RESISTOR	R49		15K ¼w 5%	
103												
104												
105					1		3100-1503		R123		150K ⅛W, 1%	
106					1		3100 5621		R127		5.62K	
107					1		3100-3921	RESISTOR	R128		3.92K ⅛W 1%	
108												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

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POWER SUPPLY ASSY PWA

biomation

B	0285-0010	REV KK
MODEL 4500	CODE	SHEET 6 OF 13

							PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION
110											
111					8		3120-1002	RESISTOR	R56, 58, 68, 69, 73, 74		10K 1/8W .5%
112									71, 72		
113					1		3100-8871	RESISTOR	R158		8.87K, 1/8W, 1%
114					1		3100-1151	RESISTOR	R159		1.15K, 1/8W, 1%
115					2		3050-1507	RESISTOR	R25, 26		1.5Ω 1/2W 5%
116					2		-8200		R29, 30		820Ω 1/2W 5%
117											
118					1		3200-0039	RESISTOR	R139		22Ω, 2W
119											
120					2		3070-3000	RESISTOR	R100, 131		300Ω 1W 5%
121					1		3070-4700	RESISTOR	R3		470Ω 1W 5%
122					1		3050-1007	RESISTOR	R143		1Ω, 1/2W, 5%
123					2		0285-0200-20	RESISTOR	R90, 91		1.2 MILLI OHM
124											
125					2		3080-5602	RESISTOR	R10, 11		56K 2W 5%
126					1		3080-5106	RESISTOR	R157		51Ω 2W 5%
127					1		3050-1206	RESISTOR	R156		12Ω 1/2W 5%

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
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DRAWN M.K. Bo[illegible] DATE 11-20-80
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128											
129					1		3200-0037	RESISTOR	R16		3.0K 5W
130					3		3200-0033	RESISTOR	R33,34,133		10Ω 5W
131					2		3200-0035	RESISTOR	R35,36		500Ω 10W
132					1		3080-3906	RESISTOR	R99		39Ω 2W 5%
133											
134					2		0285-0199	RESISTOR COIL	R75,76		10 Milli Ohm
135					1		0285-0200-10	RESISTOR COIL	R89		2 Milli Ohm
136					2		3200-0038	RESISTOR	R132,134		47Ω 3W 5%
137											
138					5		3300-0005	VAR. RESISTOR	R53,54,94-96		200Ω
139					5		3300-0068	VAR. RESISTOR	R63,64,87,129,	141	5K
140											
141											
142											
143											
144											
145											

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APP

DASH NO.	NUMBER	QTY
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DRAWN M.H. Bart — DATE 11.20.80

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SHEET 3 OF 13

		COST	COST

	60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION
146											
147					1		4010-0101	CAPACITOR	C60		100 pF
148					1		4010-0103	CAPACITOR	C14,		.01uf 50V
149					3		4000-0049		C6, 7, 67		.01uf 1KV, 20%
150					20		4000-0104		C1,8,19,20,27-32, 43,		.1uf, 50V
									50,57,61,63-66	(C25,62,-20 ONLY)	
152					9		4000-0044	CAPACITOR	C26,37, 33, 34, 42,	44, 47, 49,59	.01uf, 100V
153					2		4200-0037	CAPACITOR	C22, 23		.01uf, 400V POLYPROPYLENE
154					1		4200-0006	CAPACITOR	C39		.01uf, 100V
155					1		4000-0007	CAPACITOR	C58		1uf, 50V
156					3		4100-0015	CAPACITOR	C15, 16, 36		1000 pf, 500V
157					3		4100-0018	CAPACITOR	C17, 18, 35		330 pf, 500V
158					2		4010-0471	CAPACITOR	C70, 41		470pf 50V/10%
159											
160					1		4300-0024	CAPACITOR	C45		4.7uf, 50V
161					2		4010-0822	CAPACITOR	C40, 69		.0082uf, 50V, 10%
162											
163											

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN		DATE 11 20 80
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LIST OF MATERIAL
POWER SUPPLY
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CODE		REV
B	0285-0010	KK

SHEET 1 OF 3

164					1		4400-0037	CAPACITOR	C2		470µ 25V	
165					1		4100-0012	CAPACITOR	C48,		390 pf, 500V	
166					3		4400-0050	CAPACITOR	C53,54,55		470µf, 12V	
167					2		4400-0052		C51,52		470uf/50V	
168					1		4300-0009		C21		22uf, 15V	
169												
170												
171					1		4200-0036		C11		6uf, 200V	
172					1		4000-0050	CAPACITOR	C68		.005 uf	
173					2		4200-0041	CAPACITOR	C4,5		47µf, 400V	
174					1		4400-0051	CAPACITOR	C3		2200 uf, 25V	
175												
176												
177					4		6400-0039	L.E.D.	DS4,5,6,7		RED	
178												
179												
180					1		0285-0221-10	WIRE ASSY				
181					1		0285-0221-20	WIRE ASSY				

ASSEMBLY TIME

COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
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SHEET 12 OF 13

		COST	COST

	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
182					1		640[illegible] 0052	NEON LAMP	DS3	NE2		
183												
184												
185												
186					1		2500-0010-20	TRANSFORMER	T1		LINE XFMR 110/220 PRIMARY.	
187					1		9000-0164	TRANSFORMER	T2,		INPUT BALUN XFMR 2213	
188					2		9000-0075	TRANSFORMER	T4, T5		BASE DRIVE XFMR	
189												
190					1		9000-0078	TRANSFORMER	T7		CURRENT SENSING XFMR	
191					1		9000-0079-20	INDUCTOR	L6		12μh	
192					2		9000-0077	INDUCTOR	L2, L3		SNUBBER INDUCTOR 15 μH	
193					1		9000-0079-10	INDUCTOR	L5		HI-CURRENT OUTPUT INDUCTOR, 45 uH	
194					2		9000-0080	INDUCTOR	L7, L8		LO-CURRENT OUTPUT INDUCTOR, 250 μH	
195					1		9000-0083	INDUCTOR	L4			
196					2		9000-0165	INDUCTOR	L9, L10			
197												
198												
199												

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	[illegible]	11-20-[illegible]
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200					2		0285-0187-10	WIRE FAB			BRN	
201					3		-20				RED	
202					—		-30				BLK	
203					—		-40				RED	
204					5		-50				BLK	
205					1		-60				BRN	
206					1		-70				RED	
207					1		-80				BLK	
208					1		0285-0186	CABLE ASSY			RED BRN	LM
209												
210					2		0285-0185-10	"			BRN	LM
211					2		" -20	"			RED	LM
212					1		0285-0190-10	ASSY, BRIDGE WIRE			ORG	LM
213					1		-20	"			YEL	LM
214					1		-30	"			VIO	LM
215					1		-40	"			BLK	LM
216					1		0285-0191-10	CABLE ASSY, FAN			BLK, TAN	LM
217					—		0285-0187-91	CABLE FAB			BLK	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN SANDELL	DATE 12-2-80	
CHECKED		
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MANUFACTURING		
QUALITY ASSURANCE		

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL
POWER SUPPLY ASSY

biomation

B	0285-0010	REV KK
MODEL 4500	CODE	SHEET 12 OF 13

	60	50	40	30	20	10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	REV
218					1		0285 201-01	RECT. WIRE FAB			2N	
219					1		-03				RED	
220					1		-04				RED	
221					1		-05				ORG	
222					1		-06				ORG	
223					1		-07				YEL	
224												
225												
226					1		-10				WHT/RED	
227					1		0285-0189-90	WIRE FAB			GRN/YEL	
228					—		0285-0189-92	WIRE FAB			BLK	
229					2		6100-0150	SOCKET	XQ18, 20		.060 DIA. TERM.	
230					4		6100-0149	"	XQ7, 8, 14, 16		.040 DIA TERM.	
231												
232					2		7200-0029	MOUSE TAIL			3" LONG	
233					1		0285-0334-10	CABLE ASSY			BLACK	
234					2		0285-0334-20	CABLE ASSY			RED	
235					1		0285-0334-30	CABLE ASSY			BLACK	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

ASSEMBLY TIME	COMPONENT LEAD SPACING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN	SNUDELL	1-27-81
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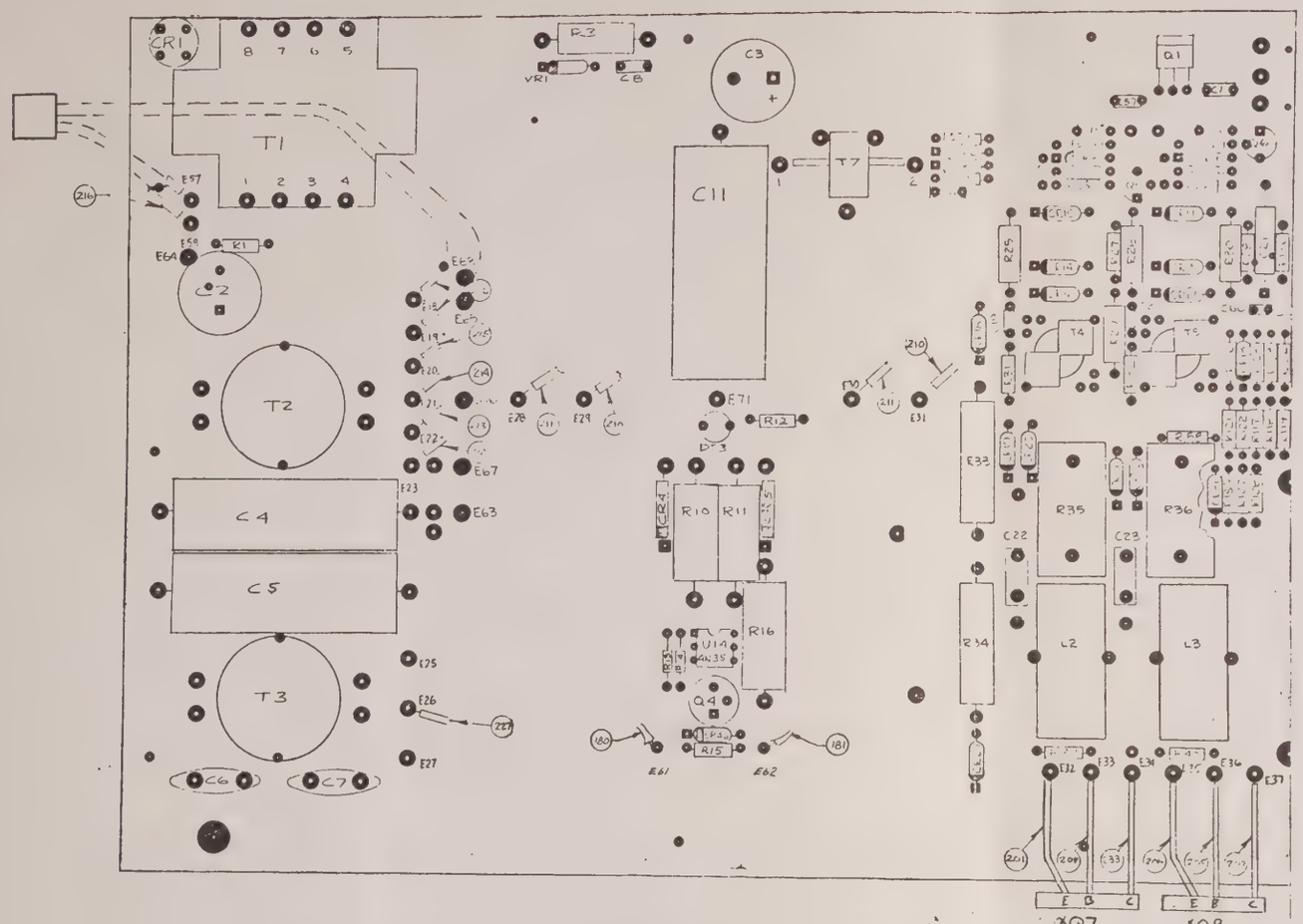
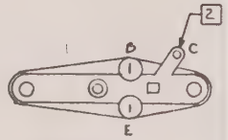
REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	C		RELEASED PER ERN [illegible]	[illegible]	[illegible]	[illegible]
	D	1486	CHANGES MADE PER ECO	[illegible]	[illegible]	[illegible]
	E	1521	UPDATED PER PILOT RUN	[illegible]	[illegible]	[illegible]
	F	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	G	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	H	[illegible]	[illegible]	[illegible]	[illegible]	
	J	[illegible]	[illegible]	[illegible]	[illegible]	
	K	[illegible]	[illegible]	[illegible]	[illegible]	
	L	[illegible]	[illegible]	[illegible]	[illegible]	
	M	[illegible]	REVISED PER ECO	[illegible]	[illegible]	
	N	1617	REVISED PER ECO	[illegible]	[illegible]	
	P	1728	REVISED PER ECO	[illegible]	[illegible]	
	Q	1738	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	Q	—	[illegible] PER ERN N00152	[illegible]	PG	[illegible]
	R	1781	REVISED PER ECO	KL		
	S	1785	REVISED PER ECO	MS		6-11-81
	T	1831	REVISED PER ECO	KL	[illegible]	[illegible]
	U	1853	REVISED PER ECO	KL	[illegible]	[illegible]
	V	1893	REVISED PER ECO	KL	[illegible]	[illegible]
	W	1980	REVISED PER ECO	KL	[illegible]	[illegible]
	X	2018	REVISED PER ECO	KL	[illegible]	[illegible]
	Y	2043	REVISED PER ECO	KL	[illegible]	[illegible]
	Z	2152	REVISED PER ECO	MS		[illegible]
	AA	2299	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	BB	2420	REVISED PER ECO	[illegible]	[illegible]	
	CC	2453	REVISED PER ECO	JWR	T.J.	[illegible]
	DD	2508	REVISED PER ECO	JWR	T.J.	[illegible]
	EE	2629	REVISED PER ECO	[illegible]		
	FF	2632	REVISED PER ECO	[illegible]		
	GG	2722	REVISED PER ECO	[illegible]		
	HH	2793	REVISED PER ECO	[illegible]		
	JJ	3516	REVISED PER ECO *	DGW		
	KK	3600A	REVISED PER ECO *	MW	DGW	[illegible]



LEFT SIDE

SEE DETAIL A



DETAIL A

REAR VIEW

REFERENCE PRINT

APR 22 1983

NOTE

1. R41, 87, 57, 54, 95, 96, 125, 63, 64 ARE TO BE MOUNTED ON THE FAR SIDE OF THE PCB.
2. DRILL OUT "C" HOLE (.125 DIA) ON XQ18 & XQ20.
3. SEE TOP ASSY 0285-0003.
4. (C22 & C23 TO BE MOUNTED ON THE SOLDER OF PCB)

DASH NO	NUMBER NEXT ASSEMBLY	QTY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP CORNERS. CLEAN IN ETCHING AND APPLY OVER ALL FINISHES EXCEPT PAINT SURFACE ALIGNMENTS

TOLERANCE

DIMENSIONAL: X ± ANGLES ±; .XX ± .030; .XXX ± .010; NOTE: .XX ± .01; .XXX ± .005; ANGLES ±0.5°

ENG SERV

DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DRAWN

DATE

CHECKED — 5/19/81

PROJ. ENG — 6/[illegible]

MANUFACTURING — 6/3/81

QUALITY ASSUR

GOULD biomation

TITLE A[illegible] ASSEMBLY [illegible] DRAWING PCB

SCALE 1/1

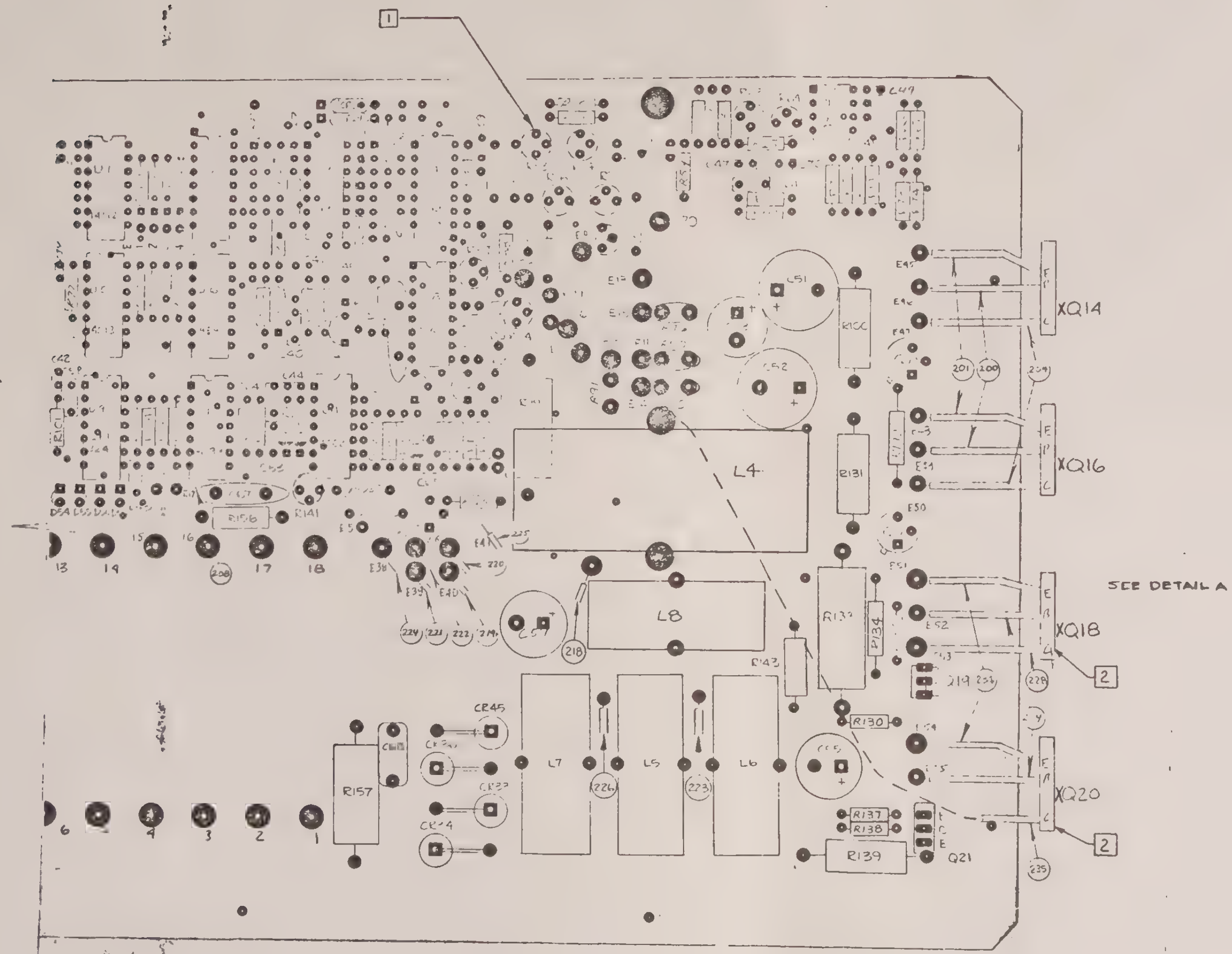
SIZE D

PART NUMBER [illegible]

REV KK

CODE [illegible]

SHEET 1 OF 2



RIGHT SIDE

DASH NO	NUMBER	Q'TY	NEXT ASSEMBLY

50	.40	30	.20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

TOLERANCE

DRAWN	[illegible]
CHECKED	
PROJ. ENG	
MANUFACTURING	
QUALITY ASSUR	
ENG. SERV	DATE

GOULD biomation

TITLE: ASSEMBLY POWER SUPPLY PWB

SCALE	SIZE	PART NUMBER	REV
2/1	D	[illegible]	KY

CODE [illegible] SHEET 2 OF 3

WIRE LIST				
WIRE Nº	FROM	TO	ITEM Nº	DESCRIPTION
1				[3]
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16	E16		208	BRN
17	E17		208	RED
18	E18	P3	216	TAN
19	E19	P4	216	TAN
20	E20		215	BLK
21	E21		214	VIO
22	E22		213	YEL
23	E23		212	ORG
24	E24		N/C	—
25	E25		[1]	[1]
26	E26		227	GRN/YEL
27	E27		[1]	[1]
28	E28		211	RED
29	E29		210	BRN
30	E30		211	RED
31	E31		210	BRN
32	E32	XQ7 E	201	RED
33	E33	XQ7 B	204	BLK
34	E34	XQ7 C	202	BLK
35	E35	XQ8 E	206	RED
36	E36	XQ8 B	205	BRN
37	E37	XQ8 C	207	BLK
38				
39	E39		221	ORG
40	E59		222	ORG
41	E40		219	RED
42	E60		220	RED
43				
44	E42		218	BRN
45	E43		223	YEL
46	E44		226	WHT/RED
47	E45	XQ14 E	201	RED
48	E46	XQ14 B	200	BRN
49	E47	XQ14 C	204	BLK
50	E48	XQ16 E	201	RED
51	E49	XQ16 B	200	BRN
52	E50	XQ16 C	204	BLK
53	E51	XQ18 E	234	RED
54	E52	XQ18 B	204	BLK
55	E53	XQ18 C	233	BLK
56	E54	XQ20 E	234	RED
57	E55	XQ20 B	204	BLK
58	E56	XQ20 C	235	BLK
59	E57	P1	216	BLK
60	E58	P2	216	BLK
61	E61	—	180	BRN
62	E62	-	181	RED
63	E70	-	214	VIO
64	T6	E71	—	WHT (IF USED)

DWG NO. [illegible] SH 2 REV KK

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND CHAMFER ON DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X 1 ANGLES; XX .020 1°; XXX .010; HOLE SIZE: 0 99 .003; 0.99 999 .004; 1.000 1.999 .005

ENG SERV | DATE

DRAWN | DATE

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

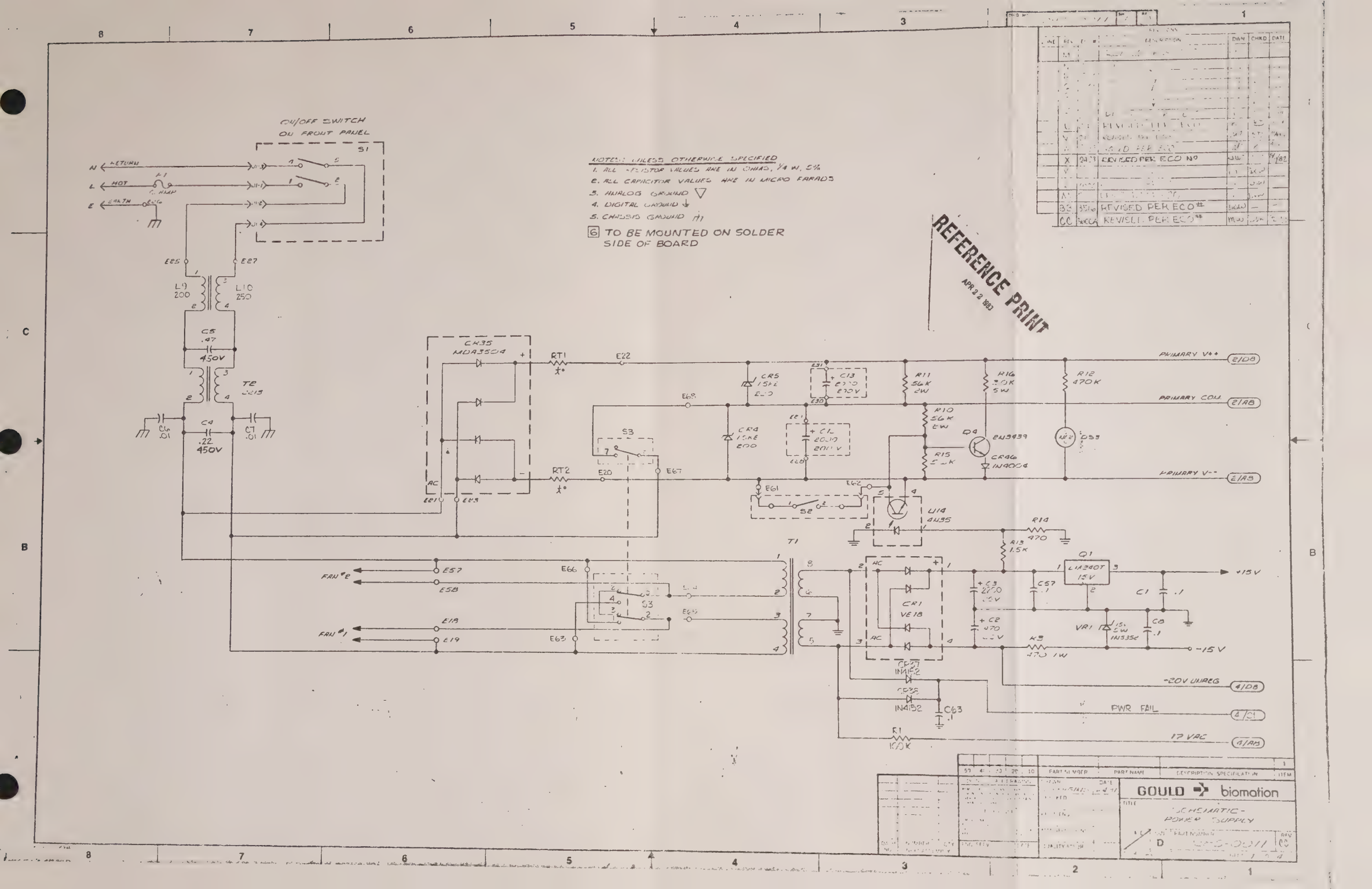
GOULD biomation

TITLE A[illegible]Y POWER SUPPLY P.W.B.

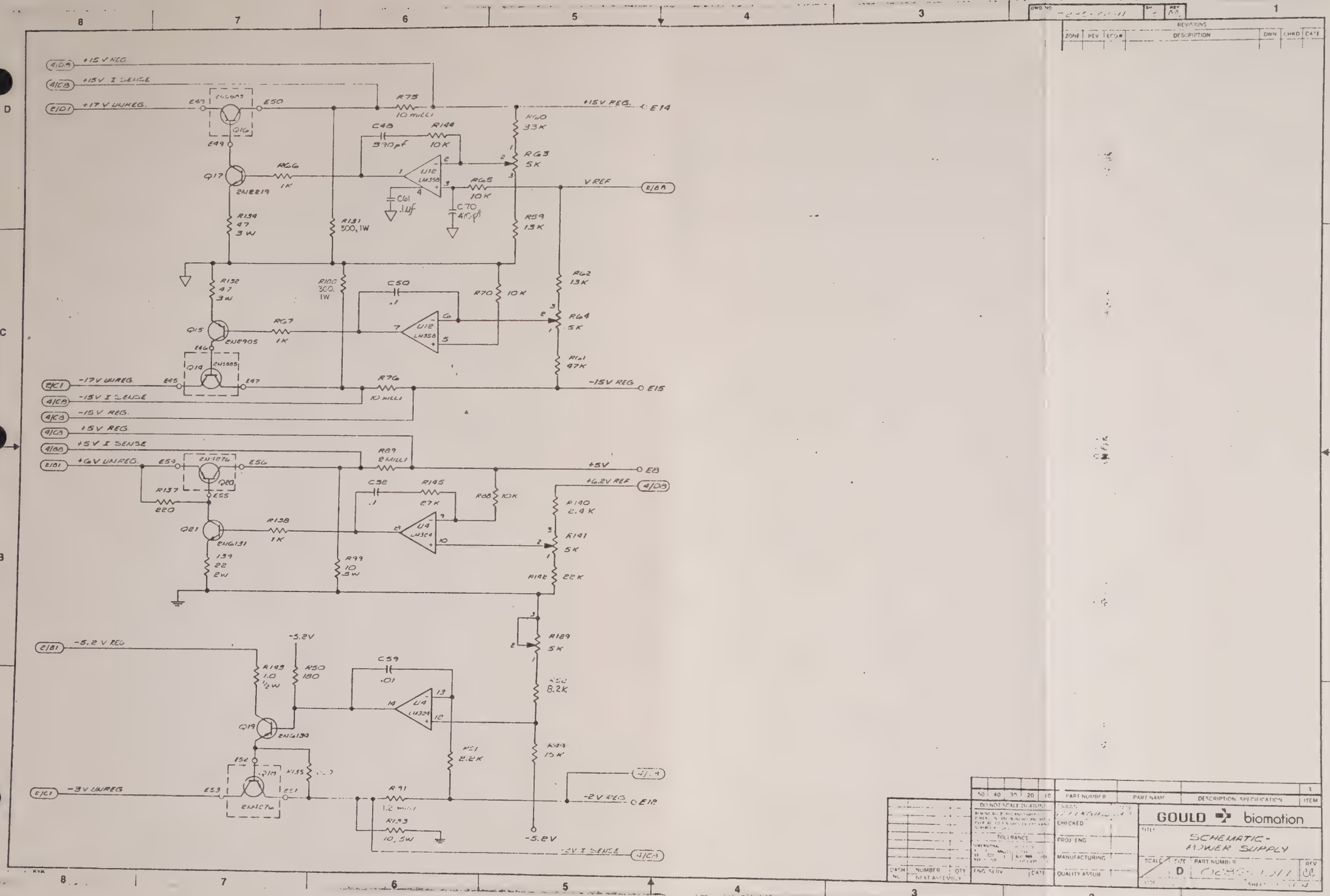
SCALE [illegible] | SIZE D | PART NUMBER [illegible] | REV KK

CODE [illegible] | SHEET [illegible] OF [illegible]

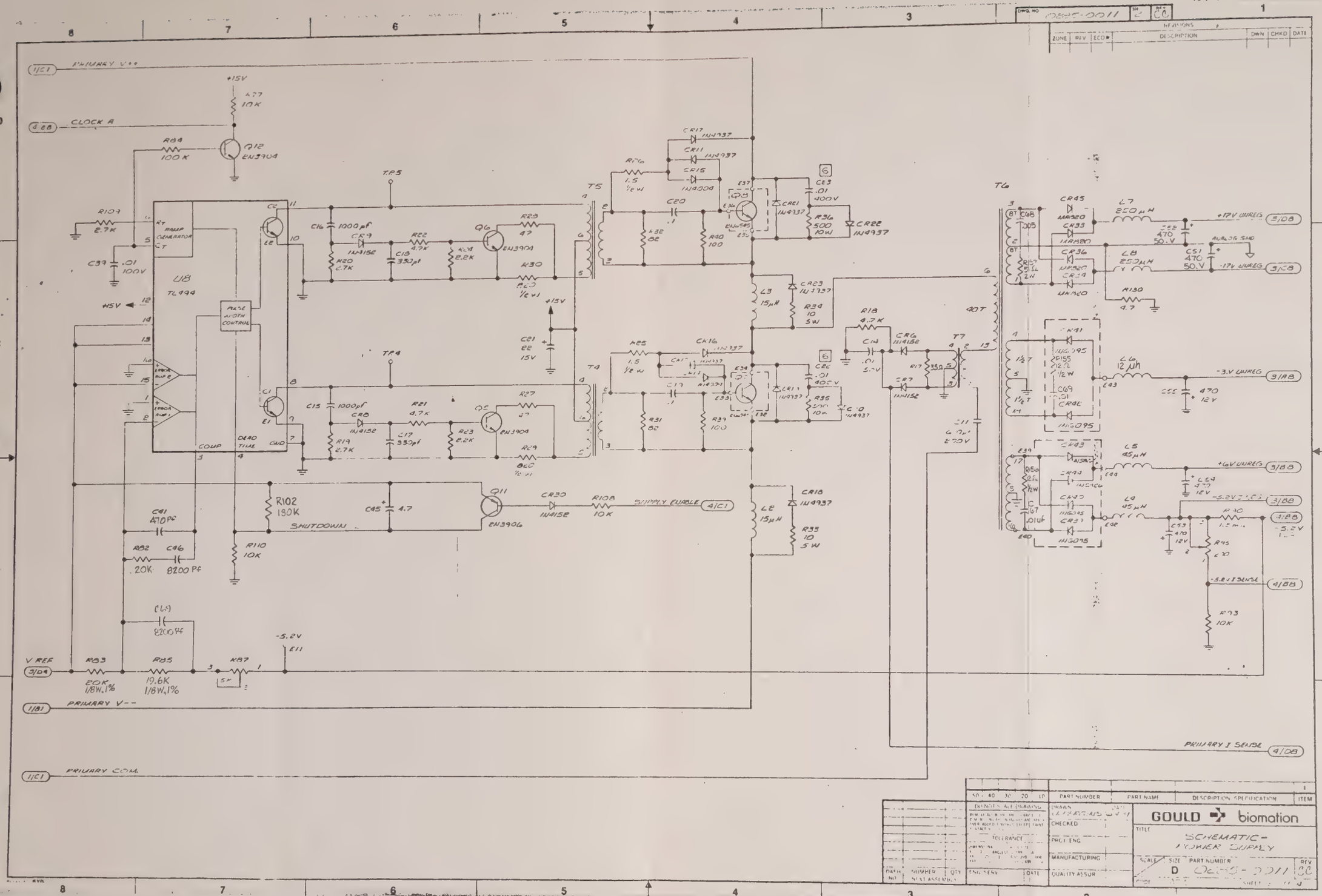
DASH NO | NUMBER | QTY | NEXT ASSEMBLY

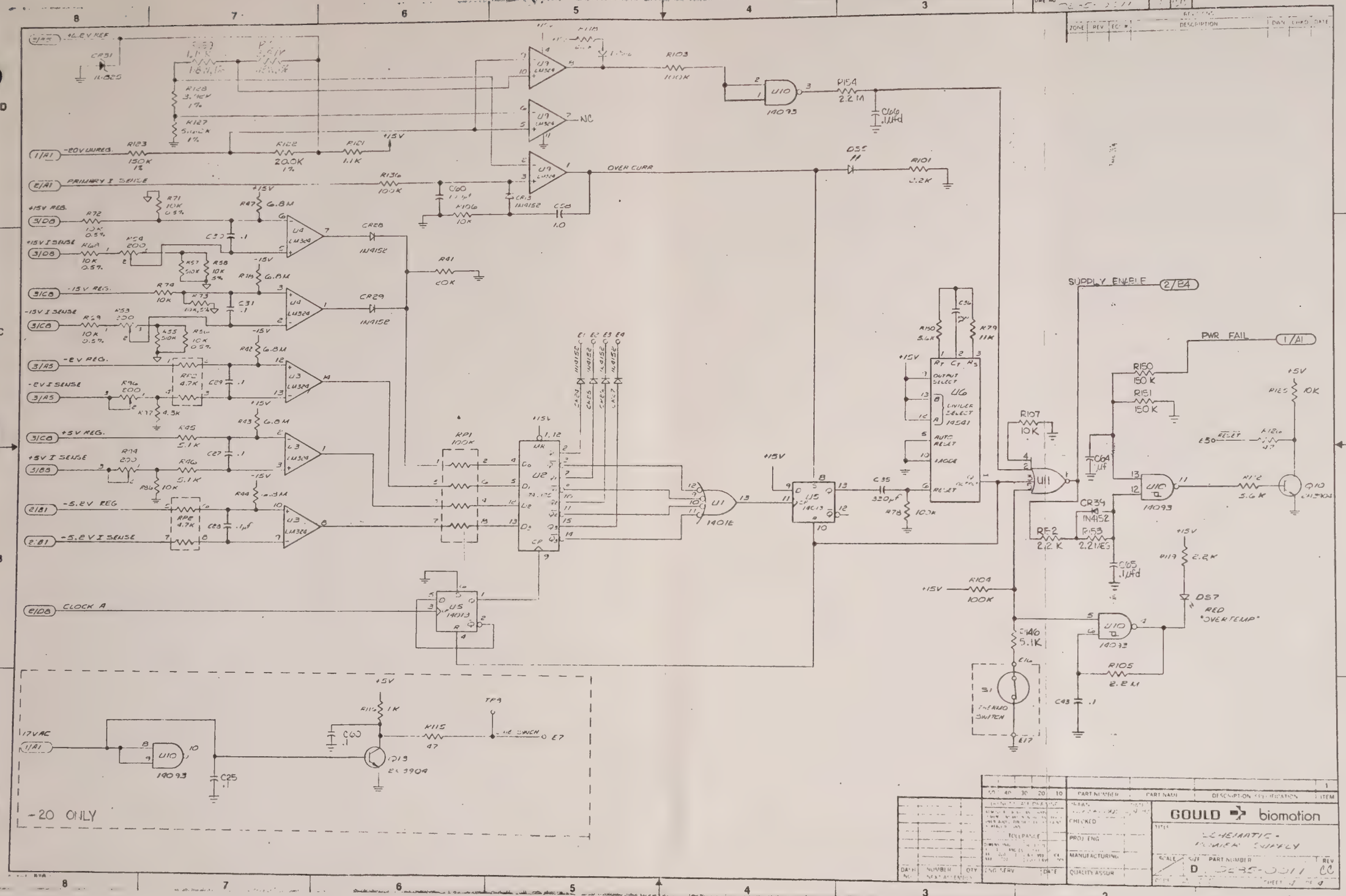


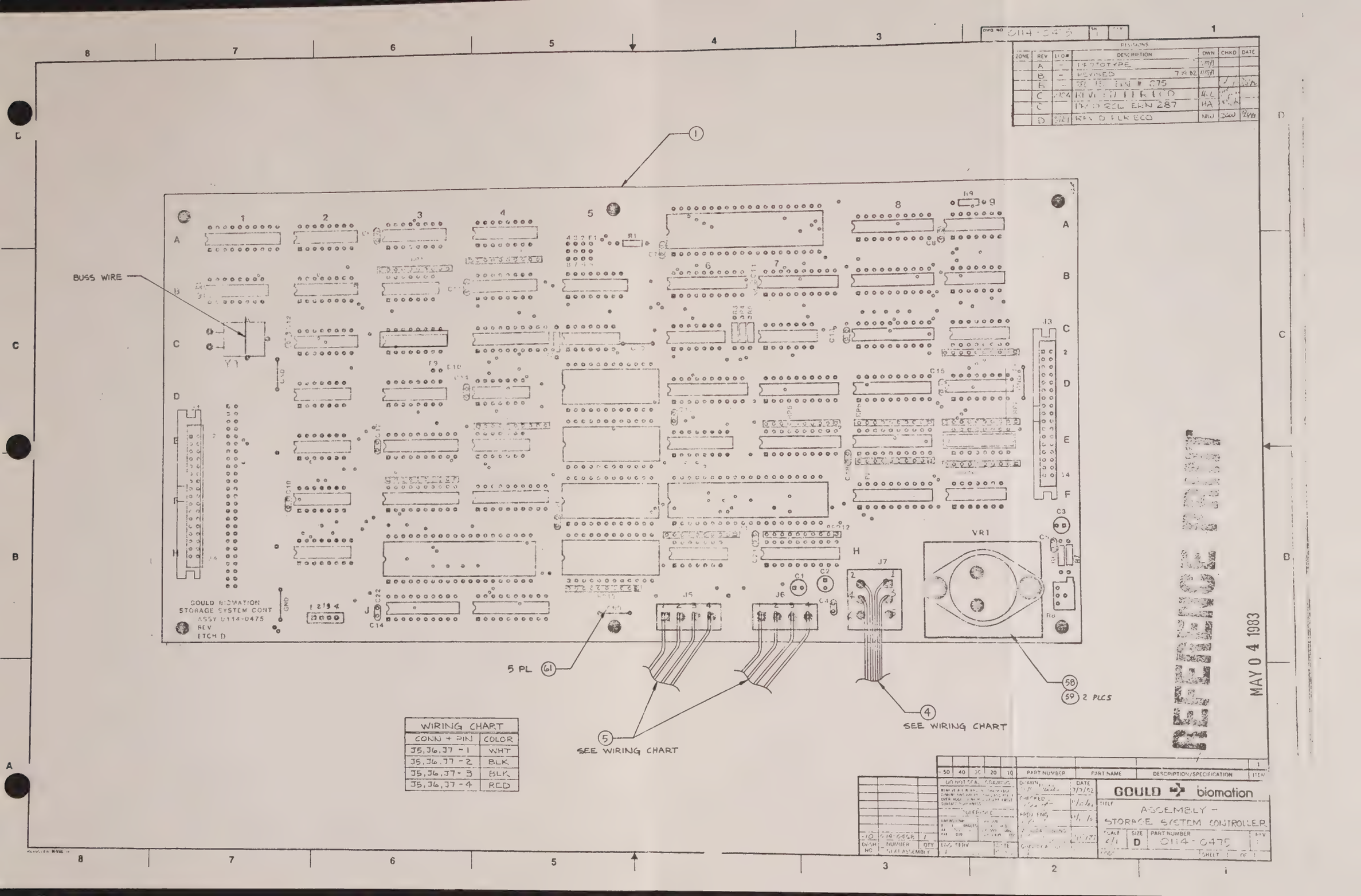
ON/OFF SWITCH
ON FRONT PANEL
S1
N RETURN
L HOT
E EARTH
F1
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS
3. ANALOG GROUND
4. DIGITAL GROUND
5. CHASSIS GROUND
6 TO BE MOUNTED ON SOLDER SIDE OF BOARD
REFERENCE PRINT
APR 22 1983
L9 200
L10 250
C5 .47 450V
T2
C4 .22 450V
C6 .01
C7 .01
CR35 MDA3504
RT1
RT2
E22
E20
E67
E68
CR5 15KE 200
CR4 15KE 200
C13 2000 200V
C12 2000 200V
R11 56K 2W
R10 56K 2W
R15
R16 30K 5W
R12 470K
Q4 2N3439
CR46 1N4004
DS3
PRIMARY V++ 2/D8
PRIMARY COM. 2/A8
PRIMARY V-- 2/A8
S3
S2
E61
E62
U14 4N35
R14 470
R13 1.5K
T1
FAN #2
FAN #1
E57
E58
E18
E19
E66
E63
CR1 VE18
C3 2200 25V
C2 470 25V
C57 .1
Q1 LM340T 15V
C1 .1
C8 .1
VR1 15V 5W 1N5352
R3 470 1W
+15V
-15V
CR37 1N4152
CR38 1N4152
C63 .1
R1 100K
-20V UNREG 4/D8
PWR FAIL 4/C1
17 VAC 4/A8
REVISED PER ECO #
GOULD biomation
SCHEMATIC - POWER SUPPLY
D



+15 V REG
+15V I SENSE
+17 V UNREG.
+15V REG.
E14
R75
10 MILLI
R60
33K
C48
390pf
R144
10K
R63
5K
Q16
Q17
2N2219
R66
1K
U12
LM358
R65
10K
V REF
C61
.1uf
C70
410pf
R134
47
3W
R131
300, 1W
R59
13K
R132
47
3W
R100
300,
1W
C50
.1
R70
10K
R62
13K
Q15
2N2905
R67
1K
R64
5K
R61
47K
Q14
2N5885
-17V UNREG.
-15V I SENSE
-15V REG.
R76
10 MILLI
-15V REG
E15
+5V REG.
+5V I SENSE
+6V UNREG.
R89
2 MILLI
+5V
E8
+6.2V REF
Q20
R137
220
C32
.1
R145
27K
R88
10K
R140
2.4K
Q21
2N6131
R138
1K
U4
LM324
R141
5K
R99
10
5W
R142
22K
-5.2 V REG
-5.2V
R143
1.0
1/2W
R50
180
C59
.01
R129
5K
R52
8.2K
Q19
2N6134
R51
2.2K
R49
15K
Q18
2N4276
-3V UNREG
R91
1.2 MILLI
R133
10, 5W
-2V REG
E12
-5.2V
-2V I SENSE
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC-
POWER SUPPLY
SCALE
SIZE
D
PART NUMBER
REV
SHEET


PRIMARY V++
CLOCK A
+15V
R77 10K
R84 100K
Q12 2N3904
R109 2.7K
C39 .01 100V
U8 TL494
RAMP GENERATOR
PULSE WIDTH CONTROL
ERROR AMP 2
ERROR AMP 1
COMP
DEAD TIME
GND
+5V
C16 1000pf
CR9 1N4152
R20 2.7K
R22 4.7K
C18 330pf
R24 2.2K
Q6 2N3904
R23 47
R30 8.0 1/2 W
TP5
T5
TP4
T4
C21 22 15V
C15 1000pf
CR8 1N4152
R19 2.7K
R21 4.7K
C17 330pf
R23 2.2K
Q5 2N3904
R27 47
R29 8.0 1/2 W
R102 180K
C45 4.7
SHUTDOWN
Q11 2N3906
CR30 1N4152
R108 10K
SUPPLY ENABLE
C41 470PF
R32 20K
C46 8200 PF
R110 10K
C49 8200PF
V REF
R83 20K 1/8W,1%
R85 19.6K 1/8W,1%
R87 5K
-5.2V
PRIMARY V--
PRIMARY COM.
R116 1.5 1/2 W
CR17 1N4937
CR11 1N4937
CR15 1N4004
C20 .1
R32 82
R40 100
Q8 2N6545
CR21 1N4937
C23 .01 400V
R36 500 10W
CR22 1N4937
L3 15µH
CR23 1N4937
R34 10 5W
R25 1.5 1/2 W
CR16 1N4937
CR17 1N4937
C19 .1
R31 82
R39 100
Q7 2N6545
CR21 1N4937
C26 .01 400V
R35 500 10W
C10 1N4937
CR18 1N4937
L2 15µH
R35 10 5W
R18 4.7K
C14 .01 50V
CR26 1N4152
R17 350
CR27 1N4152
T7
40T
C11 6.8µF 250V
T6
CR45 1N4820
L7 250µH
C68 .005
CR33 1N4820
C55 470 50V
+12V UNREG
ANALOG GND
CR36 1N4820
CR34 1N4820
L8 250µH
C51 470 50V
-12V UNREG
R130 4.7
R57 5.1 2W
CR41 1N5095
C69 .01
CR42 1N5095
L6 12µH
C55 470 12V
-3V UNREG
CR43 1N5095
L5 45µH
+6V UNREG
C54 470 12V
-5.2V I SENSE
CR44 1N5095
CR45 1N5095
L4 45µH
C53 470 12V
R30 1.5 min
R45 20
-5.2V
R93 10K
PRIMARY I SENSE
PRIMARY COM.
GOULD biomation
SCHEMATIC - POWER SUPPLY
D
D2CS-0011
REVISIONS
ZONE REV ECO DESCRIPTION DWN CHKD DATE
PART NUMBER PART NAME DESCRIPTION SPECIFICATION ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
TOLERANCE
DO NOT SCALE DRAWING


+6.2V REF
CR31
1N829
R128 3.16K 1%
R127 5.11K 1%
-20V UNREG.
R123 150K 1%
R122 20.0K 1%
R121 1.1K
+15V
PRIMARY I SENSE
R136 100K
C60
R106 10K
CR13 1N4152
C58 1.0
U9 LM324
NC
OVER CURR
R103 100K
U10 14093
R154 2.21M
C66 .1µfd
DS5
R101 6.2K
+15V REG.
R72 10K 0.5%
R71 10K 0.5%
R67 6.8M
U4 LM324
C32 .1
CR28 1N4152
+15V I SENSE
R68 10K 0.5%
R56 200
R57 510K
R58 10K 0.5%
-15V
R41 20K
-15V REG.
R74 10K
R73 10K,5%
R75 6.8M
C31 .1
CR29 1N4152
-15V I SENSE
R29 10K 0.5%
R53 200
R55 510K
R54 10K 0.5%
-2V REG.
R42 6.8M
U3 LM324
C29 .1
-2V I SENSE
R96 200
R97 4.3K
RP2 4.7K
+5V REG.
R95 5.1K
R43 6.8M
C27 .1
+5V I SENSE
R94 200
R96 5.1K
R86 10K
-5.2V REG
R44 6.8M
RP6 4.7K
C28 .1µf
-5.2V I SENSE
CLOCK A
U5 14013
RP1 100K
U2 LM324
E1 E2 E3 E4
CR23 CR25 CR26 CR27
U1 14012
U5 14013
C35 330µf
R78 10K
U6 LM1458 SELECT 14541
OUTPUT SELECT
AUTO RESET
RESET
R50 5.6K
R79 11K
C56
SUPPLY ENABLE
2/E4
PWR FAIL
1/A1
R150 150K
R151 150K
+5V
R165 10K
E50
R112 5.6K
Q10 2N3904
U11
R107 10K
C64 .1µf
CR34 1N4152
R52 2.2K
R53 2.21MEG
C65 .1µfd
R119 2.2K
DS7 RED "OVERTEMP"
R104 100K
R146 5.1K
S1 THERMO SWITCH
R105 2.2M
C43 .1
17VAC
1/A1
U10 14093
C25 .1
R112 1K
C60 .1
Q13 2N3904
R115 47
TP9
-20 ONLY
GOULD biomation
SCHEMATIC - POWER SUPPLY
D
DC85-0011
CC



DWG NO 0114-0475
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
A - PROTOTYPE
B - REVISED 7-19-82
C - REV D PER ECO
C PROD RCL ERN 287
D REV D PER ECO
BUSS WIRE
Y1
GOULD BIOMATION
STORAGE SYSTEM CONT
ASSY 0114-0475
REV
ETCH D
VR1
J3
J5
J6
J7
5 PL 61
5 SEE WIRING CHART
4 SEE WIRING CHART
58
59 2 PLCS
REFERENCE PRINT
MAY 0 4 1983
WIRING CHART
CONN + PIN COLOR
J5,J6,J7 - 1 WHT
J5,J6,J7 - 2 BLK
J5,J6,J7 - 3 BLK
J5,J6,J7 - 4 RED
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DO NOT SCALE DRAWING
GOULD biomation
TITLE ASSEMBLY - STORAGE SYSTEM CONTROLLER
SCALE 2/1 SIZE D PART NUMBER 0114-0475 REV
DASH NO NUMBER QTY
NEXT ASSEMBLY

ITEM	-90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME DESCRIPTION	REFERENCE DESIGNATION	E/M
1									1	0114-0477	PWB		
2									1	0114-0474	I.C. PROM 32x8	3C	
3									1	0114-0479	I.C. PROM 256x4	9E	
4									1	0114-0429	Cable Assy, POWER IN	J7	
5									2	0114-0481	Cable Assy, FDC to Floppy	J5, J6	
6									1	1700-0109	I.C. LM350K 3 AMP	VR1	
7									2	1800-0085	I.C. 7407 HEX O.C. BUFFER	2E, 2F	
8									1	-0097	I.C. 7406 HEX O.C. INVERTER	2D	
9													
10									1	-0106	I.C. 74LS02 QUAD 2-IN NOR	5C	
11									1	-0109	I.C. 74LS08 QUAD 2-IN AND	7C	
12									1	-0110	I.C. 74LS10 TRIPLE 3-IN NAND	9F	
13									5	-0115	I.C. 74LS74 DUAL D FLIP-FLOP	6C, 9A, 4E, 4D, 3B	
14									5	-0125	I.C. 74LS161 4 BIT COUNTER	4A, 4B, 5B, 3A, 2C	
15									1	-0181	I.C. 74LS151 8-IN MUX	3D	
16									3	-0193	I.C. 74LS138 1 OF 8 DECODER	6E, 9C, 9D	
17									1	-0216	I.C. 74LS32 QUAD 2-IN OR	6H	
18									2	-0217	I.C. 74LS153	2A, 2B	
19									4	-0231	I.C. 74LS273 OCTAL REGISTER	8D, 8C, 3E, 4C	
20									1	-0237	I.C. 74LS139 DUAL 1 OF 4 DECODER	2H	
21									3	-0240	I.C. 74LS244 OCTAL BUFFER	6D, 8A, 8B	
22									3	-0267	I.C. 74LS240 OCTAL INVERTER	7B, 3F, 4F	
23									3	-0268	I.C. 74LS245 OCTAL BI-DIR BUFFER	8F, 8E, 7D	
24									1	-0293	I.C. 74LS374 OCTAL REGISTER	7H	
25									1	-0298	I.C. 74LS373 OCTAL LATCH	7E	
26									1	-0311	I.C. 7438 QUAD O.C. NAND	9B	
27									1	1800-0313	I.C. 1863 UART	6A	

REV	DESCRIPTION	DATE	DWN	CKD
A				
B	REVISED	7/6/82	[illegible]	
C	[illegible]	[illegible]	[illegible]	[illegible]
D	[illegible]	[illegible]	[illegible]	[illegible]

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-10	0114-0468	1

		DATE
DWN	Curt	5-25-82
CHK	Curt	11-12-82
ENGR	Curt	11-12-82
MFG.	P. Strassman	11/12/82
Q.A.	[illegible]	11-12-82

LIST OF MATERIAL

PWB ASSEMBLY

STORAGE SYSTEM CONTROLLER

GOULD biomation

B 0114-0475 REV D

MODEL SHEET 1 OF 3

KLINGLER K-VEL H-10

	-90	-80	-70	-60	-50	-40	-30	-20	-10			
28									1	1800 - 0342	I.C. 8272 FLOPPY CONT.	3H
29									1	1800 - 0357	I.C. 74LS629 OSCILLATOR	1B
30									1	1800 - 0358	I.C 8257-5 DMA CONT.	6F
31												
32												
33												
34									4	1820 - 0080	I.C. 6116LP-3 2KX8 RAM	5D, 5E, 5F, 5H
35												
36									1	3000 - 1500	RESISTOR, 150Ω, 1/4W, 5%	R1
37									1	3000 - 1001	RESISTOR, 1K, 1/4W, 5%	R7
38									5	3000 - 2201	RESISTOR 2.2K, 1/4W, 5%	R2-5,9
39									1	3000 - 6806	RESISTOR 68Ω, 1/4W, 5%	R6
40									1	3300 - 0092	POT., 100Ω, 12 T	R8
41									8	3700 - 0048	R. PACK 3K/6.2K, 10 PIN, 8 RES	RP3,5,6,9-13
42									4	3700 - 0083	R. PACK 2.2K, 10 PIN, 9 RES	RP1,2,4,7
43									1	3700 - 0100	R. PACK 150Ω, 10 PIN, 9 RES	RP8
44												
45									18	4010 - 0103	CAP .01 μd, 50 V, 10%	C4-22
46									1	4400 - 0043	CAP 47. μf/16 V	C1
47									2	4400 - 0045	CAP 33. μf/25V	C2,3
48												
49									1	5100 - 0021	CRYSTAL, 16. MHZ	Y1
50									1	6000 - 0385 - 04	HEADER, 4 PIN, KEYBOARD IN	J4
51												
52									2	6000 - 0574	CONNECTOR, 34 PIN HEADER	J1, J3
53												
54									4	6100 - 0122	SOCKET, 24 PINS	X5D, X5E, X5F, X5H
55									3	6100 - 0123	SOCKET, 40 PINS	6A, 6F, 3H
56									2	6100 - 0120	SOCKET, 16 PIN DIP, LP	3C, 9E
57												

NOTES

LIST OF MATERIAL

GOULD biomation

B 0114-0475 REV L

MODEL SHEET 2 OF 2

KLINGLER K-VEL H-10

	-90	-80	-70	-60	-50	-40	-30	-20	-10			
58									1	7000-0460-20	HEATSINK, TO-3, Bottom	for VR1
59									2	7071-0632-00	KEPNUT, 6-32	
60												
61									5	9000-0054	WIRE, FORMED GND POINT	

NOTES

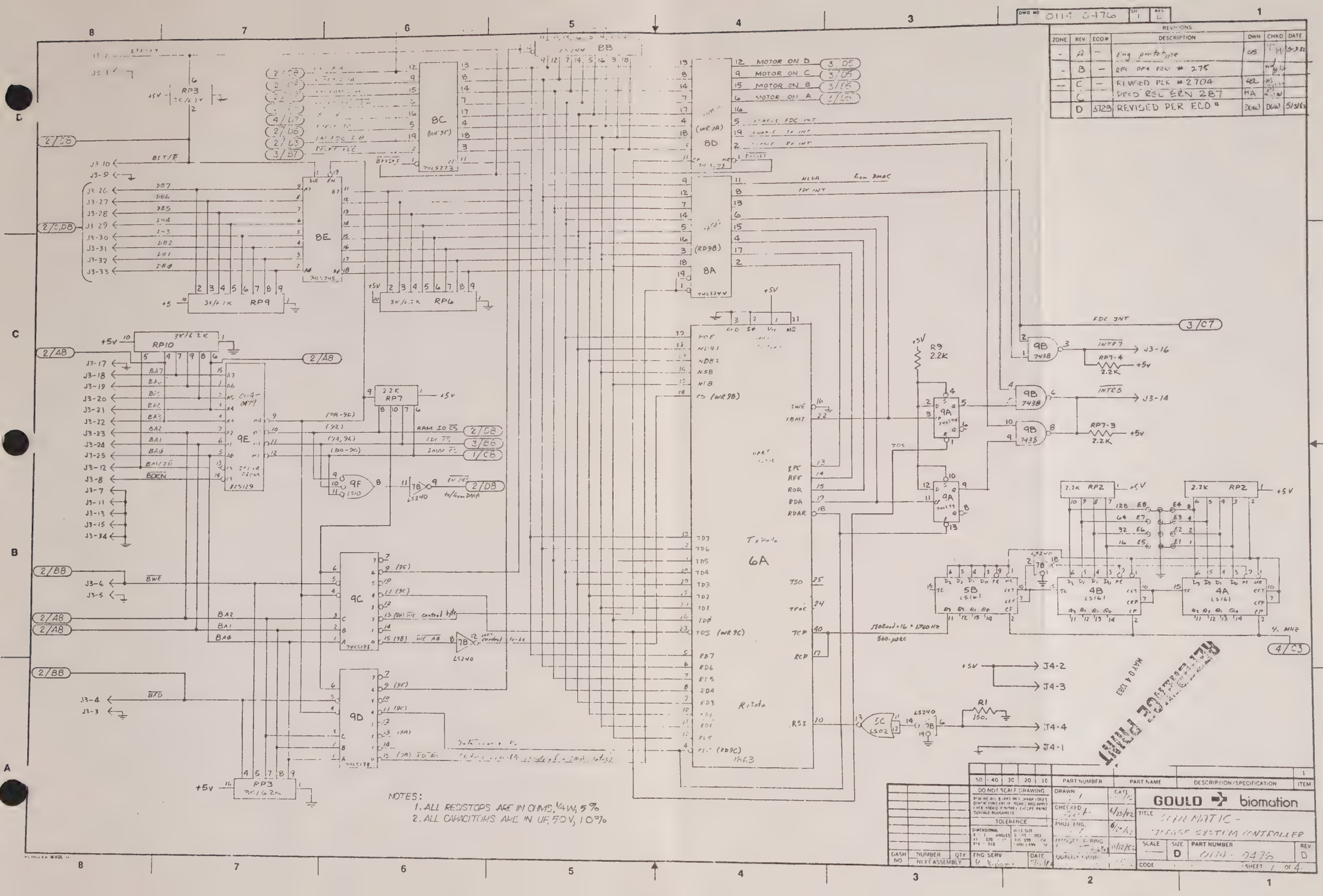
LIST OF MATERIAL

GOULD biomation

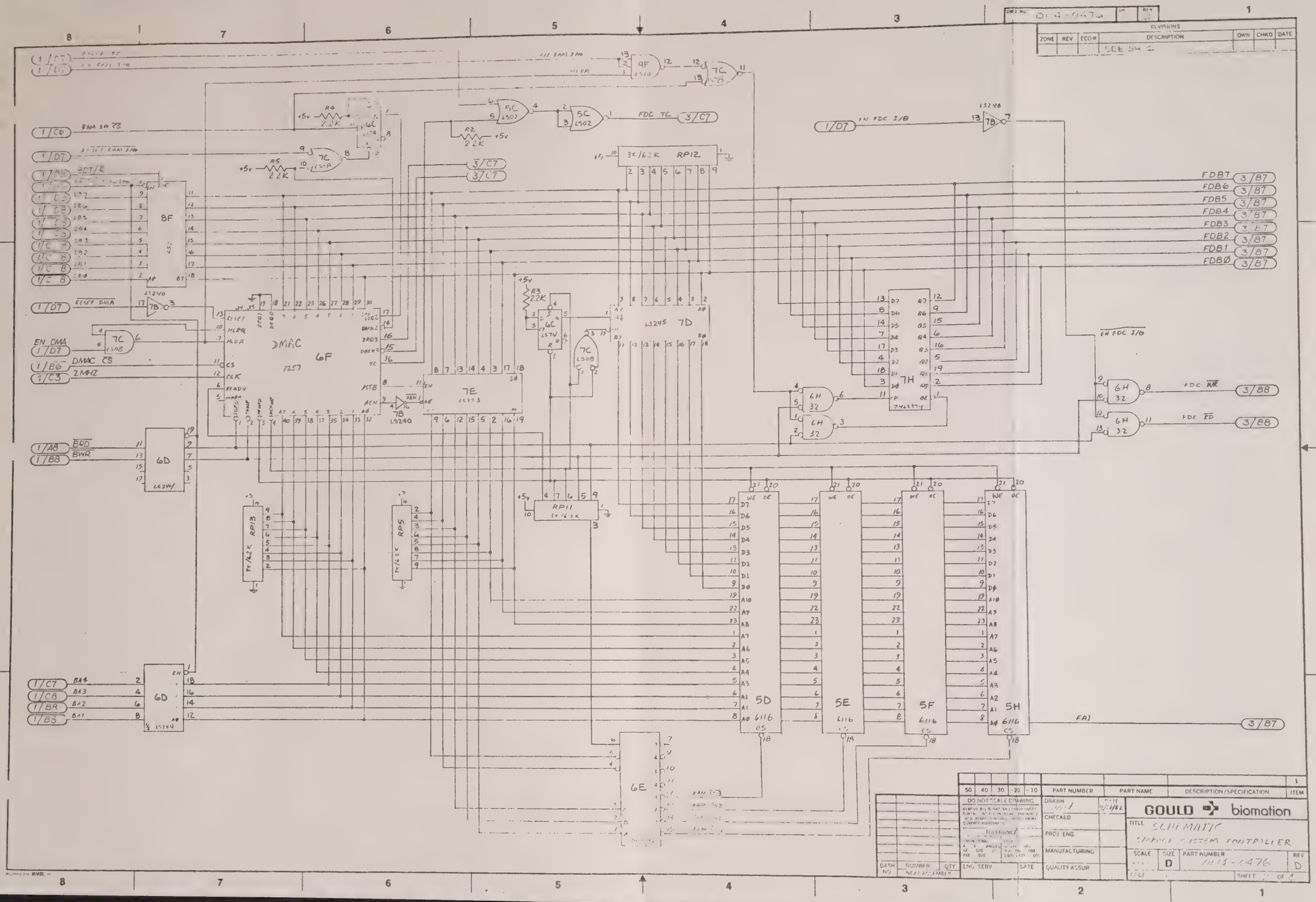
B 0114-0475 REV

MODEL SHEET 3 OF 3

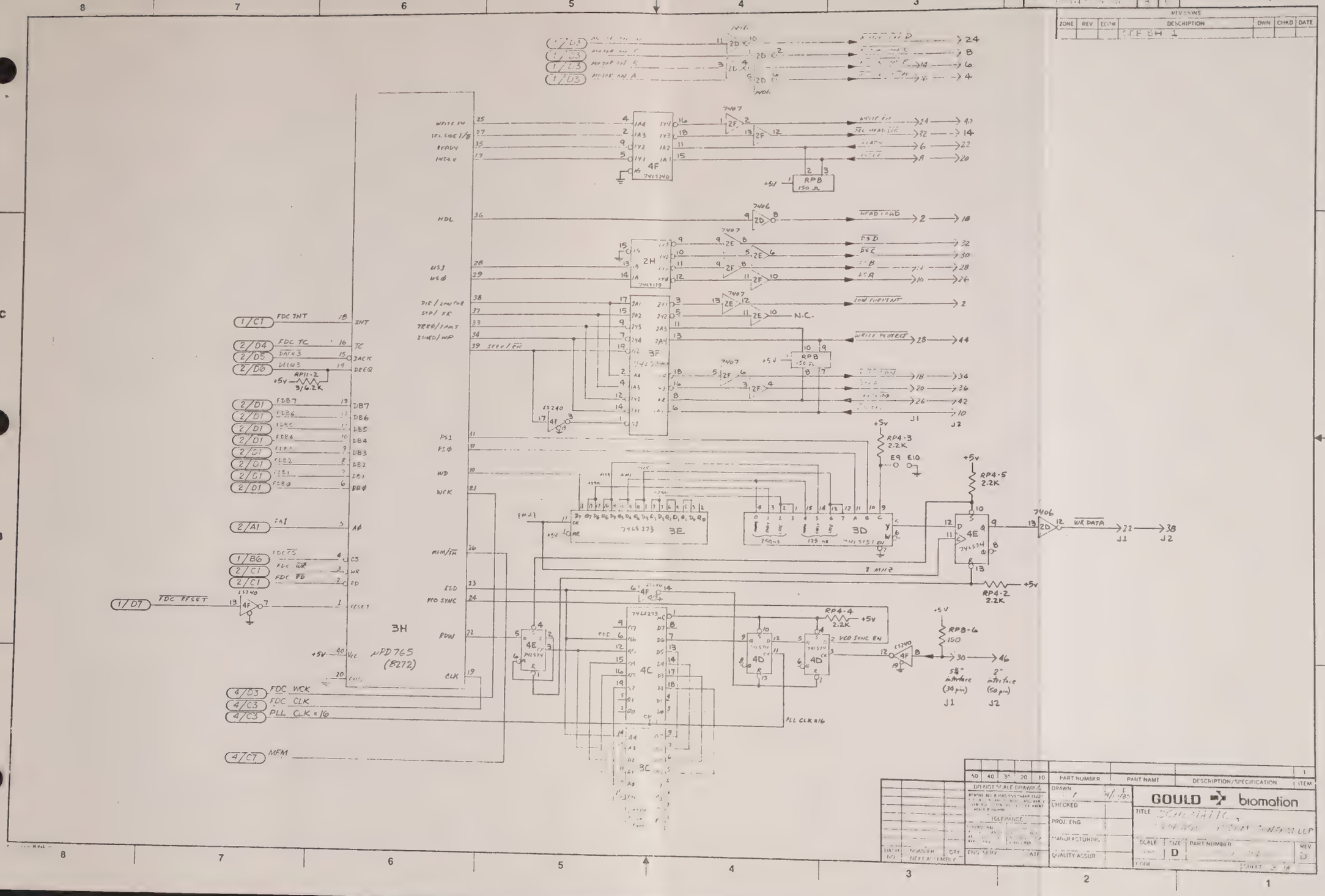
KLINGLER K-VEL H-10



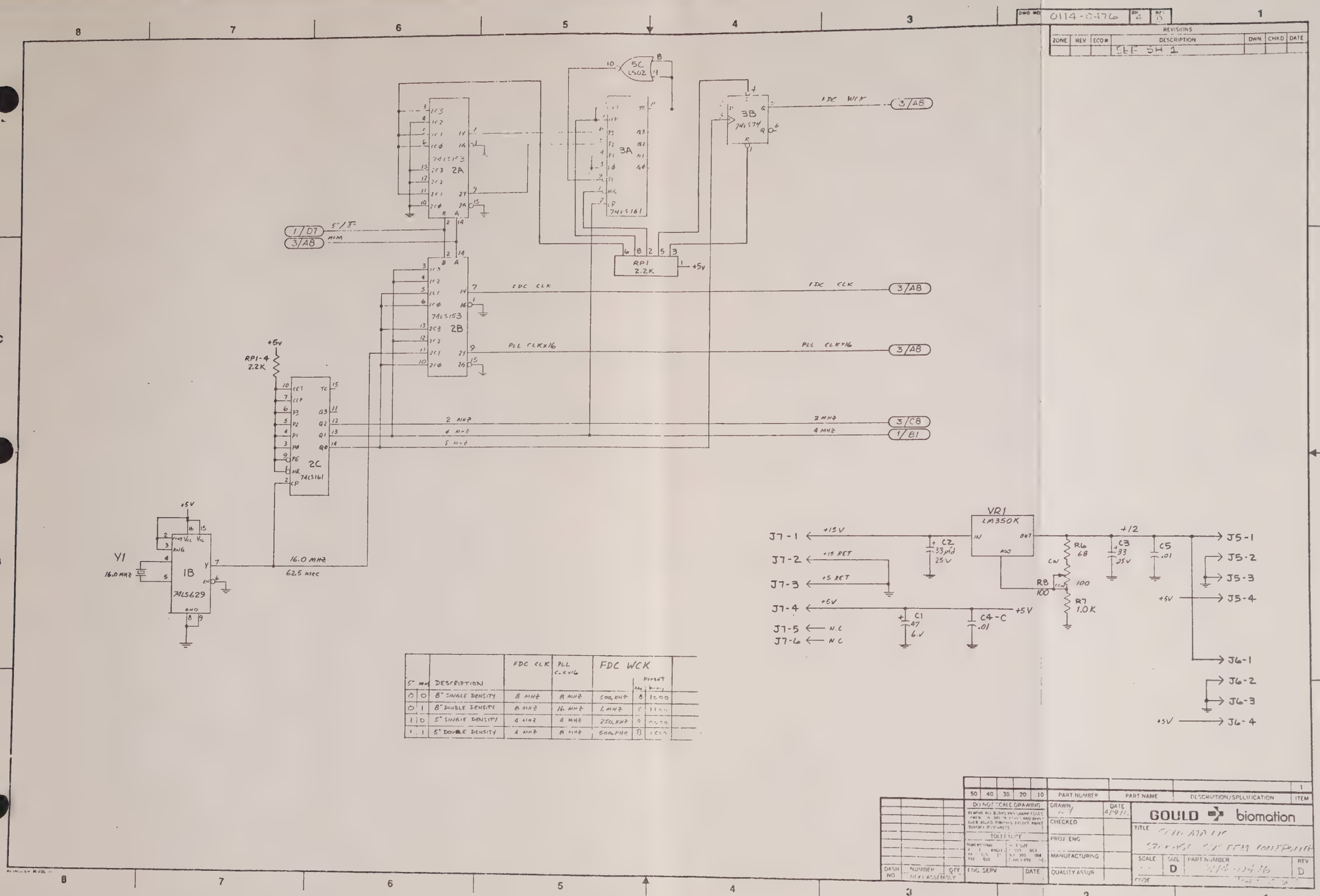
DWG NO 0114-0476
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
- | A | - | Eng prototype | GB | | 6-3-82
- | B | - | REC PER ERN # 275
- | C | - | REVISED PER # 2704 | HA
C | | PROD REL ERN 287 | HA
D | 3729 | REVISED PER ECO # | DGW | DGW | 5/3/83
MOTOR ON D
MOTOR ON C
MOTOR ON B
MOTOR ON A
8C
8D
8E
8A
8B
9A
9B
9C
9D
9E
9F
6A
5B
4B
4A
5C
RP3
RP9
RP6
RP10
RP7
RP2
RP7-4
RP7-3
RAM IO CS
FDC CS
DMAC CS
FDC INT
INTR7
INTR5
J3-16
J3-14
J4-2
J4-3
J4-4
J4-1
4. MHZ
NOTES:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE IN UF, 50V, 10%
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR.
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC - STORAGE SYSTEM CONTROLLER
SCALE
SIZE D
PART NUMBER 0114-0476
REV D
CODE
SHEET 1 OF 4
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE



REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SH 1
DMAC 6F 7257
LS245 7D
LS240
LS244
LS245
LS374
LS08
LS02
LS07
LS08
LS74
LS374
RP11
RP12
RP13
RP5
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP13
RP5
6D
6E
6F
6H
7B
7C
7D
7E
7H
8F
5D
5E
5F
5H
6116
FDB7
FDB6
FDB5
FDB4
FDB3
FDB2
FDB1
FDBØ
FDC TC
EN FDC I/O
FDC WR
FDC RD
FA1
EN DMA
DMAC CS
2MHZ
BRD
BWR
BA4
BA3
BA2
BA1
RESET DMA
BDT/R
RAM I/O CS
DO NOT SCALE DRAWING
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC
STORAGE SYSTEM CONTROLLER
SCALE
SIZE D
PART NUMBER 0114-0476
REV D
SHEET



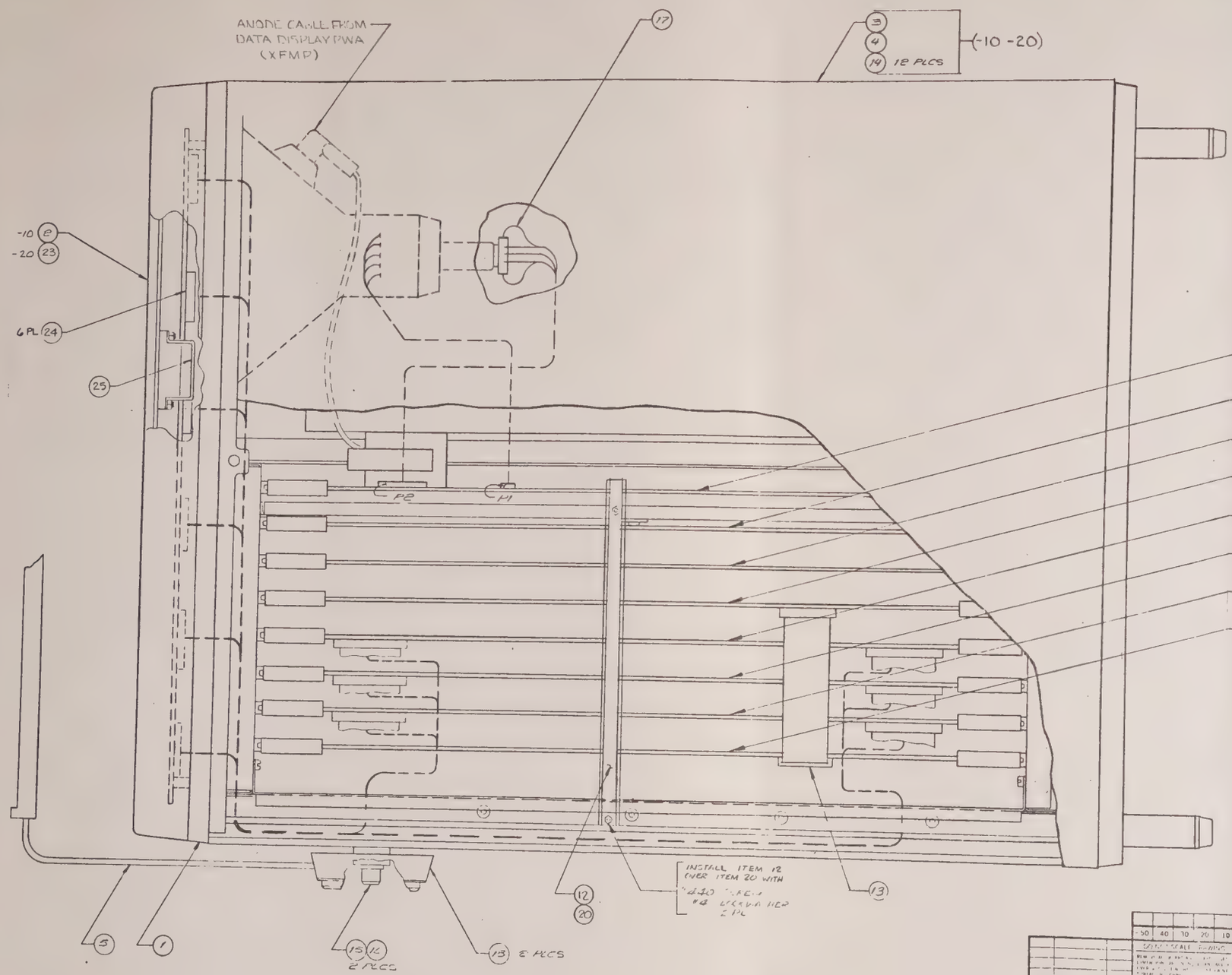
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SCE SH 1
WRITE EN
SEL SIDE 1/B
READY
INDEX
HDL
US1
US0
DIR / LOW CUR
STP / FR
TRK0 / FAULT
2SIDED / WP
SEEK / RW
FDC INT
FDC TC
DACK3
DREQ3
RP11-2
3/6.2K
FDB7
FDB6
FDB5
FDB4
FDB3
FDB2
FDB1
FDB0
FA1
FDC CS
FDC WR
FDC RD
FDC RESET
FDC WCK
FDC CLK
PLL CLK x16
MFM
INT
TC
DACK
DREQ
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
A0
CS
WR
RD
RESET
Vcc
CLK
3H
μPD765
(8272)
PS1
PS0
WD
WCK
MFM/FM
RDD
VCO SYNC
RDW
4F
74LS240
2H
74LS139
3F
74LS240
RP8
150 Ω
7407
7406
HEAD LOAD
DSD
DSC
DSB
DSA
LOW CURRENT
N.C.
WRITE PROTECT
J1
J2
RP4-3
2.2K
E9
E10
RP4-5
2.2K
3E
74LS273
3D
74LS151
4E
74LS74
WR DATA
8 MHZ
RP4-2
2.2K
RP4-4
2.2K
VCO SYNC EN
4C
4D
RP8-6
150
5¼" interface
(34 pin)
8" interface
(50 pin)
PLL CLK x16
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ. ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
SCALE
SIZE
D
PART NUMBER
REV
D
CODE
SHEET



5" MIN		DESCRIPTION	FDC CLK	PLL CLKx16	FDC WCK	Preset Adj	Preset binary
0	0	8" SINGLE DENSITY	8 MHZ	8 MHZ	500 KHZ	8	1000
0	1	8" DOUBLE DENSITY	8 MHZ	16 MHZ	1 MHZ	C	1100
1	0	5" SINGLE DENSITY	4 MHZ	4 MHZ	250 KHZ	0	0000
1	1	5" DOUBLE DENSITY	4 MHZ	8 MHZ	500 KHZ	8	1000

DWG NO 014-0002 SH 1 REV

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL PER ECN 10[illegible]	JAP	[illegible]	
	B	1851	REVISED PER ECO	JWC	[illegible]	9-4-81
	C	1889	REVISED PER ECO #	JWC	[illegible]	8-4-81
	D	[illegible]	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	[illegible]	—	[illegible] ECN # 20[illegible]	[illegible]	[illegible]	[illegible]
	E	[illegible]	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	F	2387	REVISED PER ECO NO	[illegible]	TJ	[illegible]
	G	2614	REVISED PER ECO N#	JGW	[illegible]	[illegible]
	H	[illegible]	REVISED PER ECO N#	[illegible]	JGW	[illegible]
	J	3082	REVISED PER ECO	[illegible]	JGW	[illegible]



24 DATA DISPLAY PWB (-10 -20)
9 DATA DISPLAY PWB ASSY (-40)
27 MPU PWB ASSY (-40)
11 MPU PWB ASSY (-10 -20)
10 GPIB/RS232 PWB ASSY
8 CLOCK PWB ASSY
6 H.S DATA PWB ASSY
6 H.S DATA PWB ASSY
6 H.S DATA PWB ASSY
7 RECORD CONTROL PWB ASSY

REFERENCE PRINT
MAY 09 1983

DASH NO	NUMBER NEXT ASSEMBLY	QTY

-50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN [illegible] CHECKED [illegible] ENGR ENG [illegible] ENG SERV [illegible]

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TITLE TOP ASSEMBLY

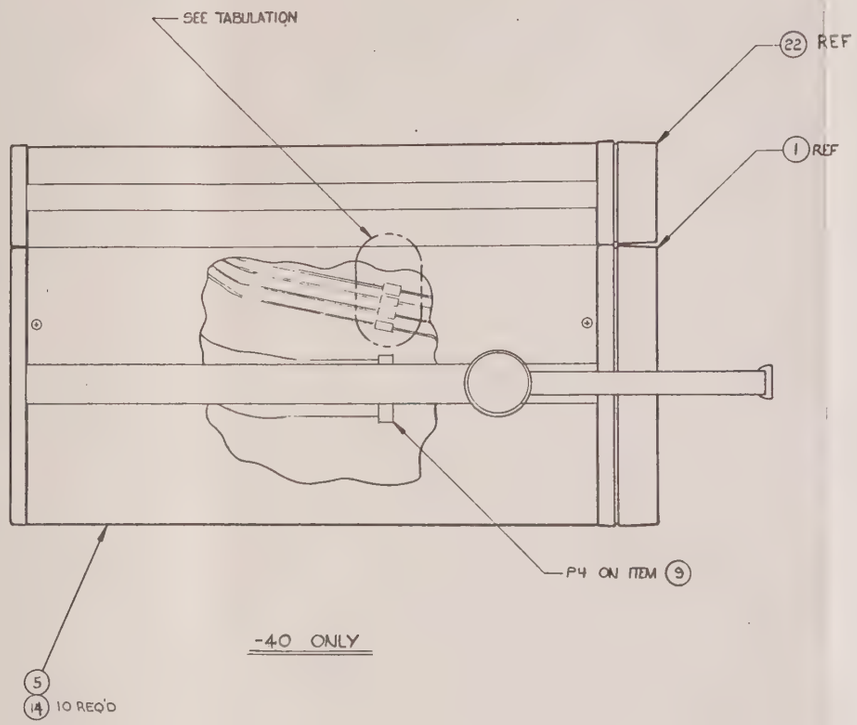
SCALE FULL SIZE D PART NUMBER 014-0002 REV J

CODE ID NO SHEET 1 OF 2

DWG NO.	SH	REV
0114-0		J

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH 1			



-40 ONLY

TABULATION

STORAGE SYS PWR CABLE	COLOR	PWR. SUPPLY CABLE TO MOTHERBOARD	DESCRIPTION
J7 – 1	WHT	J22 – 3	+ 15 V
J7 – 2	BLK	J22 – 2	GND
J7 – 3	BLK	J23 – 10	GND
J7 – 4	RED	J23 – 9	+ 5V

50	-40	30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .3 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0.599 ± .003; 800.999 ± .004; 1.000 ± .499 ± .005

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV. | DATE

DRAWN | DATE

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: TOP ASSY

SCALE	SIZE	PART NUMBER	REV
1/2	D	0114-0002	J

CODE K101 + STORAGE SYS | SHEET 2 OF 2

		COST	COST
-10 AID KEYBOARD			
-20 K100 TYPE KY BD.			
-30 - VOID -			
-40 NEW DISPLAY BD. (STORAGE SYS)			

	60	-50	-40	-30	-20	-10			REF. DESIGNATION	VENDOR NO.	DESC	
1			1		1	1	0114-0003	CHASSIS ASSY				LM
2			1		—	1	0114-0008-10	BEZEL ASSY			AID PANEL KEY BD	LM
3			1		1	1	0114-0039-10	COVER, TOP				
4			1		1	1	0114-0039-20	COVER, BOTTOM				
5			1		1	1	0111-0016	HANDLE ASSY				LM
6			3		3	3	0114-0110	HS. DATA PWB ASSY (10422)				LM
7			1		1	1	0114-0120-10	RECORD CONTROL PWB ASSY (10422)				LM
8			1		1	1	0114-0160	CLOCK PWB ASSY				LM
9			1		—	—	0114-2010-20	DATA DISPLAY PWB ASSY				LM
10			1		1	1	0114-0170-20	GPIB/RS232 PWB ASSY				LM
11			—		1	1	0114-0185-20	MPU PWB ASSY				LM
12			1		1	1	0114-0049	CARD RETAINER BKT				
13			1		1	1	0114-0054	CABLE, CONTROL BD TO CLOCK BD				LM
14			10		12	12	7000-0368	SCREW			#6-32 x 3/8" LG 100° FLT HEAD	
15			2		2	2	7000-0376	SOC. HD CAP SCR.			1/4"-20 x 3/4" LG	
16			2		2	2	———	WASHER			1/4" SPLIT LOCK, HEL.	
17			1		1	1	0950-0042	CRT CABLE ASSY				LM
18			2		2	2	0111-0059	BAIL, KNOB				

MAY 09 1983

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PILOT REL ECN #0103	2/4/81	JKP	RG	
B	REVISED PER ECO # 1871	8-1-82	JHS	RD	
C	REVISED PER ECO 1888	8-4-81	JHS	RD	
D	REVISED PER ECO 1877	8/25/82	RG	RG	
D	REL TO PROD ECN # 203	10/7/	[illegible]	RG	
E	REVISED PER ECO # 2188	11/4/8	RG	RD	
F	REVISED PER ECO NO 2349	3/3/83	[illegible]	TJ	

DASH NO.	NUMBER	QTY
-20	0114-0001-20	1
-10	0114-0001-10	1

NEXT ASSEMBLY

		DATE
DRAWN	J. PERGINS	2/4/81
CHECKED	RG	3/8/81
ENGINEER	Curt	10.8.81
MANUFACTURING	[illegible]	10/6/81
QUALITY ASSURANCE	[illegible]	[illegible]

LIST OF MATERIAL

TOP ASSEMBLY

MODEL

biomation

B 0114-0002 REV J

CODE K101 SHEET 1 OF 2

		COST	COST

	60	-50	-40	-30	20	-10	PART NO.	DESCRIPTION	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19												
20			1		1	1	0114-0047	CARD RETAINER				
21			1		1	1	7300-0029	FUSE			7A (120V)	
22			REF		–	–	TOP ASS'Y STORAGE SYSTEM					LM
23			—		1	—	0114-0008-20	BEZEL ASSY			BIOMATION KEY BD	LM
24			–		1	1	0114-0190-20	DATA BD.				
25			1		1	1	0114-0081	RETAINER CLIP PROBE TEST CONN				
26												
27			1		–	–	0114-0185-40	MPU PWB BD.				LM

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	G	REVISED PER ECO 2654	12-9-82	DGW	KV 12/16/82	
	H	REVISED PER ECO 2765A	2/11/83	MW	DGW	2-14-83
	J	REVISED PER ECO 3682	5/5/83	MW	DGW	5/6/83

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN J. PERGINS	2/4/81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

TOP ASSEMBLY

MODEL

biomation

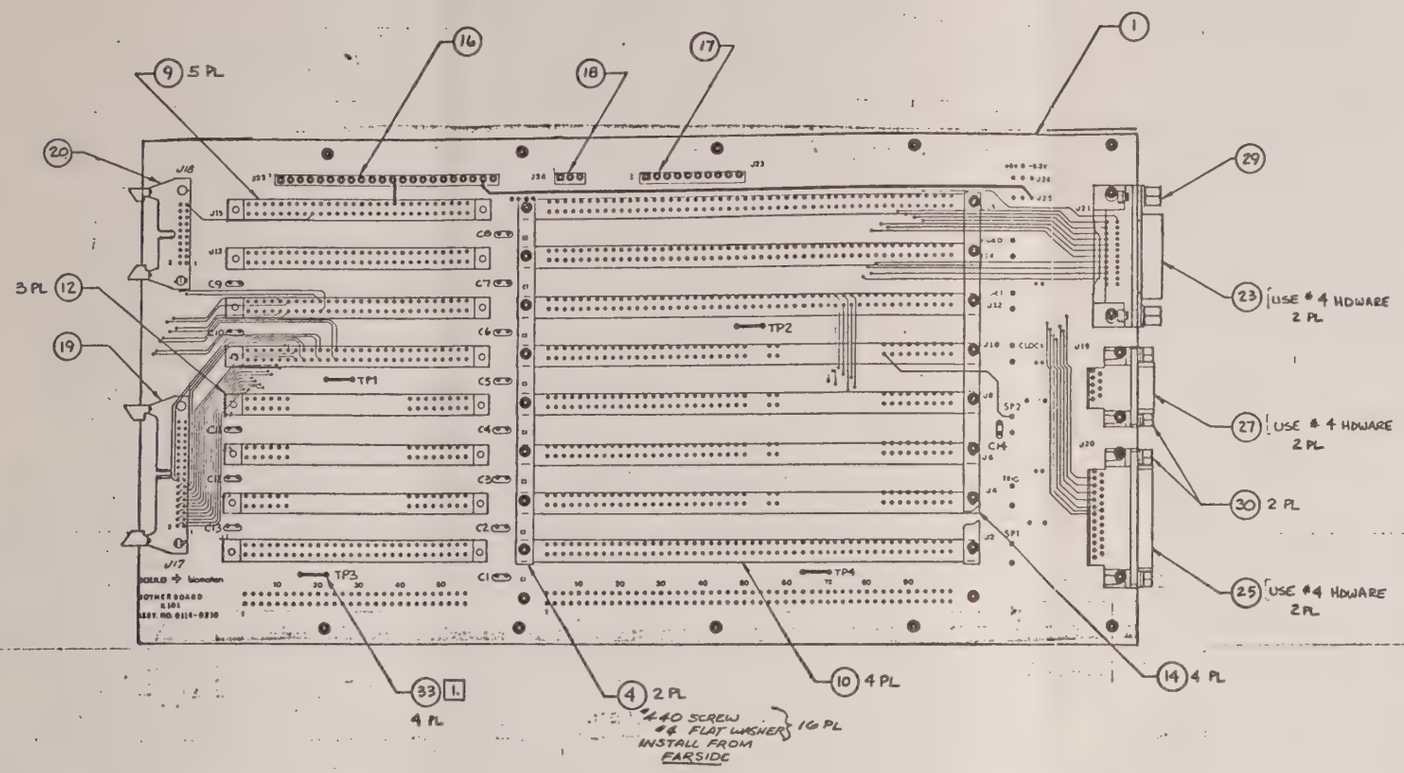
B 0114-0002 REV J

CODE K101 SHEET 2 OF 2

DWG NO. 0114-0210 SH 1 REV C

REVISIONS

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	B	-	PILOT REL PER ERN# 101	MS	RD	5/13/81
	C	1715	REVISED PER ECO	JL	[illegible]	8/6/81
	C	.	PROD REL PER ERN 207	[illegible]	RG	10/18/81



NOTES:

1. INSTALL GND BUSS WIRE; ITEM 33; ON FARSIDE AT TP1-4.

REFERENCE PRINT

MAR 0 8 1982

DASH NO	NUMBER	QTY
-10	0114-0009	1
	NEXT ASSEMBLY	

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .1 - 1 ANGLES ±1°; .1 - .620 ±.1°; .625 - .010

HOLE SIZE: 0.599 - .003; .500 .999 - .004; 3.000 1.999 - .005

ENG SERV R. Jepson DATE 1/7/82

DRAWN 4. Ku Bates DATE 2-6-81

CHECKED L. Lopez 1-22-81

PROJ ENG [illegible] 1-7-82

MANUFACTURING [illegible] 1/7/82

QUALITY ASSUR [illegible] 1/14/82

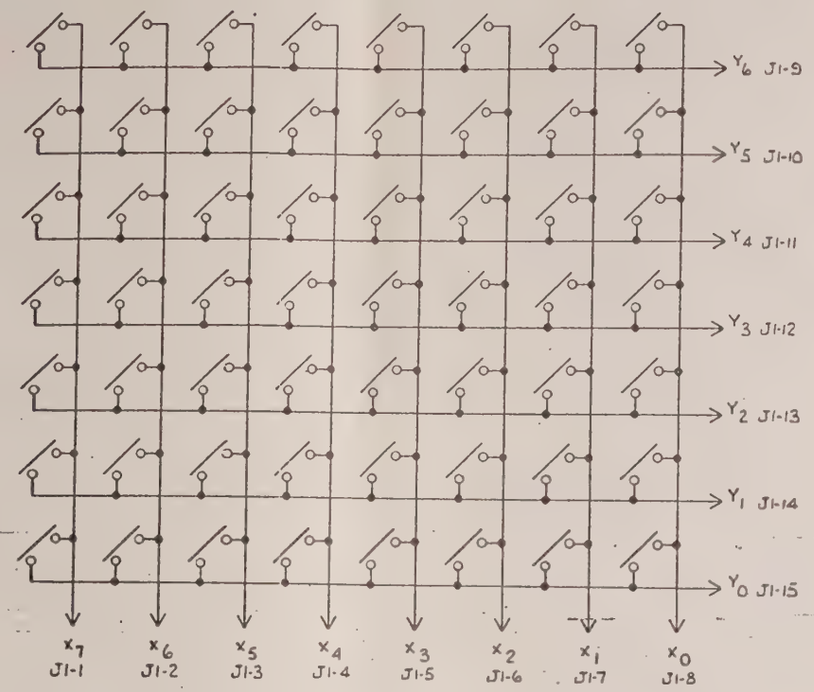
GOULD biomation

TITLE ASSEMBLY — MOTHER PWB, KIDID

SCALE | SIZE D | PART NUMBER 0114-0210 | REV C

CODE | SHEET 1 OF 1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PROTOTYPE			
	B		PILOT REL PER ENG ORI	[illegible]	RD	



MAR 0 8 1982

REFERENCE PRINT

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: .0 599 ± .003, .600 999 ± .004, 1.000 1.499 ± .005

DASH NO.	NUMBER	QTY
10	0114-200	
	NEXT ASSEMBLY	

ENG. SERV. | DATE

DRAWN S. RODELL | DATE 6-9-80

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: SCHEMATIC, K-101 KEYBOARD.

SCALE	SIZE	PART NUMBER	REV
NONE	C	0114-0201	B

CODE | SHEET 1 OF 1

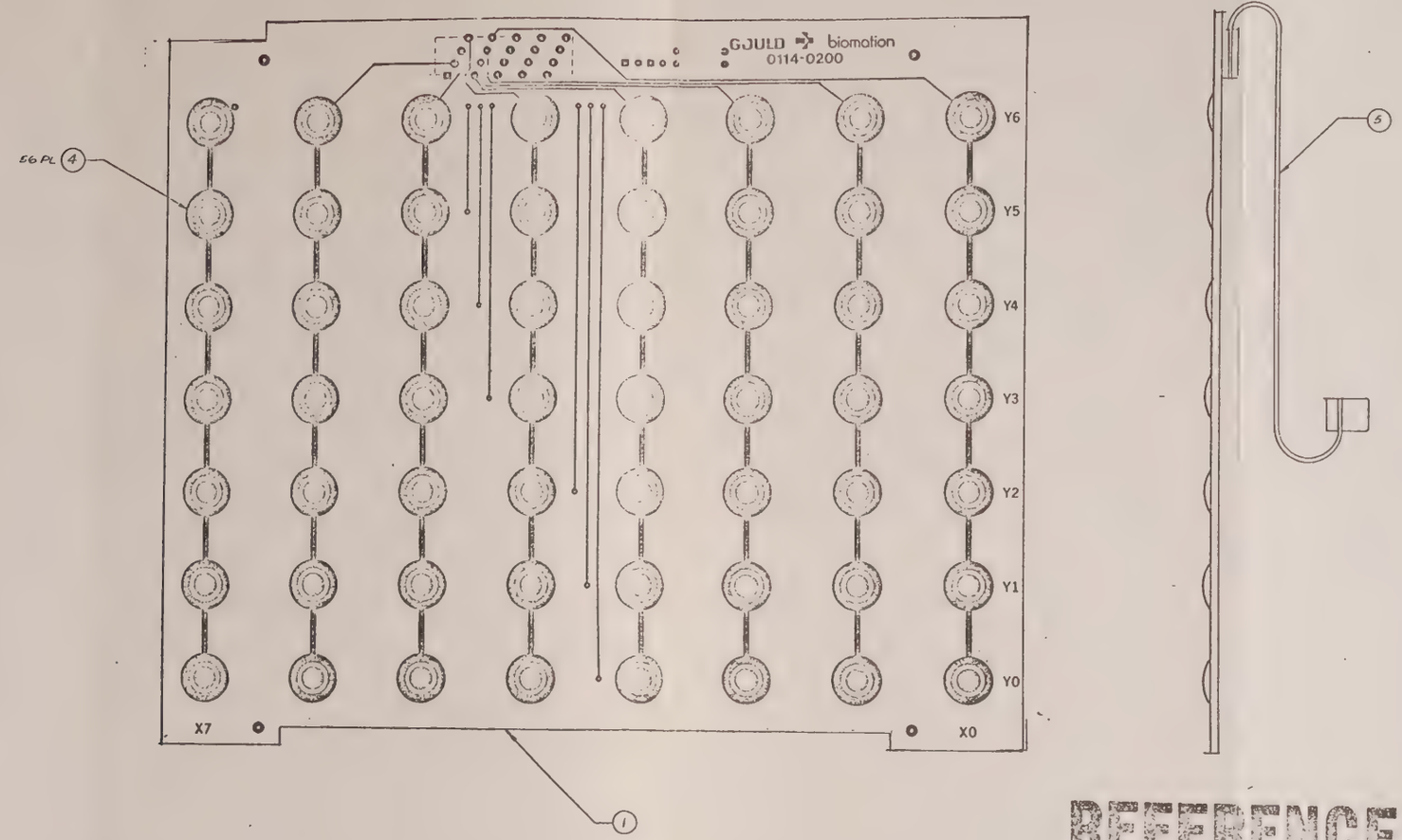
0114-0201

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4428

DWG NO.	SH	REV
0114-0200	1	B

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		[illegible]			
	B		PLOT REL ECN 0121	[illegible]	RD	



REFERENCE PRINT

MAR 0 5 1982

-50	40	30	20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. ELIMINATE ANGLES IN INCHES AND APPLY OVER AUGED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = ± ANGLES; XX = ± 0.20 ± 1°; XXX = ± .010

HOLE SIZE: 0.999 ± .001; 0.000 .999 ± .004; 1.000 1.999 ± .005

DRAWN: S. Rodell DATE: 1 11 80

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

ENG SERV. DATE

DASH NO.	NUMBER	QTY
10	0114-0200	1
	NEXT ASSEMBLY	

GOULD biomation

TITLE: ASSEMBLY, K101 SNAP-DOME KEYBOARD

SCALE	SIZE	PART NUMBER	REV
	D	0114-0200	B

CODE

SHEET 1 OF 1

Section 10

MEASUREMENT CONFIDENCE

10.1 INTRODUCTION

The K101-D has three self-diagnostic routines to give you confidence that it is operating correctly: Probe Test, Power Up Test, and Self-Test. Successful completion of these tests ensures that your K101-D is operating correctly and that the measurements it makes are valid. If there is a problem in the analyzer, these tests help you to quickly identify the problem.

a. **Probe Test:** The two clock and eight sample inputs of each probe can be quickly tested for correct detection of signal inputs by a built-in Probe Test socket which generates a known ring-counter pattern and clocking signals. Besides physically checking a probe's inputs, Probe Test can be used to explore and understand the operation of the K101-D itself.

b. **Power Up Test:** When the K101-D is turned on, a series of tests is automatically performed. The unit's ROM, RAM, power supply, CMOS RAM, USARTs, and keyboard are checked for correct operation.

c. **Self-Test:** For maximum confidence in the K101-D's operation, any of a series of detailed diagnostic tests may be performed. There are also troubleshooting test routines to help you debug any instrument error that may appear. Running Self-Test before calling the factory or shipping your instrument back for repair could save you a lot of time, trouble, and money.

10.2 **PROBE TEST**

The Probe Test discussion is intended to familiarize you with the operation of the K101-D, and verify that the equipment is working properly. The examples in this section are related to the A section inputs, and are summarized in Table 10-1. These examples are designed to be performed sequentially. The directions for creating a specific setup assume you will only need to make changes from the preceeding setup. Where appropriate, setup guides and illustrations of the desired setup screens are included to help you check that your setup is correct.

Turn the power on. Once the power up test sequence is complete, press **SHIFT, RECALL** to initialize all setups to their default values.

Note

If you make a mistake on a particular example you can start over by using the **SHIFT/RECALL** keys.

10.2.1 PROBE CONNECTION

Plug the SECTION A INPUTS CLK J, K, F . . . 8 probe cable into its front panel input and the pod into the Probe Test socket. The probe PC board key slot should be on your left and the pod labels facing up. To avoid getting noise on the other inputs, plug all the other probe cables into their appropriate front panel section inputs.

Table 10-1. Probe Test Exercises

Topic	Paragraph Number
Probe Connection	10.2.1
Polarity and Threshold:	
a. Fixed TTL	10.2.2.1
b. Fixed ECL	10.2.2.2
c. Stabilize pattern	10.2.2.3
d. Variable threshold	10.2.2.4
e. Negative polarity	10.2.2.5
Data Format:	
a. Delete inputs	10.2.3.1
b. Repeat inputs	10.2.3.2
c. Fixed format	10.2.3.3
Clock and Input:	
a. Sample internally	10.2.4.1
b. Sample -- single external clock	10.2.4.2
c. Sample -- multiple external clocks	10.2.4.3
d. Latch (Enable) -- combination	10.2.4.4
e. Demux -- single enable input	10.2.4.5
f. Demux -- combination enable inputs	10.2.4.6
Basic Trace Control:	
a. Fill MEM from anywhere	10.2.5.1
b. Record immediately after event	10.2.5.2
c. Record immediately before event	10.2.5.3
d. Record around an event	10.2.5.4
e. Record long after event	10.2.5.5
f. Record from here to there	10.2.5.6
g. Don´t record from here to there	10.2.5.7

Table 10-1. Probe Test Exercises (Cont'd)

Topic	Paragraph Number
h. Selectively record -- n times	10.2.5.8
i. Follow a path -- then record	10.2.5.9
j. Record -- then follow a path	10.2.5.10
k. Check for event 1 or 2	10.2.5.11
l. Take same path -- ignore events	10.2.5.12
m. Check timing between two events	10.2.5.13
n. Monitor for correct operation	10.2.5.14
Advanced Trace Control:	
a. Continuous check -- path and timing	10.2.6.1
b. Trace independent of execution path	10.2.6.2
c. End level break point	10.2.6.3
d. Segments, patterns, and total trace time	10.2.6.4
Record:	
a. Manual arm	10.2.7.1
b. Auto arm	10.2.7.2
c. Limiting the count	10.2.7.3
d. Stop if A ≠ B	10.2.7.4
e. Auto Stop if A = B	10.2.7.5
f. Auto Stop if A ≠ B within limits	10.2.7.6
g. Auto Stop if A = B within limits	10.2.7.7

10.2.2 POLARITY AND THRESHOLD

10.2.2.1 **Fixed TTL Threshold**

SET UP: None required. Uses the default values.

RECORD: Press [ARM] . This will arm (enable) recording of data.

REVIEW: Display timing data page 4. Press [TIMING] , [PAGE 4] four times to reach page 4.

You should see all zeros on all inputs (see Figure 10-1). This is because the Probe Test signals are generated by ECL logic, which typically uses a threshold of -1.30 volts (well below the default TTL value of +1.4 volts).

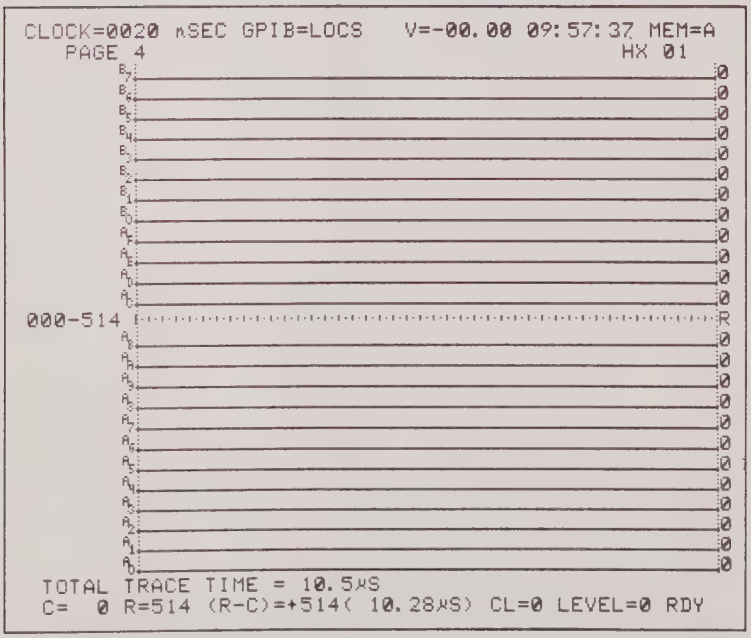


Figure 10-1. Resulting Probe Test Recording Using a TTL Threshold.

10.2.2.2 **Fixed ECL Threshold**

SET UP: Press [INPUT MODE]

Change the threshold for inputs AF through A8 to ECL by moving the blinking cursor to the AF-A8 line of the Input Mode display and change TTL to ECL.

Press [△] three times, [▷], [EBCDIC 9 ECL].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

A staircase pattern of pulses should be seen (Figure 10-2). This pattern may start anywhere on the screen because of the default trace control program, "Fill Memory with Samples from Anywhere in the Data Stream." Use the Control and Reference Cursors to measure the characteristic total trace time of 10.5 microseconds and pulse width of 0.9 microseconds.

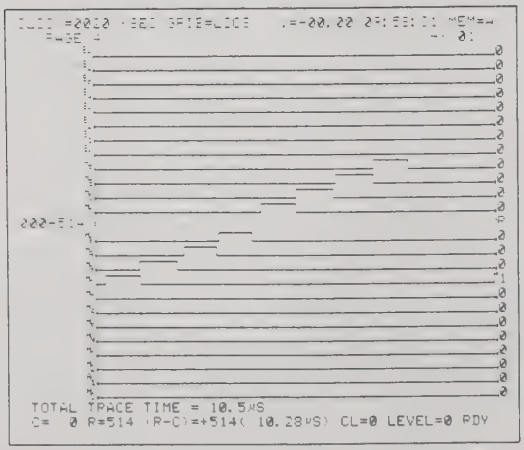


Figure 10-2. Typical Probe Test Recording Using an ECL Threshold.

10.2.2.3 **Stabilize Pattern**

SET UP: Obtain one full pattern that starts in the same location every time. Change the S word recognizer to S = xxxx xxxx 01xx.

Press [TRACE CONTROL] .

Move the cursor to S. Press [▽ SET] twice, [◁ SET] eight times, then [0 G], [1 H].

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

The display should look like Figure 10-3. The pattern will begin in the same location every recording through the use of the trace control command STOP IF DATA = S AND SAMPLE COUNT DELAY WHERE S = XXXX XXXX 01XX and DELAY = DEC 515 CLOCKS. Note that the total trace time is greater than 10.5 microseconds because of the extra time spent waiting for the specified trace control STOP condition to come true.

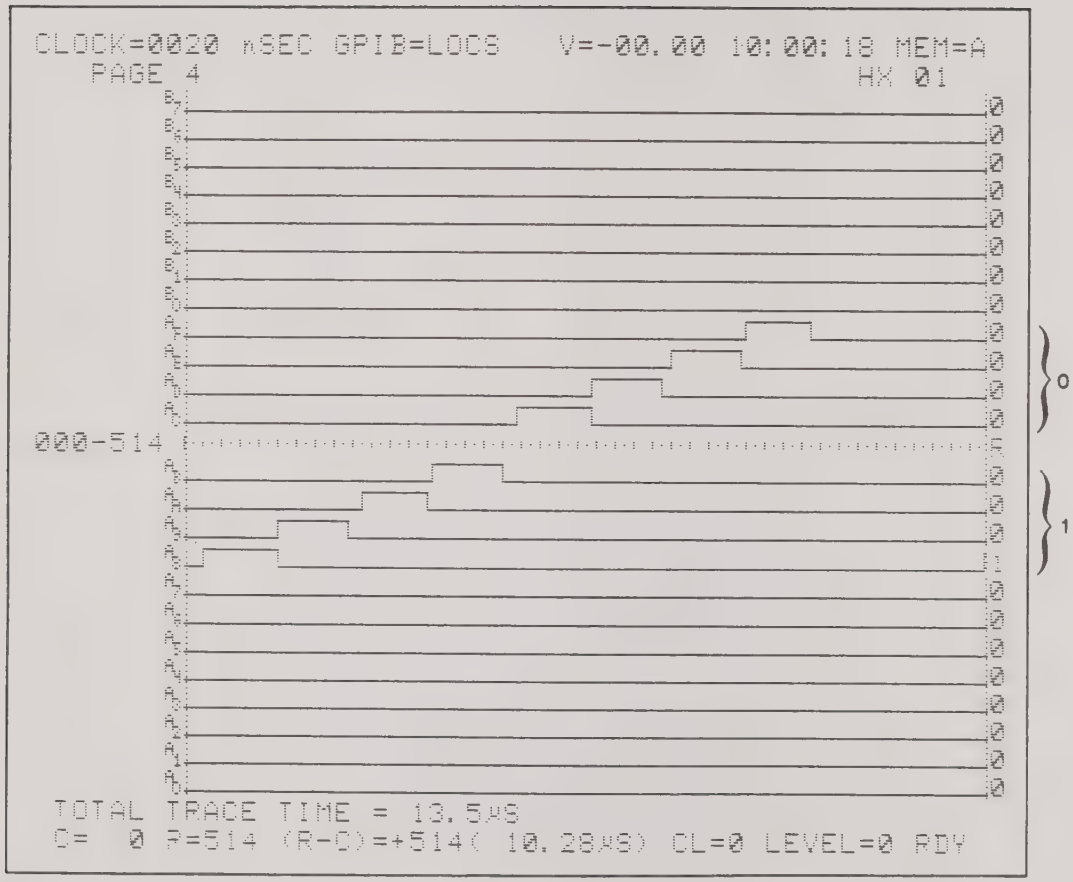


Figure 10-3. Fixed Location Pattern.

10.2.2.4 **Variable Threshold**

SET UP: Display the Input Mode screen.

Press [INPUT MODE] .

Change the threshold for inputs AF through A8 to VARA.

Press [△] three times, [▷] , [ASCII A] .

Change the value to something other than -1.30 volts such as -1.00 volts. Move the cursor to the numerical value and enter the digits (which are entered sequentially).

Press [▷] , [FALSE −] , [Hx3 1] , [Hx1 0] , [Hx1 0] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

Look for any difference in the pattern such as missing or shortened (<0.9 microsecond) pulses (check pulse width with the cursors), as shown in Figures 10-4 and 10-5, respectively. In Figure 10-4 note that the pulses that do not exceed the threshold will not be detected (threshold = 0.00 volts). In Figure 10-5 note that slow rise and fall times cause only that portion of the pulse that exceeds the threshold to be detected (threshold = +0.50 volts). If you see no irregularities, go back and change the threshold to some other value, record, and review again. Repeat this process until you perceive a noticeable change.

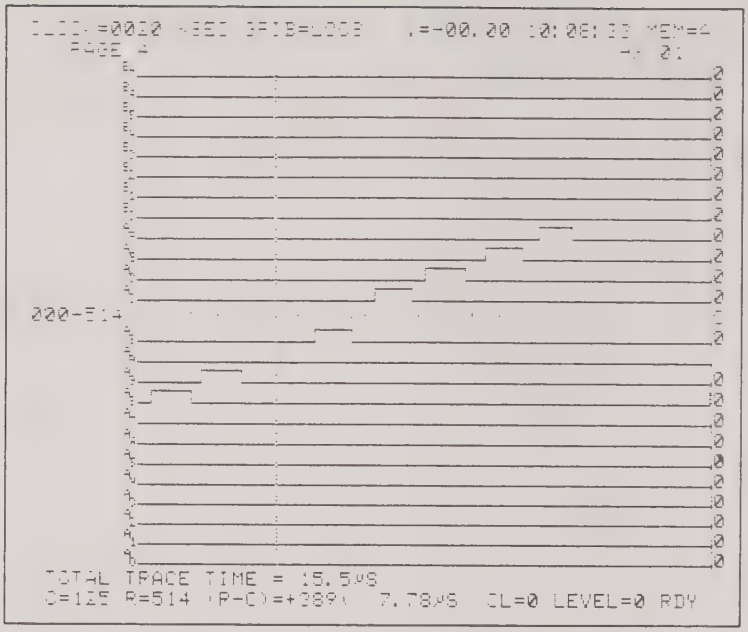


Figure 10-4. Pattern Changes with Threshold Changes.

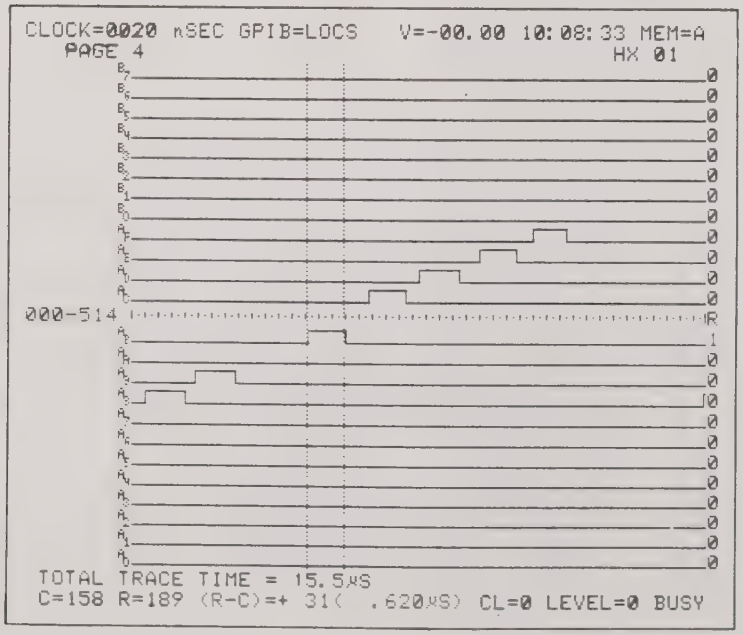


Figure 10-5. Effect of Rise and Fall Time.

10.2.2.5 **Negative Polarity**

SET UP: Display logic polarity screen. Press [LOGIC POLARITY] .

Change the polarity of inputs AF through A8 to negative.

Press [▽ SET] twice, [FALSE −] eight times.

Return threshold to ECL.

Press [INPUT MODE] , [△] three times, [▷] , [EBCDIC 9 ECL] P.

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

The trace level status will say LEVEL = 0 BUSY. (The displayed timing information is from the previous recording.) Trace control looks for 01 (hex) but never sees it because of the reversed polarity. Check what information is flowing from memory M to memory A.

Press [M→A] .

The display shows what information was flowing into memory and through trace control (see Figure 10-6). With negative polarity, positive-going pulses are a logical "0." The total trace time reading reflects the time between your pressing of the **ARM** and **M -> A** keys. Move the Control or Reference Cursor through the pulses (by holding down the appropriate cursor keys) while watching the binary cursor readout. Stop when the cursor is at the A8 input pulse. Note that for inputs AF through A8, a positive-going pulse is detected and represented as a logical "0," which is the definition of negative polarity.

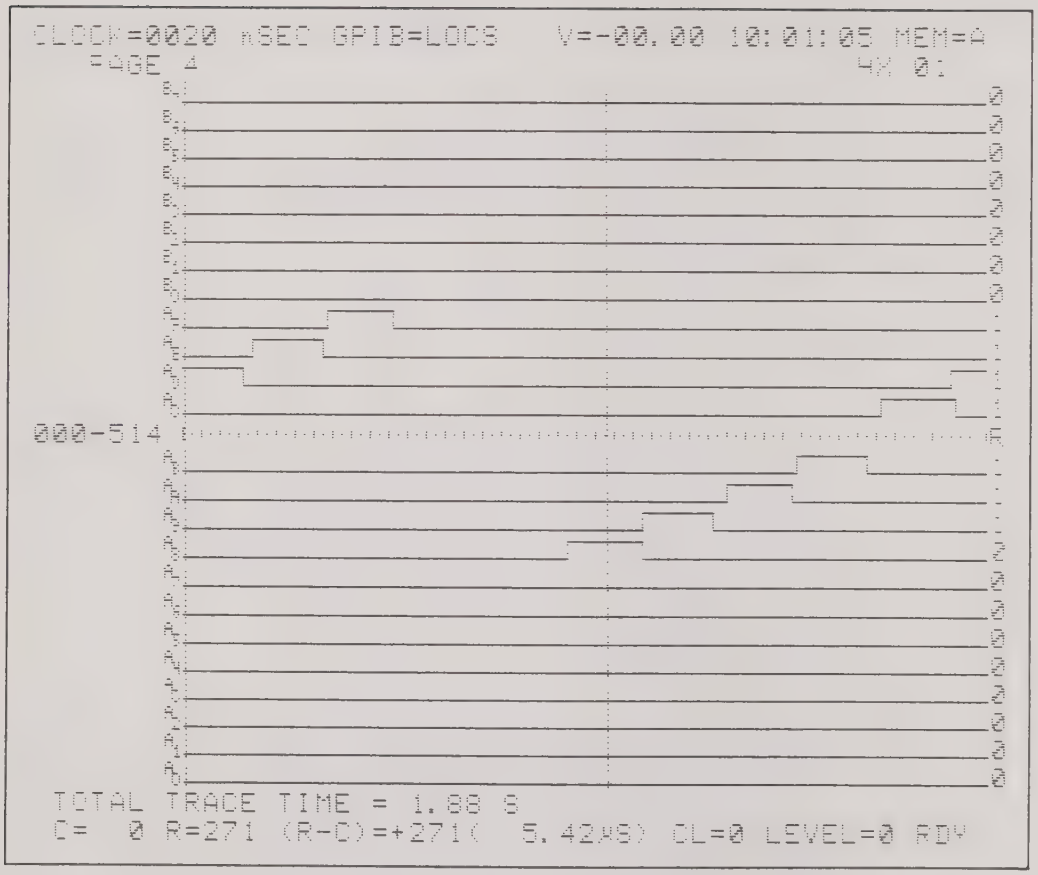


Figure 10-6. Information Flow.

10.2.3 DATA FORMAT

10.2.3.1 **Delete Inputs**

SET UP: See setup guide in Figure 10-7. Display Clock Select screen.

Press [CLOCK SELECT] .

Select the first option. Press [Hx3 1 H] .

Move to the master clock line. Press [▽ SET] twice.

Select second option and move cursor. Press [Hx6 2 ′] , [▷] twice.

Select first option. Press [Hx3 1 H] .

Select Logic Polarity display. Press [LOGIC POLARITY] .

Move cursor to A section. Press [▽ SET] twice.

Enter plus polarity for first eight inputs. Press [TRUE +] eight times.

The Clock Select and Trace Control displays should now look like Figures 10-8 and 10-9.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 31 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX:	H	H	H	H		H	H	H	H		H	H	H	H		
MSB																
16																
DATA 5																
4																
3	C_F	C_B	C_7	C_3		B_F	B_B	B_7	B_3		A_F	A_B	A_7	A_3		
2	C_E	C_A	C_6	C_2		B_E	B_A	B_6	B_2		A_E	A_A	A_6	A_2		
1	C_D	C_9	C_5	C_1		B_D	B_9	B_5	B_1		A_D	A_9	A_5	A_1		
LSB	C_C	C_8	C_4	C_0		B_C	B_8	B_4	B_0		A_C	A_8	A_4	A_0		

RADIX CHOICES. (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true simultaneously if nine conditions

Quick Key	Command Condition	
0	If DATA = D	
1	Always	
2	Never	
3	If DATA = D and Sample Count = Delay	
4	If DATA = D and Sample Count > Delay	
5	If DATA = D and Sample Count < Delay	
6	If DATA = D and Sample Count ≠ Delay	
7	If DATA = D and Sample Count ≥ Delay	
8	If DATA = D and Sample Count ≤ Delay	

(0 = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (QUICK KEY; 0-F) DELAY = DEC 515 (DEC/HEX; 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X X X X X X X X X X X

(2) JUMP TO 0 (0-F) NEVER
J = X X X X X X X X X X X X

(2) ADVANCE NEVER
A = X X X X X X X X X X X X

(1) TRACE ALWAYS
T = X X X X X X X X X X X X

COMMENTS

LEVEL ___ (0-F) DELAY = _____ (DEC/HEX; 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(....) STOP _____
S = _____

(.....) JUMP TO ___ (0-F) _____
J = _____

(.....) ADVANCE _____
A = _____

(....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (0-F) DELAY = _____ (DEC/HEX; 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (0-F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (0-F) DELAY = _____ (DEC/HEX; 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (0-F) _____
J = _____

(...) ADVANCE _____
A = _____

(...) TRACE _____
T = _____

COMMENTS

Figure 10-7. Setup (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 3.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____ ● _____ ● AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____ ● _____ ● _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = (_____ ● _____ ● _____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF AO sequence
1	OCTAL Fixed octal format & CF AO sequence
2	BINARY Fixed binary format & CF AO sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF AO SEQN Any radix fixed CF AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE ↓ ACTIVE FALLING EDGE
2	NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	NOT USED

QUICK KEY	MODE & DESCRIPTIONS
	INTERNAL [illegible]
	EXTERNAL SINGLE PHASED [illegible]
	EXTERNAL MULTI-PHASED [illegible]
	MIXED SINGLE PHASED [illegible]
4	MIXED MULTI PHASED [illegible]
	INTERNAL EXTENDED [illegible]

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
	AUTO STOP IF A B
	AUTO STOP IF A B
4	AUTO STOP IF A B WITHIN LIMITS
5	AUTO STOP IF A B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
	NEGATIVE

DWS24-12.5183

Figure 10-7. Setup (Sheet 2 of 2).

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 12:59:51 MEM=M
                    CLOCK SELECT

                 MODE = EXTERNAL SINGLE-PHASED

    INT. CLOCK PERIOD = 0020 NANOSECONDS

 MASTER CLOCK = (____•____•AJ↓)+(____+____+____)

 SAMPLE CLOCK

   C = SAME AS MASTER

   B = SAME AS MASTER

   A = SAME AS MASTER

 ENABLE  -- (used only in Latch & Demux)

   C = EXT (CR↑•____•____)+(____+____+____)

   B = EXT (CR↑•____•____)+(____+____+____)

   A = EXT (CR↑•____•____)+(____+____+____)

 MASTER CLOCK = 1.00µS

 C=     R=     (R-C)=     (          ) CL=  LEVEL=0 RDY
```

Figure 10-8. Clock Select for Delete Example.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 14:01:21 MEM=M

                    TRACE CONTROL

     HHHH HHHH HHHH
MSB
 6
 5
 4
 3   ____ ____ ____
 2   ____ ____ ____
 1   ____ ____ ____
LSB  ____ ____ ____
-----------------------------------------------------
LEVEL 0 DELAY = DEC 00515 CLOCKS          END LEVEL    F

  STOP IF DATA=0 AND SAMPLE COUNT >DELAY
 B= XXXX XXXX 01XX

  JUMP TO 0 NEVER
 J= XXXX XXXX XXXX

  ADVANCE NEVER
 A= XXXX XXXX XXXX

  TRACE ALWAYS
 T= XXXX XXXX XXXX

 C=     R=     (R-C)=     (          ) CL=  LEVEL=0 RDY
```

Figure 10-9. Trace Control for Delete Example.

RECORD: Press [ARM] .

REVIEW: Display the synchronously recorded pattern.

Press [TIMING] , [Hx12 3] .

Display the data. Press [DATA] .

The display should look like Figure 10-10 which is full data display for inputs AF through A8, probe test recording. . (If any columns are filled with Fs, it means that the probe is not plugged into the front panel.)

Display the corresponding graph (see Figure 10-11) which is based on the original data format. Since the hex value of each 12-character word is close to zero, only a baseline can be seen.

```
CLOCK=EXT - SGL GPIB=LOCS   V=-00.00 10:16:24 MEM=A

     HHHH HHHH HHHH              HHHH HHHH HHHH
000C0000 0000 0000          024 0000 0000 0800
001 0000 0000 0100          025 0000 0000 1000
002 0000 0000 0200          026 0000 0000 2000
003 0000 0000 0400          027 0000 0000 4000
004 0000 0000 0800          028 0000 0000 8000
005 0000 0000 1000          029 0000 0000 0000
006 0000 0000 2000          030 0000 0000 0000
007 0000 0000 4000          031 0000 0000 0100
008 0000 0000 8000          032 0000 0000 0200
009 0000 0000 0000          033 0000 0000 0400
010 0000 0000 0000          034 0000 0000 0800
011 0000 0000 0100          035 0000 0000 1000
012 0000 0000 0200          036 0000 0000 2000
013 0000 0000 0400          037 0000 0000 4000
014 0000 0000 0800          038 0000 0000 8000
015 0000 0000 1000          039 0000 0000 0000
016 0000 0000 2000          040 0000 0000 0000
017 0000 0000 4000          041 0000 0000 0100
018 0000 0000 8000          042 0000 0000 0200
019 0000 0000 0000          043 0000 0000 0400
020 0000 0000 0000          044 0000 0000 0800
021 0000 0000 0100          045 0000 0000 1000
022 0000 0000 0200          046 0000 0000 2000
023 0000 0000 0400          047 0000 0000 4000

 C=  0 R=514 (R-C)=+514(        ) CL=0 LEVEL=0 RDY
```

Figure 10-10. Data Display, Probe Inputs AF through A8.

```
CLOCK=EXT - SGL GPIB=LOCS   V=-00.00 14:06:46 MEM=A

 HOR.
SCALE
  = X01

   48
CHANNELS
SELECTED

GRAPH

000-514

  TIME

        C DATA=0000 0000 0000 R DATA=0000 0000 0800
 C=  0 R=514 (R-C)=+514(        ) CL=0 LEVEL=0 RDY
```

Figure 10-11. Graph of Data of Figure 10-10.

Press [GRAPH] .

Display the data format. Press [DATA FORMAT] .

Delete all inputs except AF through A8.

Press [◁] SET , [DELETE] ten times, [▷] twice, [DELETE] twice.

Check that the word recognizer formats have correspondingly changed.

Press [TRACE CONTROL] (see Figure 10-12). Note that changing the data format also changes the trace control's word recognizer format.

Press [DATA] (see Figure 10-13).

Check the new graph format.

Press [GRAPH] (see Figure 10-14).

Note the number of channels selected and that changing the data format changes the input channels that are graphed.

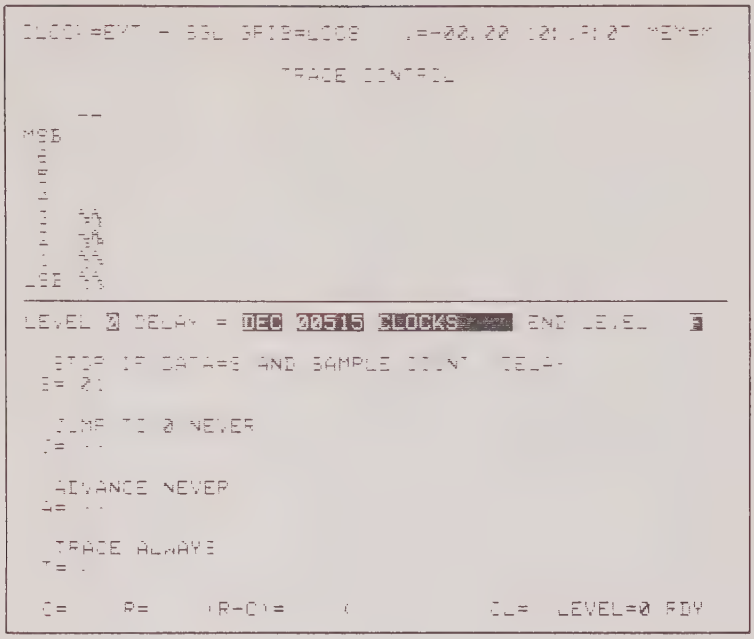


Figure 10-12. Data Format/Word Recognizer Changes.

CLOCK=EXT - SGL GPIB=LOCS V=-00.00 10:16:24 MEM=A

	HH		HH		HH		HH		HH		HH
000	C00	024	08	048	80	072	02	096	20	120	00
001	01	025	10	049	00	073	04	097	40	121	01
002	02	026	20	050	00	074	08	098	80	122	02
003	04	027	40	051	01	075	10	099	00	123	04
004	08	028	80	052	02	076	20	100	00	124	08
005	10	029	00	053	04	077	40	101	01	125	10
006	20	030	00	054	08	078	80	102	02	126	20
007	40	031	01	055	10	079	00	103	04	127	40
008	80	032	02	056	20	080	00	104	08	128	80
009	00	033	04	057	40	081	01	105	10	129	00
010	00	034	08	058	80	082	02	106	20	130	00
011	01	035	10	059	00	083	04	107	40	131	01
012	02	036	20	060	00	084	08	108	80	132	02
013	04	037	40	061	01	085	10	109	00	133	04
014	08	038	80	062	02	086	20	110	00	134	08
015	10	039	00	063	04	087	40	111	01	135	10
016	20	040	00	064	08	088	80	112	02	136	20
017	40	041	01	065	10	089	00	113	04	137	40
018	80	042	02	066	20	090	00	114	08	138	80
019	00	043	04	067	40	091	01	115	10	139	00
020	00	044	08	068	80	092	02	116	20	140	00
021	01	045	10	069	00	093	04	117	40	141	01
022	02	046	20	070	00	094	08	118	80	142	02
023	04	047	40	071	01	095	10	119	00	143	04

C= 0 R=514 (R-C)=+514( ) CL=0 LEVEL=0 RDY

Figure 10-13. New Data Display for Figure 10-12 Data Format.

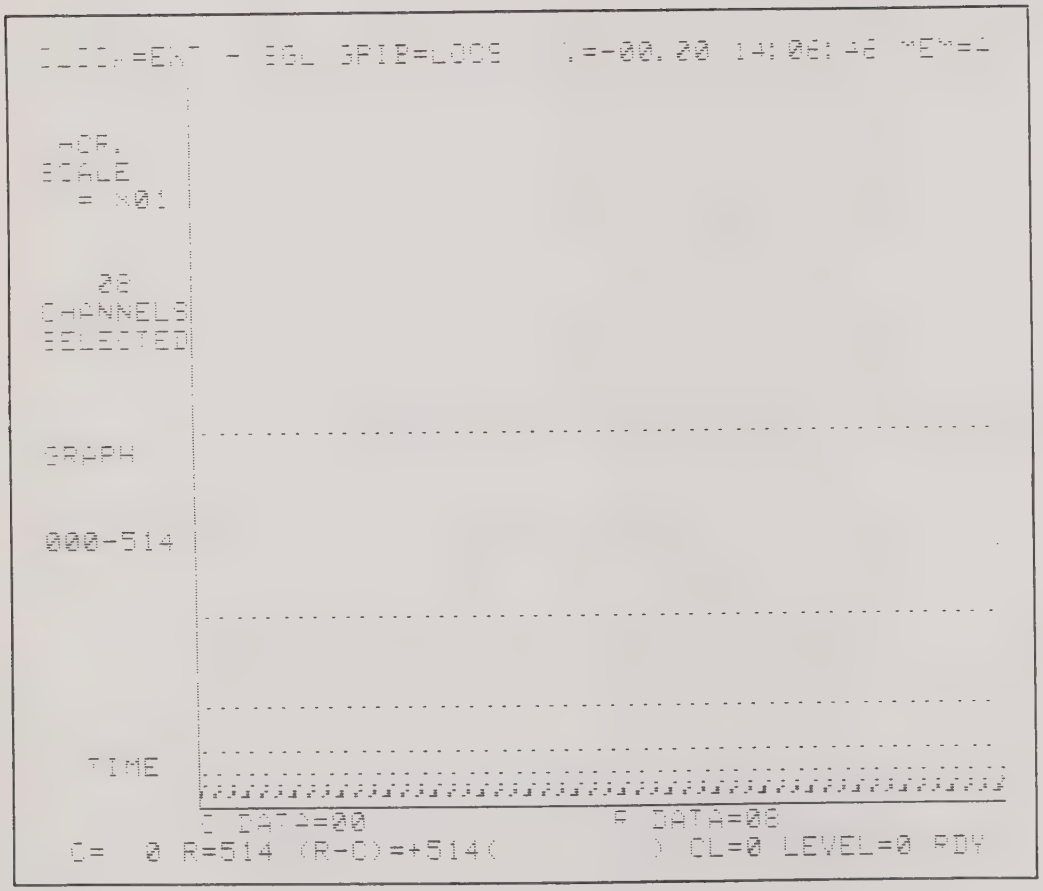


Figure 10-14. Change of Input Channel Graphed.

10.2.3.2 **Repeat Inputs**

REVIEW: Change the data format to look at inputs AF through A8 in binary as well as hex by the following procedure:

Press [DATA FORMAT], [▽ SET], [▷] twice, [INSERT], [▷],

[BINARY B R], [ASCII A Q], [DEMUX F V HEX], [BINARY B R], [ASCII A Q], [LATCH E U OCTAL],

[BINARY B R], [ASCII A Q], [GLITCH D T DECIMAL], [BINARY B R], [ASCII A Q], [SAMPLE C S],

[BINARY B R], [ASCII A Q], [BINARY B R], [BINARY B R], [ASCII A Q], [ASCII A Q],

[BINARY B R], [ASCII A Q], [EBCDIC 9 P ECL], [BINARY B R], [ASCII A Q], [PAGE↑ 8 O TTL].

The new data format should now look like Figure 10-15. The same inputs may be viewed in more than one radix. In Figure 10-15, AF through A8 are displayed in both hex and binary.

Display the reformatted information.

Press [DATA]. See Figure 10-16 which shows the corresponding data display for the data format of Figure 10-15. The binary representation of each hex word is clearly seen.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 10:25:08 MEM=M

                    DATA FORMAT
        RADIX=            GROUP=      INPUT=
                 MIXED  USER SEQN

    HH BBBBBBBB
MSB
 6
 5
 4
 3  %%
 2  %%
 1  %%
LSB %% %%%%%%%%
-------------------------------------------------------
                    SEARCH WORD
    HH BBBBBBBB
    XX XXXXXXXX
MSB
 6
 5
 4
 3  XX
 2  XX
 1  XX
LSB XX XXXXXXXX

 C=    R=    (R-C)=    (          ) CL=  LEVEL=0 RDY
```

Figure 10-15. AF through A8 Displayed In Both Hex and Binary.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 10:16:24 MEM=A

    HH BBBBBBBB       HH BBBBBBBB       HH BBBBBBBB
000C00 00000000  024 08 00001000  048 80 10000000
001 01 00000001  025 10 00010000  049 00 00000000
002 02 00000010  026 20 00100000  050 00 00000000
003 04 00000100  027 40 01000000  051 01 00000001
004 08 00001000  028 80 10000000  052 02 00000010
005 10 00010000  029 00 00000000  053 04 00000100
006 20 00100000  030 00 00000000  054 08 00001000
007 40 01000000  031 01 00000001  055 10 00010000
008 80 10000000  032 02 00000010  056 20 00100000
009 00 00000000  033 04 00000100  057 40 01000000
010 00 00000000  034 08 00001000  058 80 10000000
011 01 00000001  035 10 00010000  059 00 00000000
012 02 00000010  036 20 00100000  060 00 00000000
013 04 00000100  037 40 01000000  061 01 00000001
014 08 00001000  038 80 10000000  062 02 00000010
015 10 00010000  039 00 00000000  063 04 00000100
016 20 00100000  040 00 00000000  064 08 00001000
017 40 01000000  041 01 00000001  065 10 00010000
018 80 10000000  042 02 00000010  066 20 00100000
019 00 00000000  043 04 00000100  067 40 01000000
020 00 00000000  044 08 00001000  068 80 10000000
021 01 00000001  045 10 00010000  069 00 00000000
022 02 00000010  046 20 00100000  070 00 00000000
023 04 00000100  047 40 01000000  071 01 00000001

 C=  0 R=514  R-C =+514(          ) CL=0 LEVEL=0 RDY
```

Figure 10-16. Data Display for Figure 10-15.

10.2.3.3 **Fixed Format**

REVIEW: Display the fixed binary format.

Press [DATA FORMAT], [Hx6 2].

The display data should now look like Figure 10-17 which shows the same information viewed in a fixed binary format of all inputs CF through A0. Verify that only the first 14 binary columns (which are all zeros) are graphed.

Press [GRAPH] (see Figure 10-18) note that the graph of the first 14 columns of the fixed binary data display yields all zeros.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 10:16:24 MEM=A

    BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
000C00000000000000000000000000000000000000000000000000
001 00000000000000000000000000000000000000000100000000
002 00000000000000000000000000000000000000001000000000
003 00000000000000000000000000000000000000010000000000
004 00000000000000000000000000000000000000100000000000
005 00000000000000000000000000000000000001000000000000
006 00000000000000000000000000000000000010000000000000
007 00000000000000000000000000000000000100000000000000
008 00000000000000000000000000000000001000000000000000
009 00000000000000000000000000000000000000000000000000
010 00000000000000000000000000000000000000000000000000
011 00000000000000000000000000000000000000000100000000
012 00000000000000000000000000000000000000001000000000
013 00000000000000000000000000000000000000010000000000
014 00000000000000000000000000000000000000100000000000
015 00000000000000000000000000000000000001000000000000
016 00000000000000000000000000000000000010000000000000
017 00000000000000000000000000000000000100000000000000
018 00000000000000000000000000000000001000000000000000
019 00000000000000000000000000000000000000000000000000
020 00000000000000000000000000000000000000000000000000
021 00000000000000000000000000000000000000000100000000
022 00000000000000000000000000000000000000001000000000
023 00000000000000000000000000000000000000010000000000

 C=  0 R=514 (R-C)=+514(          ) CL=0 LEVEL=0 RDY
```

Figure 10-17. Fixed Binary Format, All Inputs CF through A0.

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 11:13:28 MEM=A

 HOR.
SCALE
  = X12

   14
CHANNELS
SELECTED

GRAPH

000-042

  TIME

          C DATA=0000              R DATA=0000
 C=  0 R=514 (R-C)=+514(          ) CL=0 LEVEL=0 RDY
```

Figure 10-18. Graph First 14 Columns as Fixed Binary Data.

10.2.4 CLOCK AND INPUT

The Probe Test pattern generator produces two clock signals in addition to its eight data signals. The first clock signal is an external J clock input for the high order (F through 8) probe of each section, or an R enable input for the low order (7 through 0) probe of each section. The second clock signal is an external K clock input for the high order probe of each section, or an S enable input for the low order probe of each section. The actual time relationship between the clock and data signals is shown in Figure 10-19.

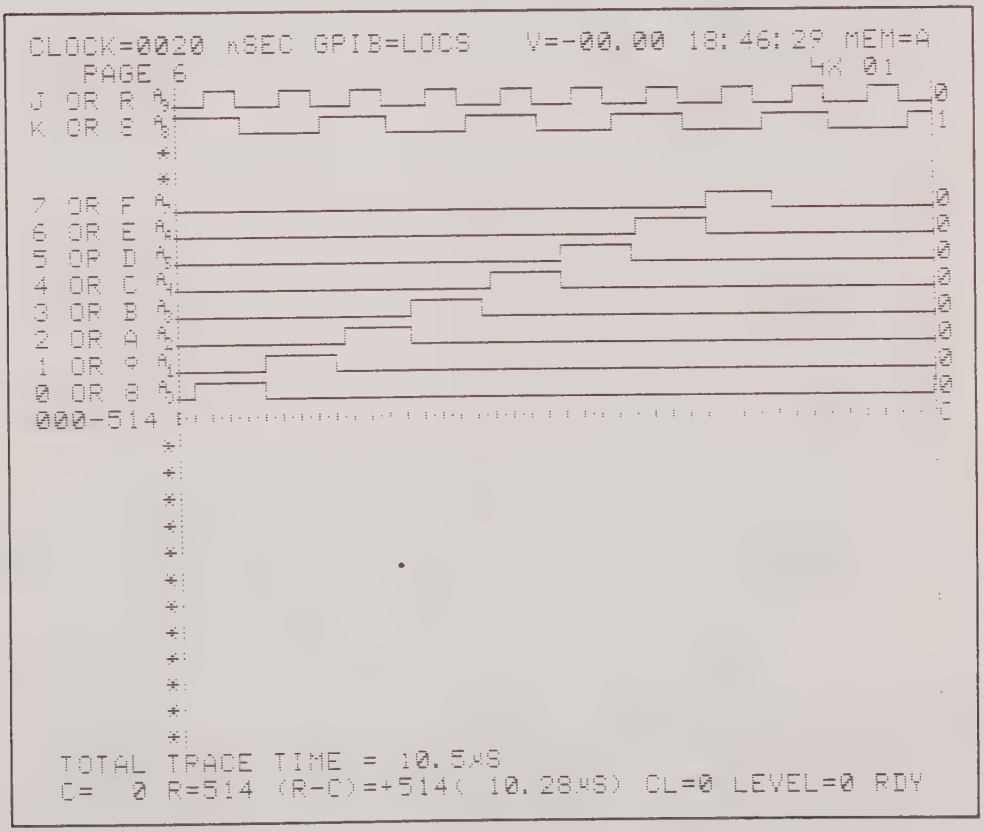


Figure 10-19. Time Relationship of Clock and Data Signals.

10.2.4.1 Sample Internally

SET UP: Take several samples of each pulse. See setup guide in Figure 10-20.

Modify Clock Select screen. Press [CLOCK SELECT], [Hx1 0 G], [▽ SET], [Hx3 1 H], [Hx1 0 G], [Hx1 0 G].

Display data format. Press [DATA FORMAT], [Hx12 3 J], [▽ SET], [▷] twice, [SHIFT], [DELETE].

The Clock Select and Data Format displays should look like Figures 10-21 and 10-22.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
6	
D N 5	
A P 4	
T J 3	AcAB
A T 2	AEAA
S 1	ADA9
LSB	AcA8

RADIX CHOICES (B) BINARY (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
A high priority commands in each level can override any lower priority conditions

Quick Key	Command Condition
3	DATA = S
	Always
	Never
4	DATA = S and Sample Count = Delay
3	DATA = S and Sample Count = Delay
2	DATA = S and Sample Count = Delay
1	DATA = S and Sample Count = Delay
0	DATA = S and Sample Count = Delay

(D, S, J, A, or T) which are assigned by command type.

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (O F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (O F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (O F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (O F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

Figure 10-20. Set Up Internal Sampling (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (0) MODE = INTERNAL

CJ BJ AJ CK BK AK

■ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = 100

MASTER = ■ INTERNAL ☐ EXT (_____●_____●_____) + (_____+_____+_____)

SECTION C = INT ■ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ■ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ■ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - A0 sequence
1	OCTAL Fixed octal format & CF - A0 sequence
2	BINARY Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF - A0 SEQN Any radix fixed CF - A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	CLOCK CHOICES
0	↑ ACTIVE RISING EDGE ↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	CLOCK CHOICES
0	↑ POSITIVE TRUE ↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A + Section B + Section C + internal clock period
	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A + Section B + Section C + Master external
2	EXTERNAL MULT PHASED Each section can be sampled at own external rate or Master external rate Section A Section B Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external Each section can be sampled at the Master external rate internal clock period or 10ns Section A Section B and or Section C + Master external or internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external Each section can be sampled at own external rate the Master external rate internal clock period or 10ns Section A Section B and or Section C Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns Section A Section B and or Section C + internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
	NEGATIVE

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Figure 10-20. Set Up Internal Sampling (Sheet 2 of 2).

```
CLOCK=0100 nSEC GPIB=LOCS    V=-00.00 14:58:02 MEM=M
                    CLOCK SELECT

                  MODE = INTERNAL

    INT. CLOCK PERIOD = 0100 NANOSECONDS

 MASTER CLOCK = INTERNAL

 SAMPLE CLOCK

   C = INT 0100  NANOSECONDS

   B = INT 0100  NANOSECONDS

   A = INT 0100  NANOSECONDS

 ENABLE  -- (used only in Latch & Demux.)

   C = EXT ( CR↑•____•____)+(____+____+____)

   B = EXT ( CR↑•____•____)+(____+____+____)

   A = EXT ( CR↑•____•____)+(____+____+____)

 C=     R=     (R-C)=     (          ) CL=  LEVEL=0 RDY
```

Figure 10-21. Clock Select for Sample Internally.

```
CLOCK=0100 nSEC GPIB=LOCS    V=-00.00 14:59:51 MEM=M

                    DATA FORMAT
          RADIX=          GROUP=      INPUT=
                 MIXED  USER SEQN

     HH
MSB
 6
 5
 4
 3  AEAB
 2  AEAB
 1  AEAB
LSB AEAB
-------------------------------------------------------
                    SEARCH WORD
     HH
     XX
MSB
 6
 5
 4
 3  XX
 2  XX
 1  XX
LSB XX

 C=     R=     (R-C)=     (          ) CL=  LEVEL=0 RDY
```

Figure 10-22. Data Format for Sample Internally.

RECORD: Press [ARM] .

REVIEW: Display the timing screen. Press [TIMING] , [Hx1 0 G] , [PAGE 4 K] to page 4.

The display should look like Figure 10-23. Each pulse is 0.9 microseconds (nine samples) wide ±100 nS (one sample). Confirm this with the cursors.

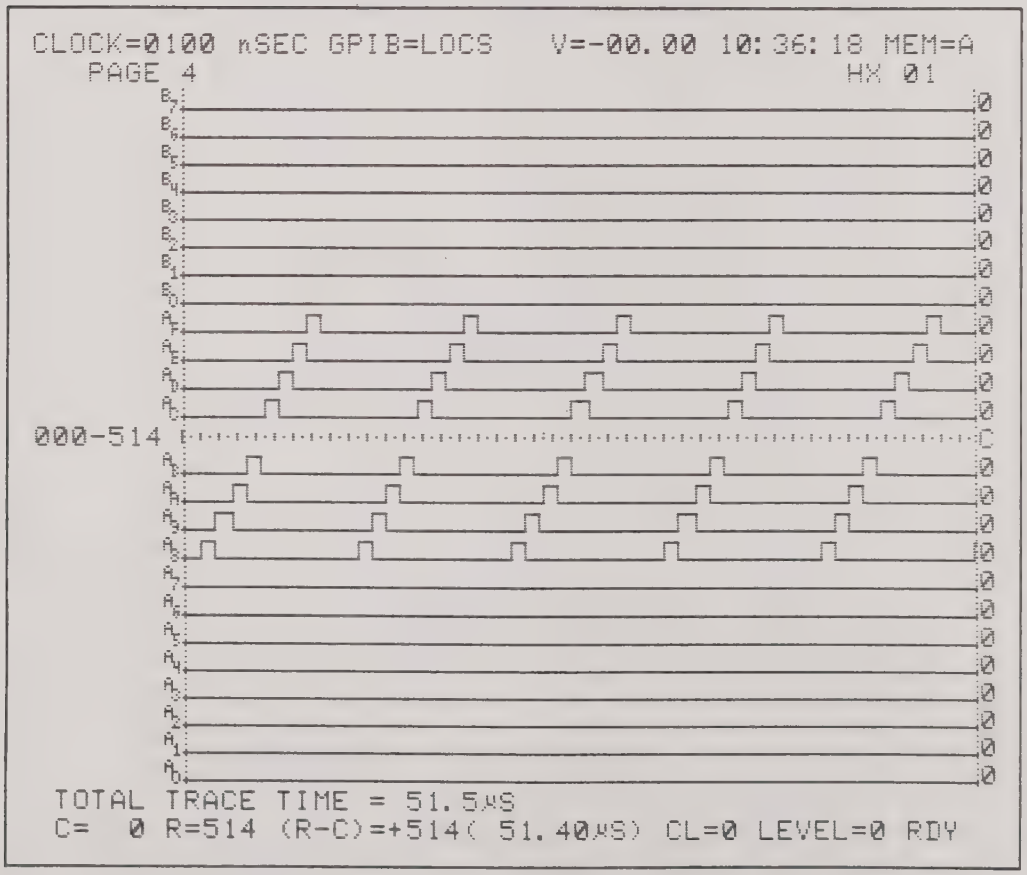

Figure 10-23. Pattern Asynchronously Sampled Every 100 ns.

10.2.4.2 **Sample On A Single External Clock (AJ↑ or AJ↓)**

SET UP: The active sampling edge of AJ can be specified as either rising or falling. Since both edges of each AJ pulse occur well within each input pulse (Figure 24a and 24b), it doesn't matter which edge is selected; the resulting recordings will be identical. In each case, one sample of each pulse will be taken. See the setup guide in Figure 10-25.

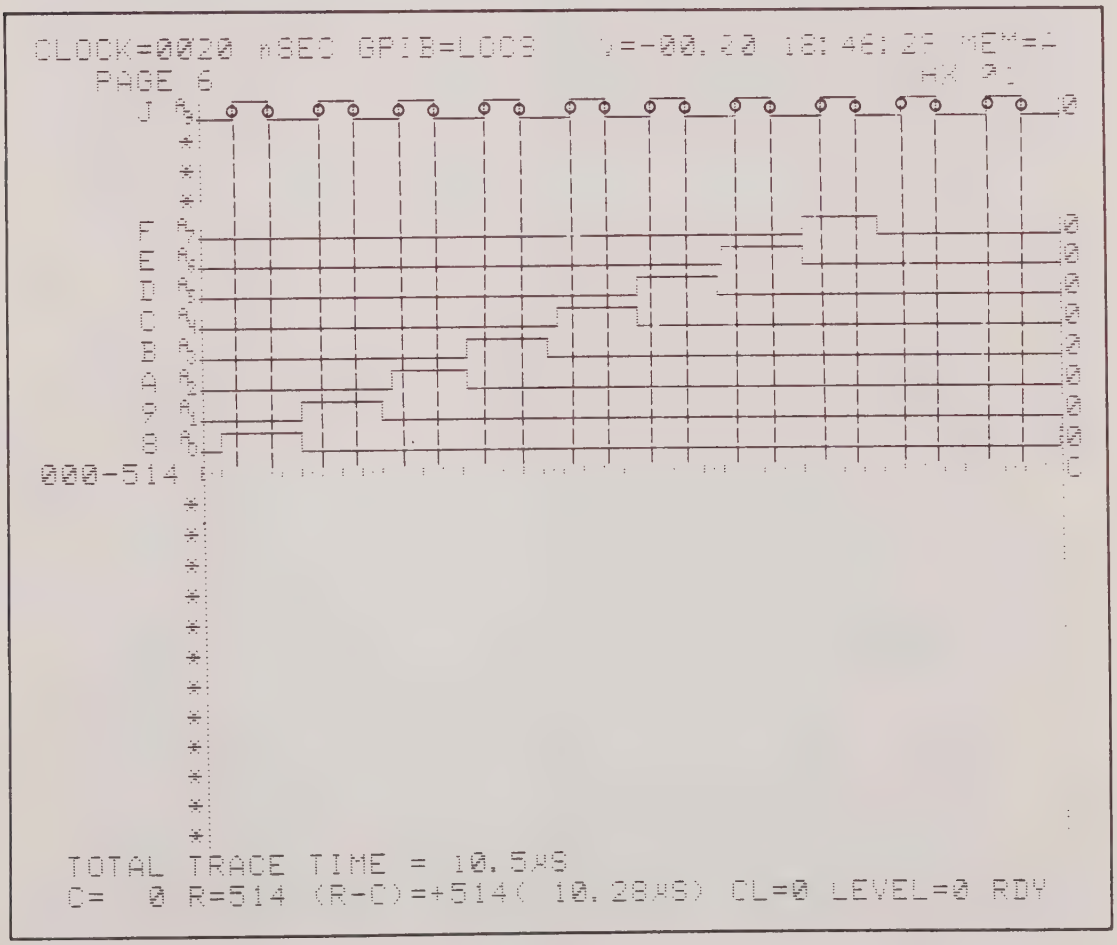

Figure 10-24. Sample Clock = AJ↑.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #4.2 OF ___ DATE _____

QUICK KEY (see back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AE A8
A T 2 AE A8
S 1 AD A1
LSB AC A0

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions.

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA ≠ D and Sample Count = Delay
5	If DATA = D and Sample Count > Delay
6	If DATA ≠ D and Sample Count > Delay
7	If DATA = D and Sample Count < Delay
8	If DATA ≠ D and Sample Count < Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

QUICK KEY — LEVEL 0 (0-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

QUICK KEY — LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (0-F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

QUICK KEY — LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (0-F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

QUICK KEY — LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____

(.....) JUMP TO ___ (0-F) _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

COMMENTS

Figure 10-25. Setup Sample, Single External Clock (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.2a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (.1.) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↑) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF AO sequence
1	OCTAL Fixed octal format & CF AO sequence
2	BINARY Fixed binary format & CF AO sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF AO SEQN Any radix, fixed CF AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	- - - - NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
3	↑ POSITIVE TRUE
4	↓ NEGATIVE TRUE
5	- NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate. Section A = Section B = Section C = internal clock period.
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate. Section A = Section B = Section C = Master external.
2	EXTERNAL MULTI PHASED Each section can be sampled at an integral rate of Master external rate. Section A, Section B, Section C & Master can be different external rate expressions.
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate or internal clock period. Section A, Section B and or Section C = Master external or internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at each external rate, the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C = Master external or internal or 10ns.
5	INTERNAL EXTENDED All sections can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C = internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (.0.) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A < B
3	AUTO STOP IF A > B
4	AUTO STOP IF A < B WITHIN LIMITS
5	AUTO STOP IF A > B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

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Figure 10-25. Setup Sample, Single External Clock (Sheet 2 of 2).

Change Clock Select display to show the following:

MASTER CLOCK = (__·__·__ AJ↑) + (__+__+__)

Press [CLOCK SELECT] , [Hx3 1 H] , [▽ SET] twice, [▷] twice, [Hx1 0 G] .

The Clock Select display should look like Figure 10-26 which shows clock select for setup AJ↑. Each subsequent push of [CLOCK SELECT] measures the external master sample clock frequency. . Note that if you press **CLOCK SELECT** a second time after setting it up, a reading of the external master clock frequency is displayed. Each press of **CLOCK SELECT** takes another frequency measurement.

RECORD: Press [ARM] .

REVIEW: Display the Timing screen.

Press [TIMING] , [Hx12 3 J] .

The display should look like Figure 10-27. Confirm that either active edge will create the same recording.

Press [A→B] , [CLOCK SELECT] , change active edges [▽ SET] twice, [▷] twice, [Hx3 1 H] , [ARM] , [DATA] , [COMPARE A/B] .

There should be no inequalities. Turn off the Comparison mode. Press [COMPARE A/B] .

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.00 16:20:37 MEM=M
                    CLOCK SELECT

                  MODE = EXTERNAL SINGLE-PHASED

    INT. CLOCK PERIOD = 0100 NANOSECONDS

 MASTER CLOCK = (____•____•AJ↑)+(____+____+____)

 SAMPLE CLOCK

   C = SAME AS MASTER

   B = SAME AS MASTER

   A = SAME AS MASTER

 ENABLE  --  used only in Latch & Demux.)

   C = EXT (CR↑•____•____)+(____+____+____)

   B = EXT (CR↑•____•____)+(____+____+____)

   A = EXT (CR↑•____•____)+(____+____+____)

 MASTER CLOCK = 1.00µS

 C=    R=    (R-C)=    (          ) CL=  LEVEL=0 RDY
```

Figure 10-26. Clock Select for AJ↑.

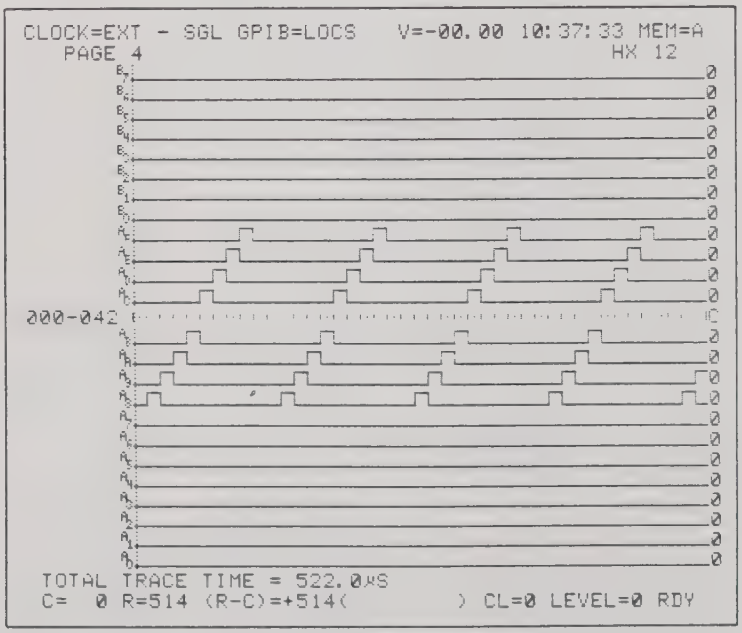

Figure 10-27. Recording for Sample Clock = AJ↑ or AJ↓.

10.2.4.3 **Sample on a Pair of External Clocks (AJ↓ and AK↑)**

SET UP: See setup guide in Figure 10-28.

A sample will be taken at each rising edge of the resultant sample clock which is created by combining AJ| and AK^ into a logical OR expression (Figure 10-29). Each odd-numbered input pulse is sampled once.

Change Clock Select display to the following:

MASTER CLOCK = (___·___· AJ↓) + (__ + __ + AK↑)

Change trace control to S = 02

Press [CLOCK SELECT], [▽ SET] twice, [▷] twice, [Hx3 1 H],
[TRACE CONTROL], [▽ SET] twice, [Hx1 0 G], [Hx6 2 I].

RECORD: Press [ARM].

REVIEW: Display timing screen. Press [TIMING].

The display should look like Figure 10-30. See Figures 10-31 and 10-32 for clocking with AJ↑ + AK↓. For Figure 10-31, a sample is taken at each rising edge of the resultant sample clock. Each even numbered input pulse is sampled twice. See Figures 10-33 and 10-34 for clocking with AJ↓ and AK↓. For Figure 10-33, a sample is taken at each rising edge of the resultant sample clock. Each even-numbered input pulse is sampled once.

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ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #4.3b OF ___ DATE _____

See back for notes (3) DATA FORMAT MIXED USER SEQN.

TRACE CONTROL NOTES

RADIX: H H

MSB	
6	
DATA 5	
4	
3	AEAB
2	AEAA
1	ADA9
LSB	ACA8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL

LEVEL 0 (QUICK KEY, OF) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (OF)

COMMENTS

(3) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY

S = 0 2

(2) JUMP TO 0 (OF) NEVER

J = X X

(2) ADVANCE NEVER

A = X X

(1) TRACE ALWAYS

T = X X

LEVEL ___ (QUICK KEY, OF) DELAY = ___ (DEC/HEX, 0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (OF)

COMMENTS

(.....) STOP

S =

(.....) JUMP TO ___ (OF)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

LEVEL ___ (QUICK KEY, OF) DELAY = ___ (DEC/HEX, 0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (OF)

COMMENTS

(.....) STOP

S =

(.....) JUMP TO ___ (OF)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

LEVEL ___ (QUICK KEY, OF) DELAY = ___ (DEC/HEX, 0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (OF)

COMMENTS

(.....) STOP

S =

(.....) JUMP TO ___ (OF)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

Figure 10-28. Setup Guide Sample on Pair of External Clocks (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # __ OF 43b DATE ____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ_↓) + (_____+_____+AK_↑)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY — FORMAT & DESCRIPTION

1 HEX — Fixed hex format & LF AD sequence

OCTAL — Fixed octal format & LF AD sequence

BINARY — Fixed binary format & LF AD sequence

3 MIXED USER SEQN — Any order any sequence

4 MIXED LF AD SEQN — Any order fixed LF AD sequence

5 DEVICE MNEMONICS — Fixed disassembled op code format only if RTE 816 attached OR

6 DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY — SAMPLE CLOCK CHOICES

1 ↑ ACTIVE RISING EDGE; ↓ ACTIVE FALLING EDGE; NOT USED

QUICK KEY — ENABLE CLOCK CHOICES

1 ↑ POSITIVE TRUE; ↓ NEGATIVE TRUE; NOT USED

QUICK KEY — MODE & DESCRIPTIONS

1 INTERNAL — A Mode: A and B sampled at the rising edge of Master clock (MCLK). B Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK).

2 EXTERNAL SINGLE PHASED — A Mode: A and B sampled at the rising edge of Master clock (MCLK). B Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK).

3 EXTERNAL MULTI PHASED — Each input sampled at the rising edge of its Master clock (MCLK). A Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK). B Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK).

4 MIXED SINGLE PHASED — Master clock (MCLK) is the rising edge of Master clock (MCLK). A Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK). B Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK).

5 MIXED MULTI PHASED — Each input sampled at the rising edge of its Master clock (MCLK). A Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK). B Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK).

6 INTERNAL LATCHED — Latch sampled at the rising edge of Master clock (MCLK). A Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK). B Mode: A sampled at the rising edge of Master clock (MCLK). B sampled at the falling edge of Master clock (MCLK).

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512 R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY — MODE CHOICES

SAMPLE — SAMPLE; GLITCH — GLITCH; LATCH — LATCH; DEMUX — DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	0.00 TO +9.00 VDC
B	VARB	0.00 TO +9.00 VDC

QUICK KEY — ARM COMMAND CHOICES

1 MANUAL; AUTO; AUTO STOP IF A B; AUTO STOP IF A + B; + AUTO STOP IF A B WITH N LIMITS; - AUTO STOP IF A + B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	+	+	+	+	+	+	+	+	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY — POLARITY CHOICES

+ POSITIVE; - NEGATIVE

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Figure 10-28. Setup Guide Sample on Pair of External Clocks (Sheet 2 of 2).

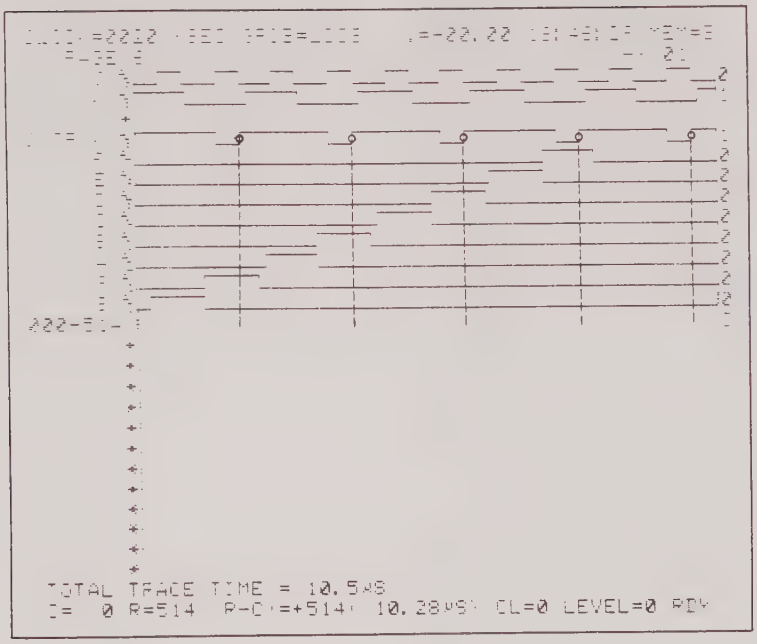

Figure 10-29. Sample Clock = AJ↓ + AK↑.

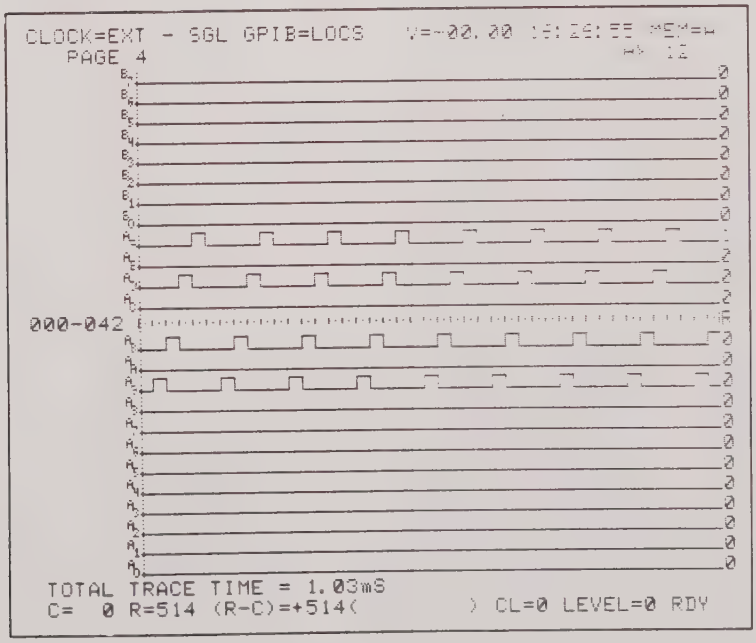

Figure 10-30. Recording for Sample Clock = AJ↓ + AK↑.

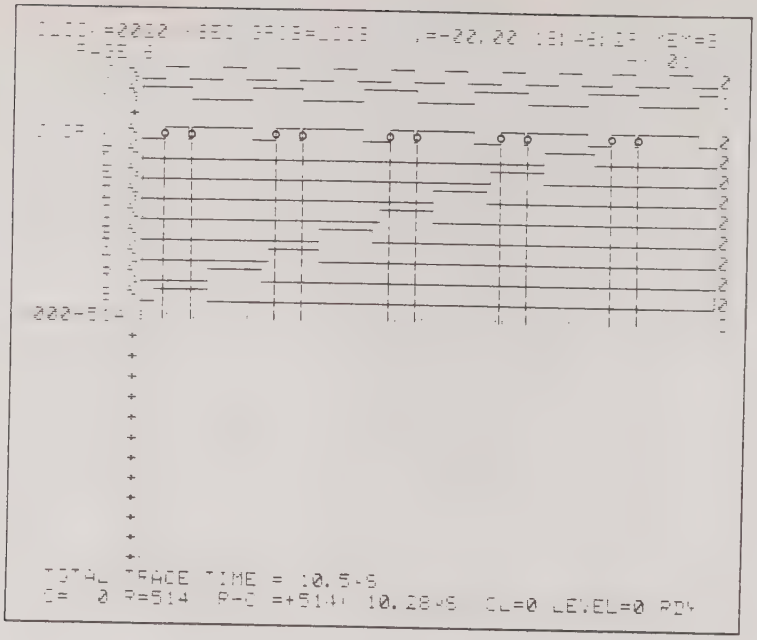

Figure 10-31. Sample Clock = AJ↑ + AK↓.

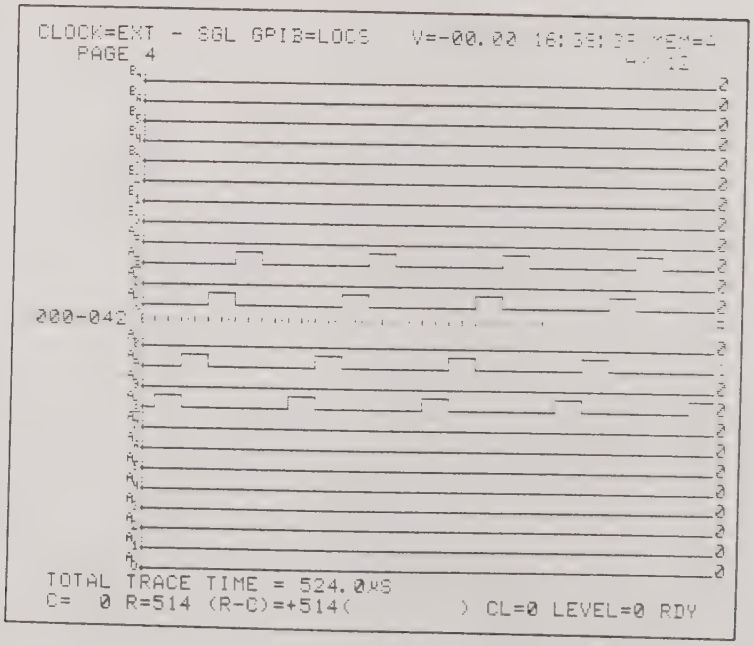

Figure 10-32. Recording for Sample Clock = AJ↑ + AK↓.

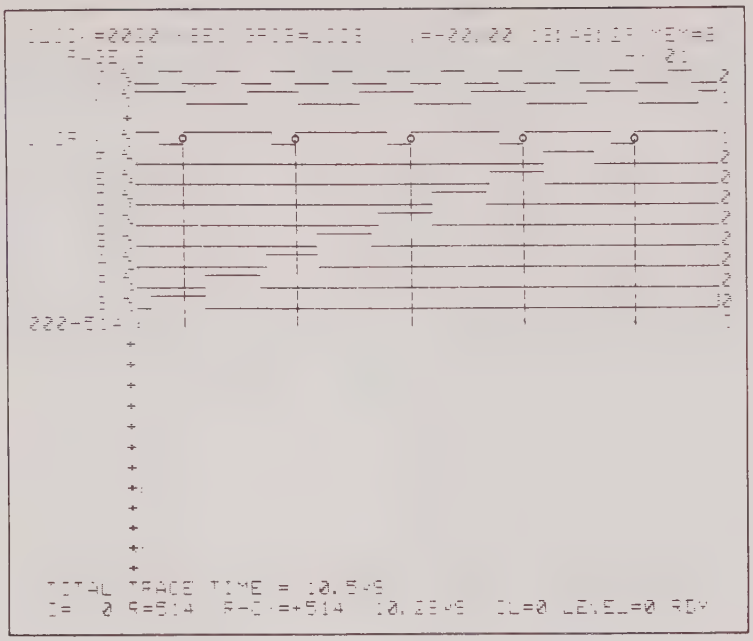

Figure 10-33. Sample Clock = AJ↓ + AK↓.

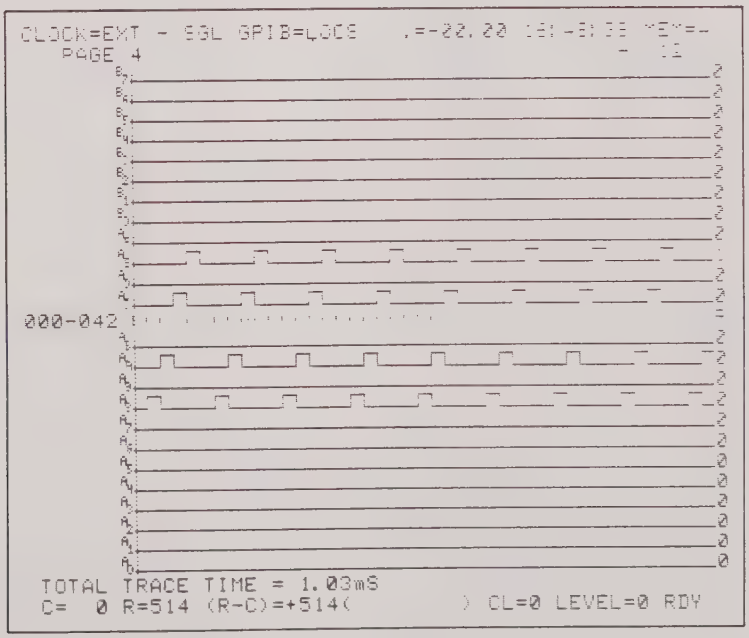

Figure 10-34. Recording for Sample Clock = AJ↓ + AK↓.

10.2.4.4 Latch (Enable) on a Single Input (AR↑, AR↓)

SET UP: See setup guide in Figure 10-35. Disconnect the AF through A8 probe from PROBE TEST connector and connect the A7 through A0 probe. Display page 6 of the Timing screen.

Press [TIMING], [PAGE ↓ 4 K] twice.

Inputs are held at the levels that exist when the latch enable signal goes false, then are released to be able to change when the signal is true. All transitions occur while the inputs are latched and, therefore, change synchronously with AR↑ going high. The latched inputs are then asynchronously sampled.

The inputs are latched while AR↑ is false (low) and released while it is true (high). Every transition is latched; therefore, all the inputs change synchronously with the rising edge of AR↑ (see Figure 10-36).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 44a OF ___ DATE _____

Quick Key (3) See back for notes DATA FORMAT MIXED USER SEQN.

RADIX: H_H

MSB	
6	
D N 5	
A P 4	
T J 3	A7A3
A 1 2	A6A2
S 1	A5A1
LSB	A4A0

RADIX CHOICES (B) BINARY (O) OCTAL, (H) HEX (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come due on any of nine conditions

Quick Key	Command Condition	
J	if DATA = D	
1	Always	
2	Never	
3	if DATA = D and Sample Count >	Delay
4	if DATA = D and Sample Count <	Delay
5	if DATA = D and Sample Count =	Delay
6	if DATA ≠ D and Sample Count >	Delay
7	if DATA ≠ D and Sample Count <	Delay
8	if DATA ≠ D and Sample Count =	Delay

D = S, J, A, or T, which are assigned by command type!

TRACE CONTROL

LEVEL 0 (Quick Key, 0-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

LEVEL ___ (Quick Key, 0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (0-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (Quick Key, 0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (0-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (Quick Key, 0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (0-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

Figure 10-35. Setup Latch (Enable) on a Single Input (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #44a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (O) MODE = INTERNAL

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = 40

■ NANOSECONDS (20-1600)
□ MICROSECONDS (1-1600)
□ MILLISECONDS (1-160)

MASTER = ■ INTERNAL □ EXT (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION C = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____ ● _____ ● _____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION B = (_____ ● _____ ● _____) + (_____ + _____ + _____)

SECTION A = (_____ ● _____ ● AR ↑) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY — FORMAT & DESCRIPTION

3 HEX — Fixed hex format & CF AO sequence
OCTAL — Fixed octal format & CF AO sequence
2 BINARY — Fixed binary format & CF AO sequence
3 MIXED USER SEQN — Any radix any sequence
4 MIXED CF AO SEQN — Any radix fixed CF AO sequence
5 DEVICE MNEMONICS — Fixed disassembled µP code format (only if RTE 816 attached)
OR
6 DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY — SAMPLE CLOCK CHOICES
↑ ACTIVE RISING EDGE
↓ ACTIVE FALLING EDGE
NOT USED

QUICK KEY — ENABLE CLOCK CHOICES
↑ POSITIVE TRUE
↓ NEGATIVE TRUE
NOT USED

QUICK KEY — MODE & DESCRIPTIONS

INTERNAL — [illegible]

INTERNAL [illegible] — [illegible]

INTERNAL [illegible] — [illegible]

[illegible]

[illegible]

INTERNAL EXTENDED — [illegible]

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	LATCH	ECL	-1.30

PASS COUNTER:
LIMIT = ____ 0-9999

QUICK KEY (O) ARM MODE: MANUAL
LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY — MODE CHOICES
SAMPLE — SAMPLE
SLITCH — SLITCH
LATCH — LATCH
DEMUX — DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY — ARM COMMAND CHOICES
MANUAL
[illegible]

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	±	±	±	±	±	±	±	±

POLARITY NOTES

DIRECT ENTRY KEY — POLARITY CHOICES
POSITIVE
NEGATIVE

DWS24-12 5183

Figure 10-35. Setup Latch (Enable) on a Single Input (Sheet 2 of 2).

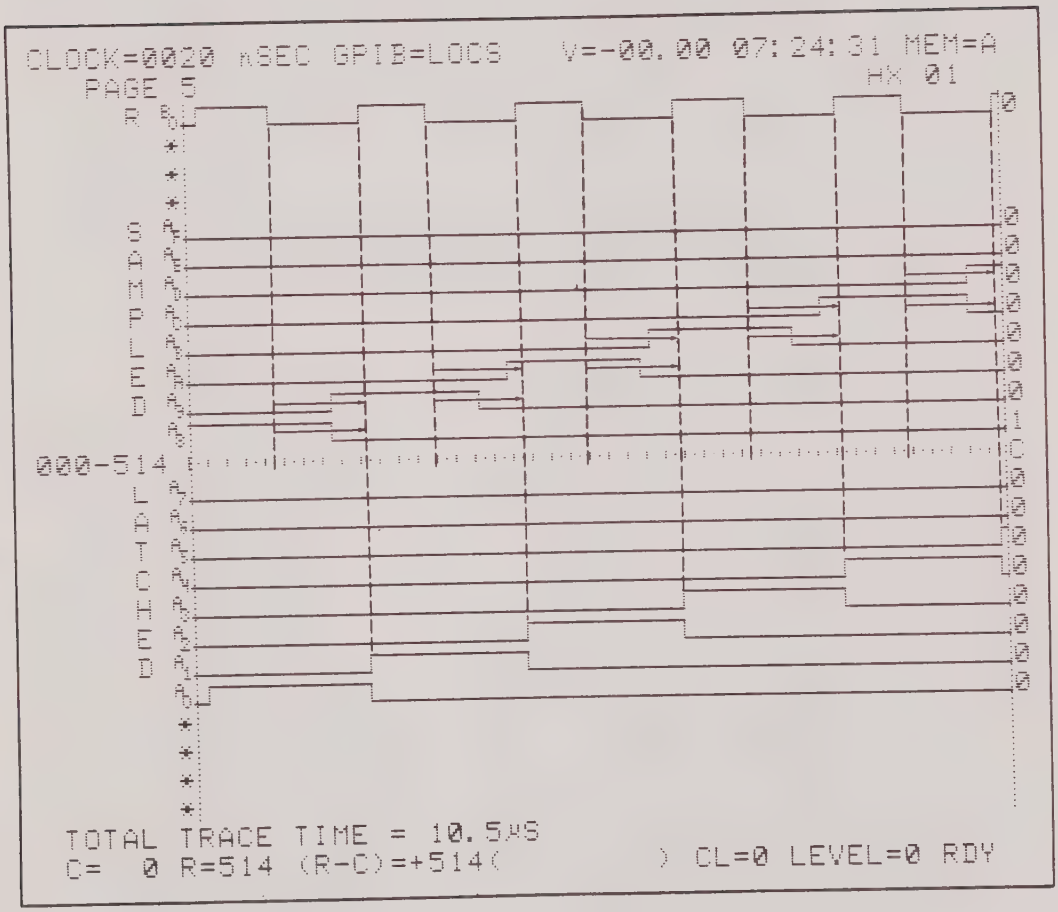

Figure 10-36. Enable = AR↑.

Set up the Clock Select screen.

Press [CLOCK SELECT], [Hx1 0 G], [▽ SET], [PAGE 4 K], [Hx1 0 G], [▽ SET] three times, [Hx6 2 I], [▷] twice, [Hx1 0 G].

Display the Input Mode screen.

Press [INPUT MODE], [△] twice, [LATCH E U OCTAL], [▷], [EBCDIC 9 P ECL].

Display the Data Format screen.

Press [DATA FORMAT], [▽ SET] twice, [ASCII A Q A], [V6 7 N], [ASCII A Q A], [V12 6 M], [ASCII A Q A], [V24 5 L], [ASCII A Q A], [PAGE 4 K], [▽ SET], [ASCII A Q A], [Hx12 3 J], [ASCII A Q A], [Hx6 2 I], [ASCII A Q A], [Hx3 1 H], [ASCII A Q A], [Hx1 0 G].

Display Trace Control screen.

Press [TRACE CONTROL], [▽ SET] twice, [Hx1 0 G], [Hx3 1 H].

Clock Select and Input Mode screens should look like Figures 10-37 and 10-38.

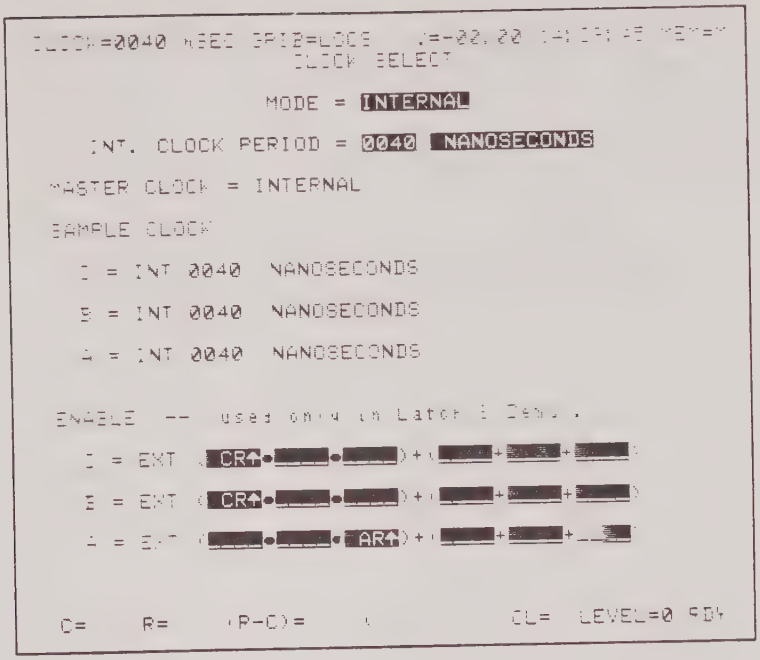

Figure 10-37. Clock Select for Enable = AR↑.

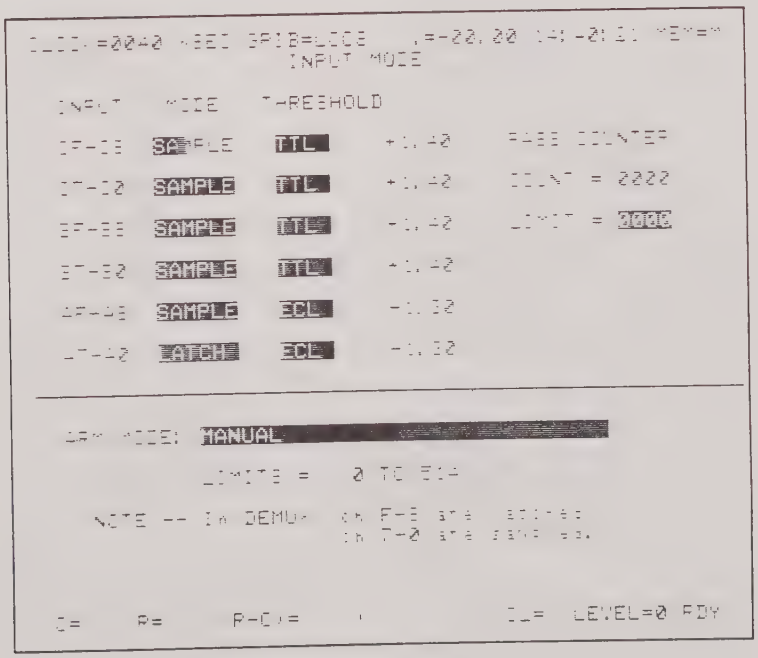

Figure 10-38. Input Mode for Latch on Single Input.

RECORD: Press [ARM] .

REVIEW: Display the Timing screen. Press [TIMING] .

The display should look like Figure 10-39. Note that all transitions now occur synchronously.

SET UP: When AR↓ is used, the inputs are latched while AR↓ is false (high) and released while it is true (low). Since the latching occurs totally within each pulse (i.e., no input signal transitions occur during the latch period), the latch signal has no effect on the inputs (see Figure 10-40).

Change the Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+__)

Press [CLOCK SELECT] , [▽ SET] four times, [▷] twice, [1 H×3 H] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

When AR↓ is used this display should look like Figure 10-41. Note that the transitions are asynchronous.

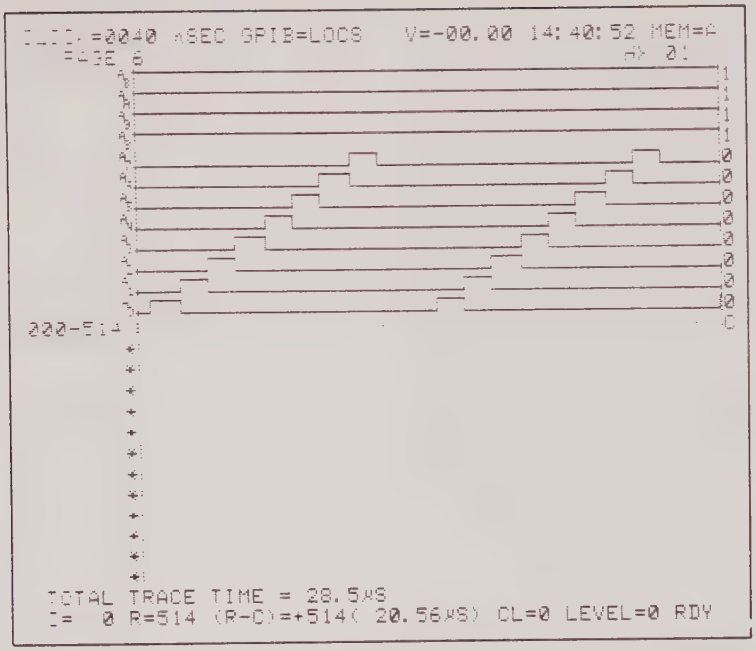

Figure 10-39. Recording of Asynchronously Sampled Latched Inputs for Enable = AR↑.

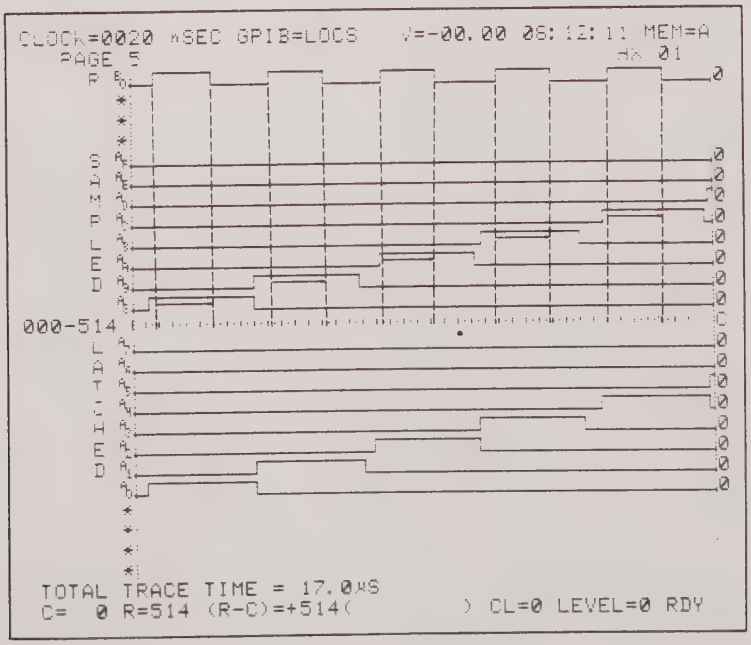

Figure 10-40. Function of Input Signal Transitions Latch Enable Signal.

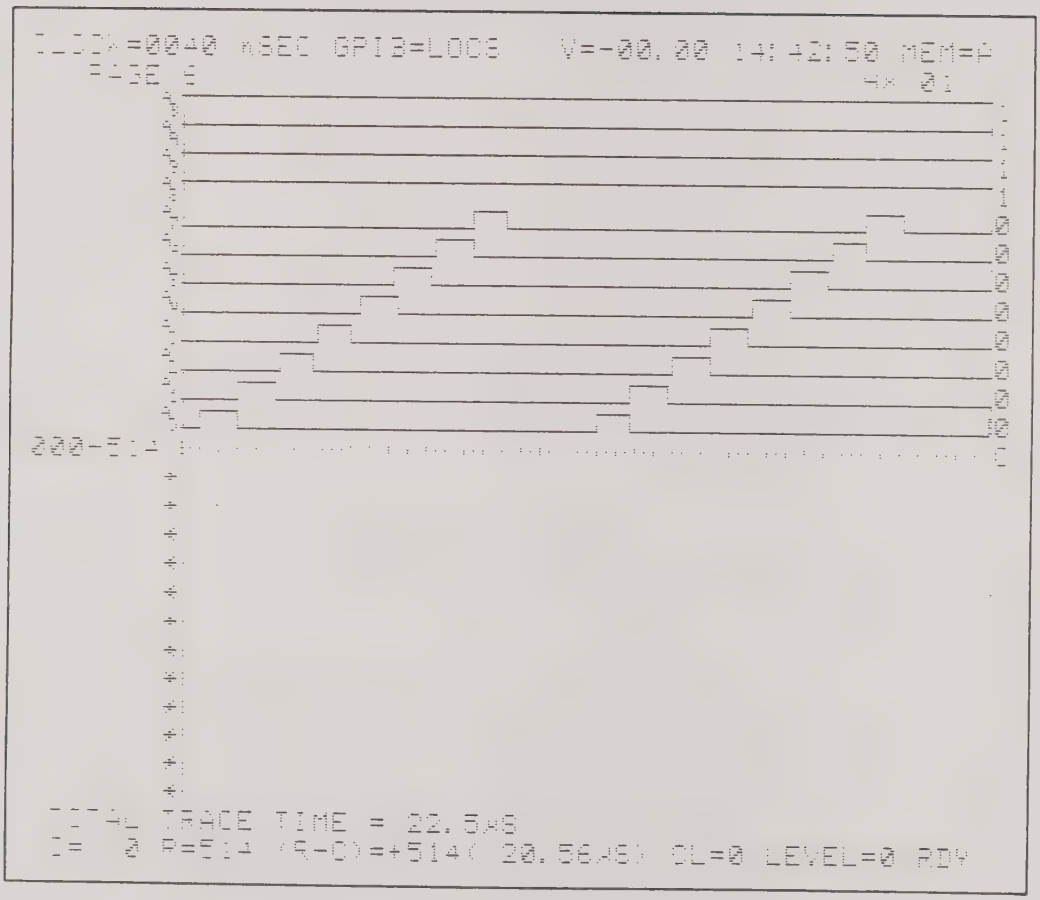

Figure 10-41. Recording for Enable = AR↓.

SET UP: When AS↑ is used the inputs are latched while AS↑ is false (low) and released while it is true (high). Every other transition is latched (see Figure 10-42). Note that every other input transition occurs during a latched period and, therefore, cannot change until enable returns to true.

When AS↑ is used the Timing display should look like Figure 10-43. Note that every other transition is synchronous.

SET UP: When AS↓ is used the inputs are latched while AS↓ is false (high) and released while it is true (low). Every other transition is latched (see Figure 10-44) or every other input transition AS↓ occurs during a latched period and, therefore, cannot change until enable returns to true.

When AS↓ is used the Timing display should look like Figure 10-45.

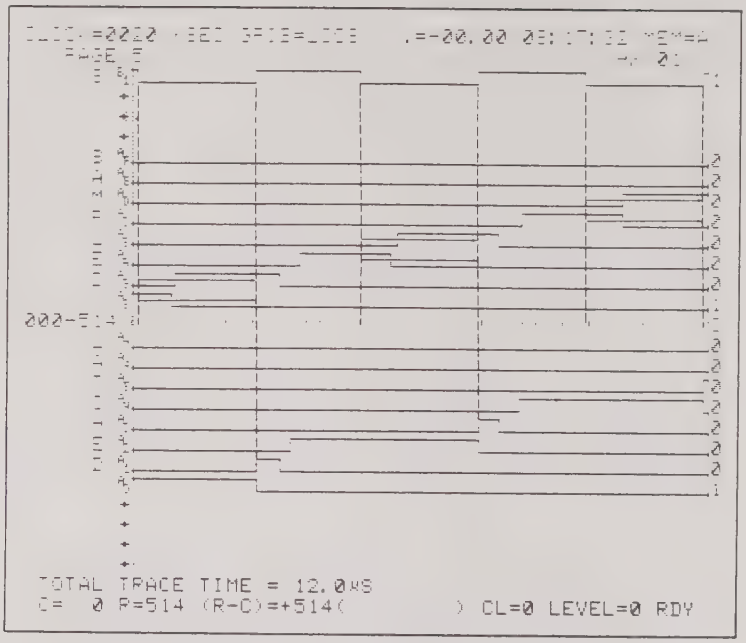

Figure 10-42. Enable = AS↑ Every Other Transition Latched.

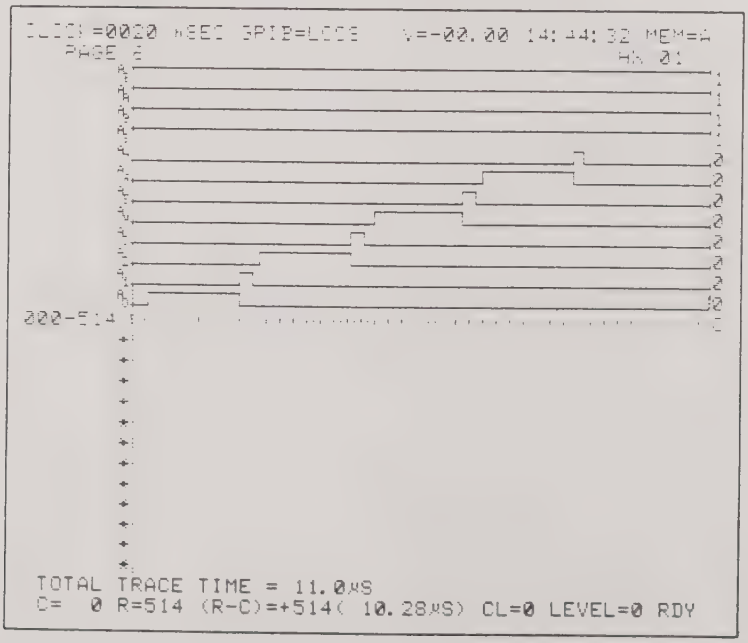

Figure 10-43. Time Recording for Enable = AS↑.

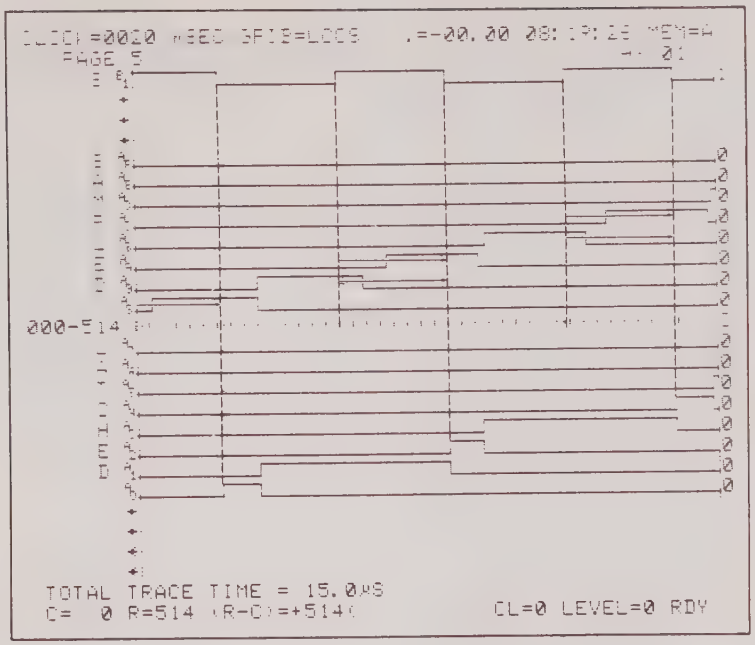

Figure 10-44. Enable = AS↓, Inputs Latched When AS↓ True.

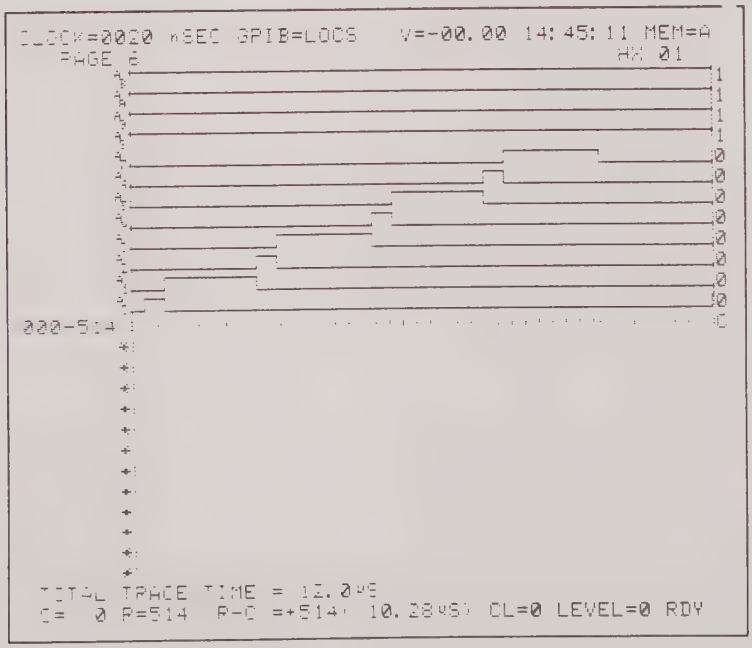

Figure 10-45. Recording for Enable = AS↓.

10.2.4.5 Latch (Enable) on a Combination of Inputs (AR↑ + AS↑, AR↓ + AS↑, AR↑ + AJ↓, AR↓ + AJ↓)

SET UP: The latch enable signal is created by combining AR^ and AS| into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Every other transition is latched (see Figure 10-46). Every other input transition occurs during a latched period and, therefore, cannot change until the enable expression becomes true.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↑) + (__+__+ AS↑)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx1 0 G], [▷] three times, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Display the Timing screen. Press [TIMING].

The display should look like Figure 10-47.

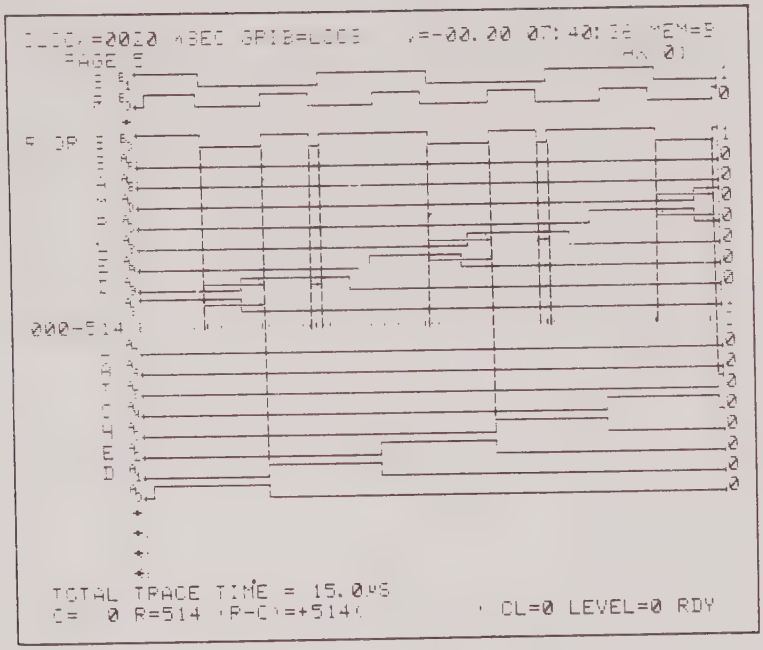

Figure 10-46. Enable = AR↑ + AS↑.

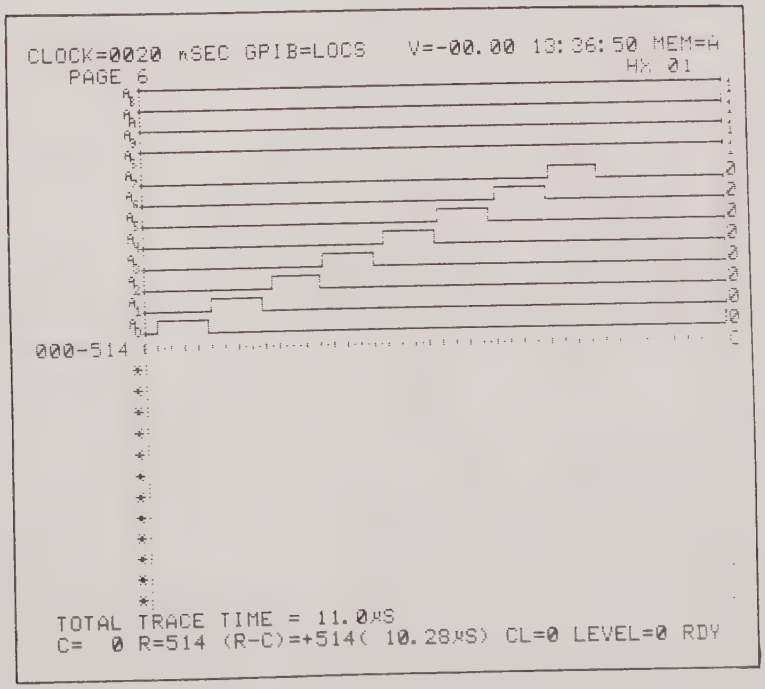

Figure 10-47. Recording for Enable = AR↑ + AS↑.

SET UP: When AR↓ + AS↑ is used, the latch enable signal is created by combining AR↓ and AS↓ into a logical OR expression. The inputs are latched while the resultant enable signal is false and released while it is true. Since latching occurs totally within every other pulse, the latch signal has no affect on the inputs (see Figure 10-48). No input transitions occur during a latched period; therefore, the Enable expression has no affect on the inputs.

When AR↓ + AS↑ is used, the Timing display should look like Figure 10-49.

SET UP: When AR↑ + AS↓ is used the latch enable signal is created by combining AR↑ and AS↓ into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Latching occurs at every other transition (see Figure 10-50). Note that every other input transition occurs during a latched period and, therefore, cannot change until enable becomes true.

Change Clock Select display to the following:

ENABLE A = EXT (__ · __ · AR↑) + (__ + __ + AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx1 0 G], [▷] three times, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↑ + AS↓ is used, the Timing display should look like Figure 10-51.

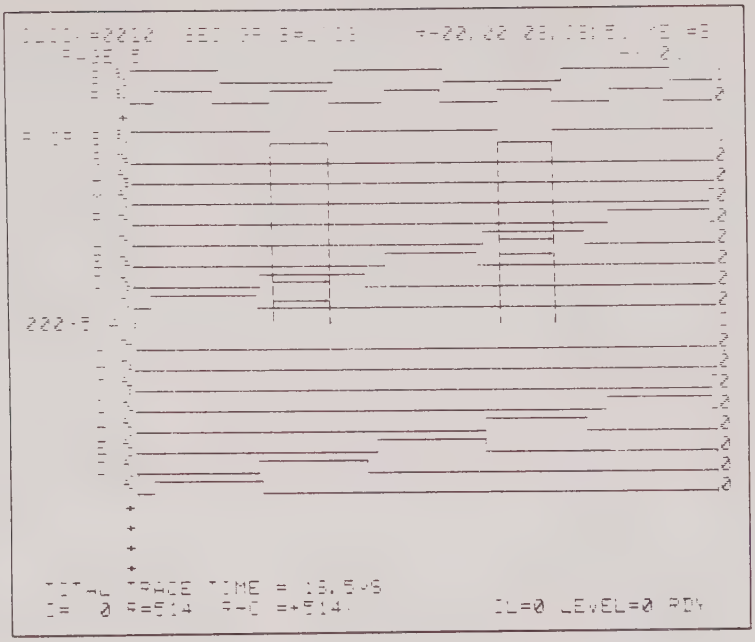

Figure 10-48. Enable = AR↓ + AJ↑.

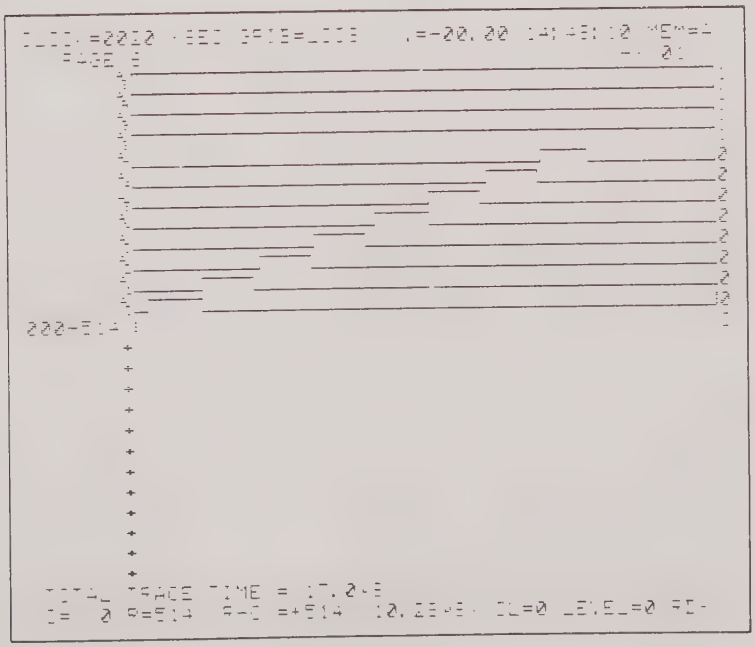

Figure 10-49. Recording for Enable = AR↓ + AS↑.

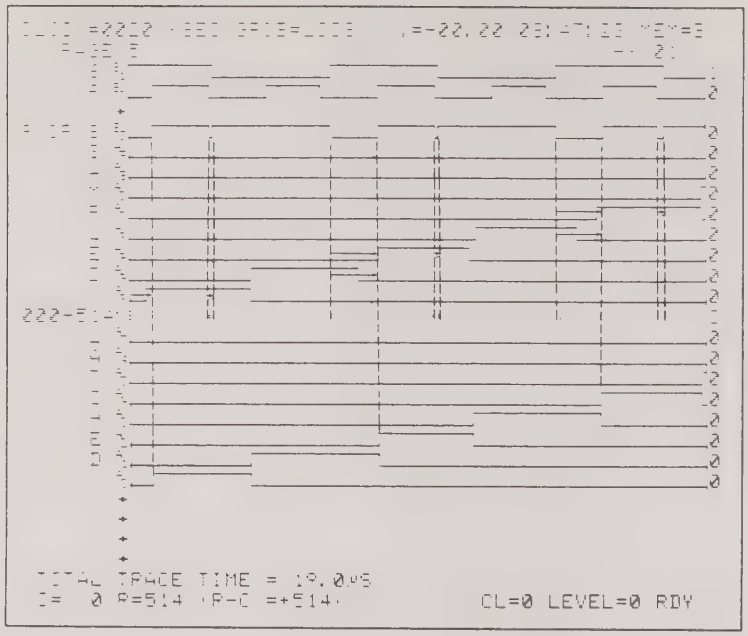

Figure 10-50. Enable = AR↑ + AS↓.

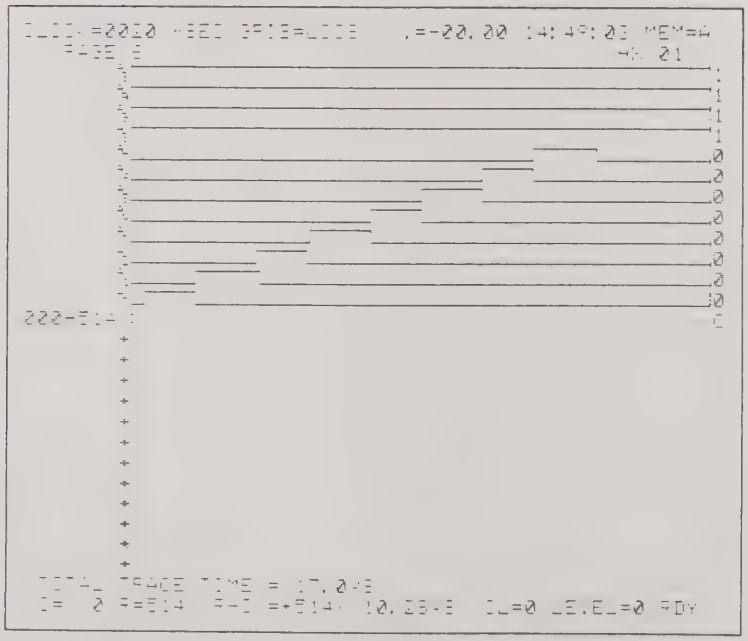

Figure 10-51. Recording for Enable = AR↑ + AS↓.

SET UP: When AR↓ + AS↓ is used the latch enable signal is created by combining AR↓ and AS↓ into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Since the latching occurs totally within every other pulse, the latch signal has no affect on the inputs (see Figure 10-52). Note that no input transitions occur during a latched period; therefore, latch enable has no affect on the inputs.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+ AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] five times, [1 H] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

When AR↓ + AS↓ is used, the Timing display should look like Figure 10-53.

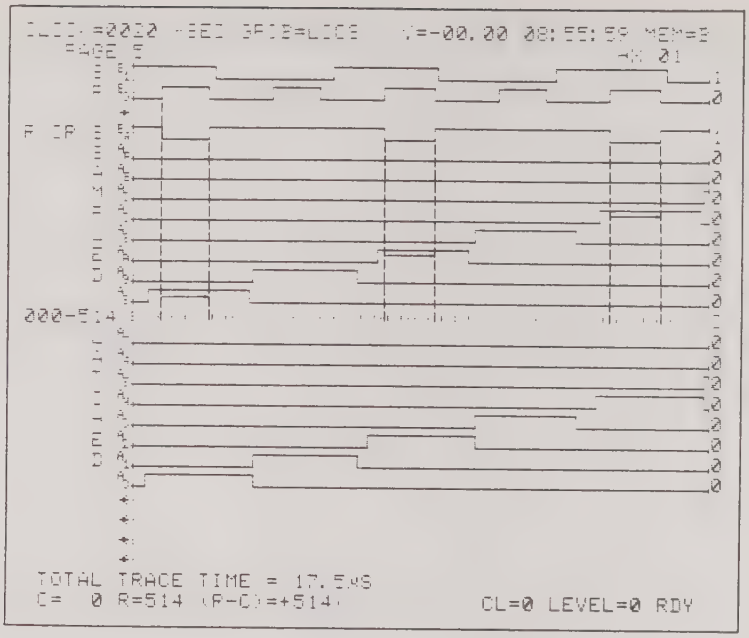

Figure 10-52. Enable = AR↓ + AS↓.

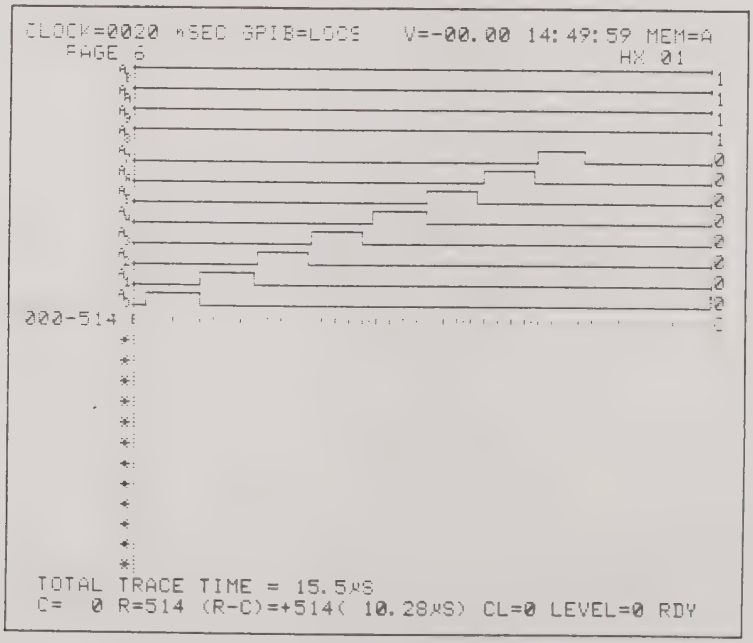

Figure 10-53. Recording for Enable = AR↓ + AS↓.

10.2.4.6 **Demultiplex on a Single Enable Input (AR↑, AR↓, AS↑, AS↓)**

SET UP: The inputs on A7 through A0 are put in the Sample input mode. The inputs on A7 to A0 are also sent to AF through A8 and latched there by the enable signal AR↑.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↑) + (__+__+__)

Change Input mode for inputs AF through A8 and A7 through A0 to display DEMUX.

Display Clock Select screen. Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [0 G], [▷] three times, [2 H] .

Display Input Mode screen. Press [INPUT MODE], [△] three times, [F V DEMUX HEX] .

RECORD: Press [ARM] .

REVIEW: Display Timing screen. Press [TIMING] .

The display should look like Figure 10-54. The same information is sampled on inputs A7 through A0 and latched before sampling on AF through A8.

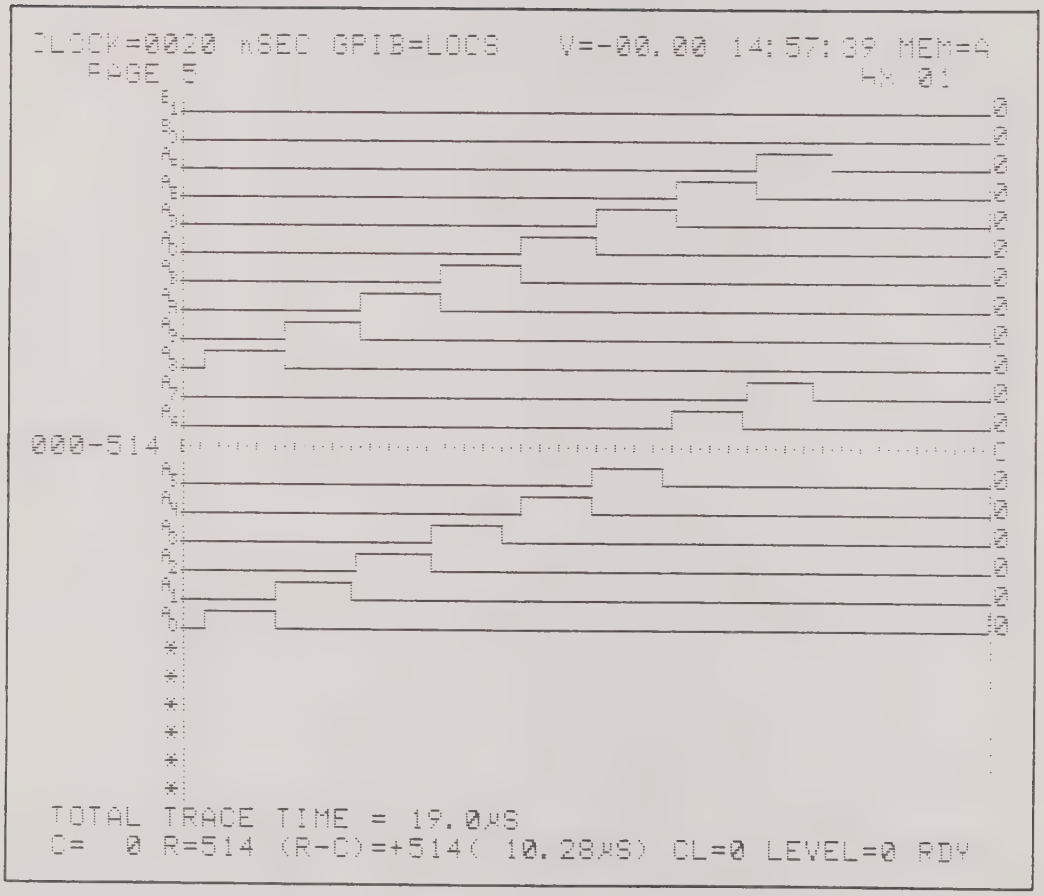

Figure 10-54. AF Through A8 Latched by AR↑.

SET UP: When AR↓ is used the A7 through A0 inputs also sent to AF through A8 are latched there by the enable signal AR↓.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+__)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↓ is used, the Timing display should look like Figure 10-55. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓.

SET UP: When AS↑ is used, the A7 through A0 inputs also sent to AF through A8 are latched there by the enable signal AS↑.

When AS↑ is used, the Timing display should look like Figure 10-56. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AS↑.

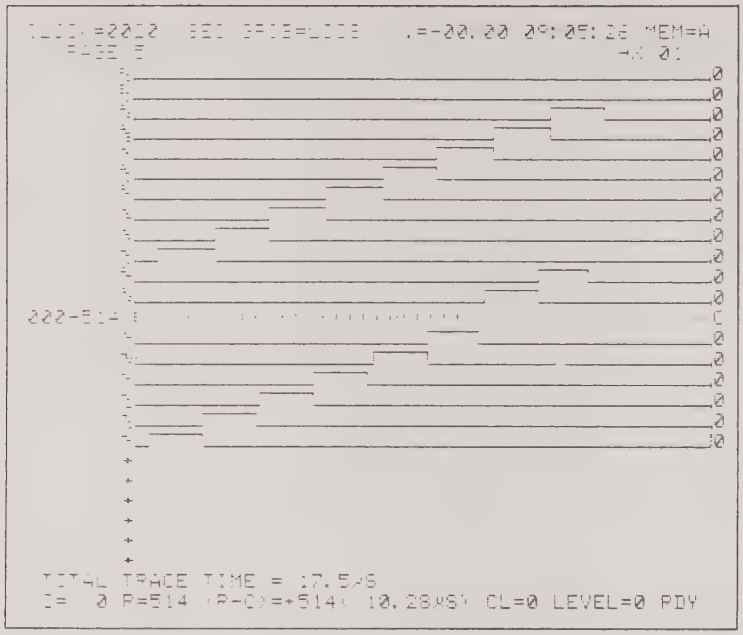

Figure 10-55. AF Through AS Latched by AR↓.

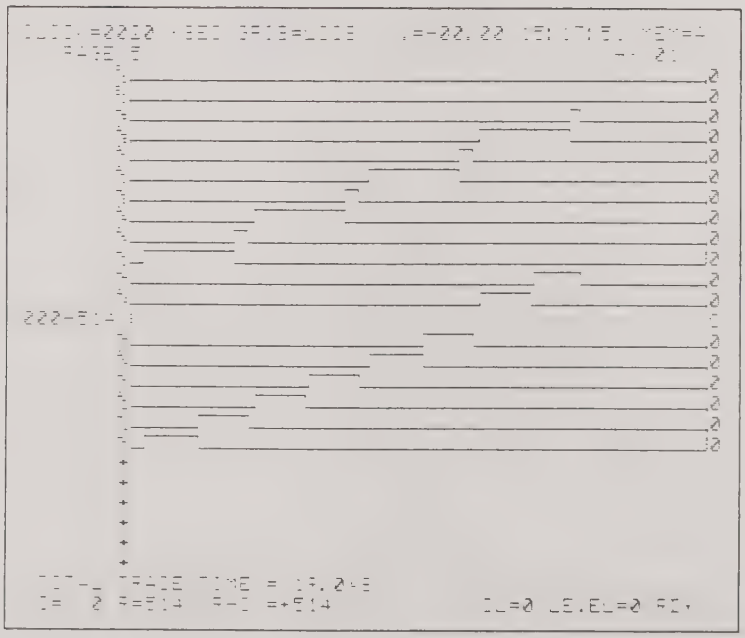

Figure 10-56. AF Through A8 Latched by AS↑.

SET UP: When AS↓ is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AS↓.

Change Clock Select display to the following:

ENABLE A = EXT (__·__·__) + (__+__+ AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] five times, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AS↓ is used, the Timing display should look like Figure 10-57. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AS↓.

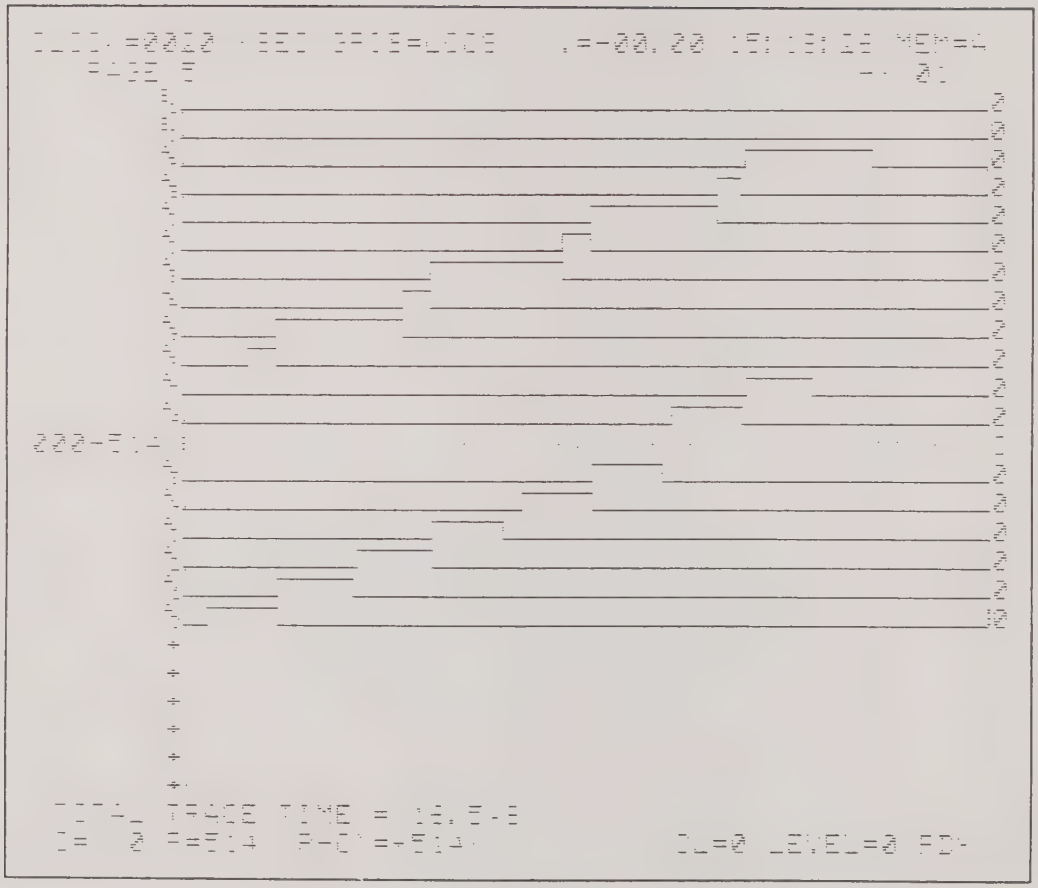

Figure 10-57. AF Through AS Latched by AS↓.

10.2.4.7 Demultiplex on a Combination of Enable Signals (AR↑ + AS↑, AR↓ + AS↑, AR↑ + AS↓, AR↓ + AS↓)

SET UP: The A7 through A0 inputs, also sent to AF through A8, are latched there by the enable signal AR↑, AS↑. Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↑) + (__+__+ AS↑)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx1 0 G], [▷] three times, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Display the Timing screen. Press [TIMING].

The display should look like Figure 10-58. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↑ + AS↑.

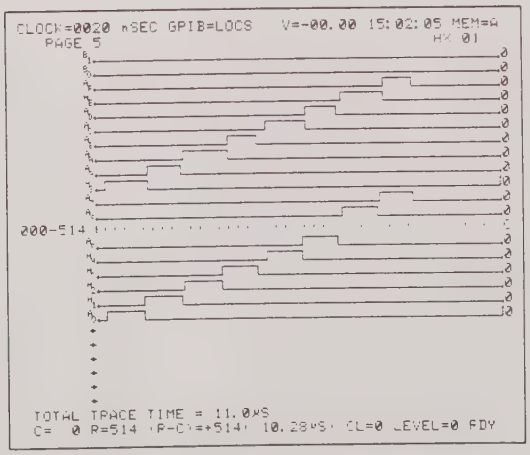

Figure 10-58. AF Through A8 Latched by AR↑ + AS↑.

SET UP: When AR↓ + AS↑ is used, the A7 through A0 inputs, also sent to AF through A8, are latched there by the enable signal AR↓ + AS↑.

Change Clock Select display to the following:

ENABLE A = EXT (__ · __ · AR↓) + (__ + __ + AS↑)

Press [CLOCK SELECT] , [▽ SET] four times, [▷] twice, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

When AR↓ + AS↑ is used, the display should look like Figure 10-59. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓ + AS↑.

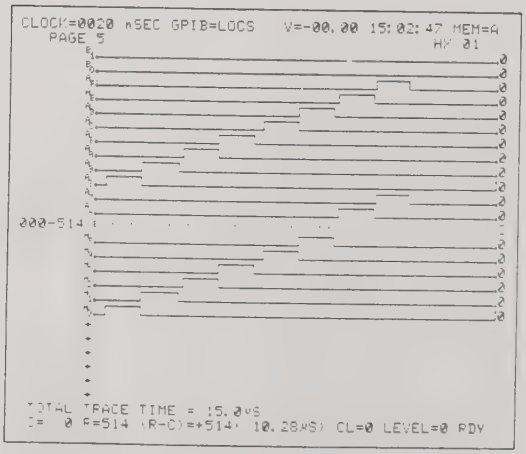

Figure 10-59. AF Through A8 Latched by AR↓ + AS↑.

SET UP: When AR↑ + AS↓ is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AR↑ + AS↓.

When AR↑ + AS↓ is used, the Timing display should look like Figure 10-60. Demultiplexing the information, on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↑ + AS↓.

SET UP: When AR↓ + AS↓is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AR↓ + AS↓.

When AR↓ + AS↓ is used, the Timing display should look like Figure 10-61. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓ + AS↓.

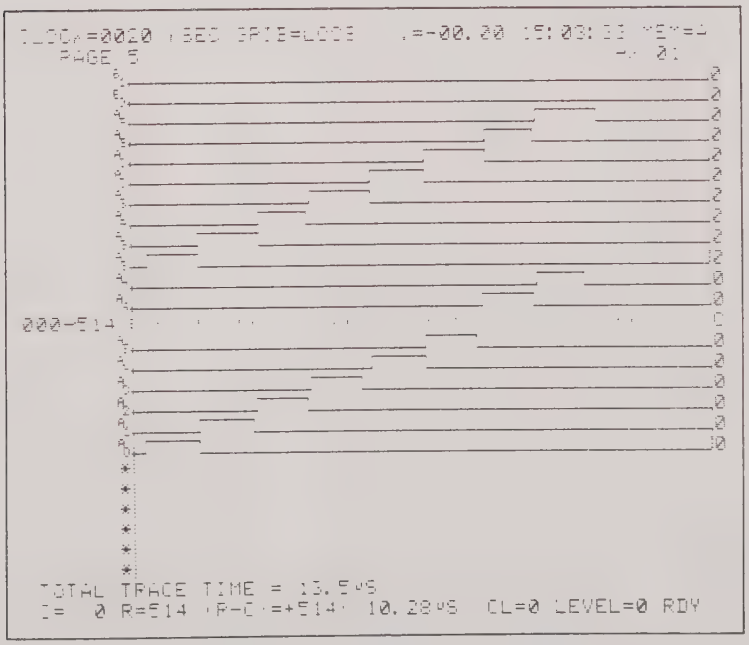

Figure 10-60. AF Through AS Latched by AR↑ + AS↓.

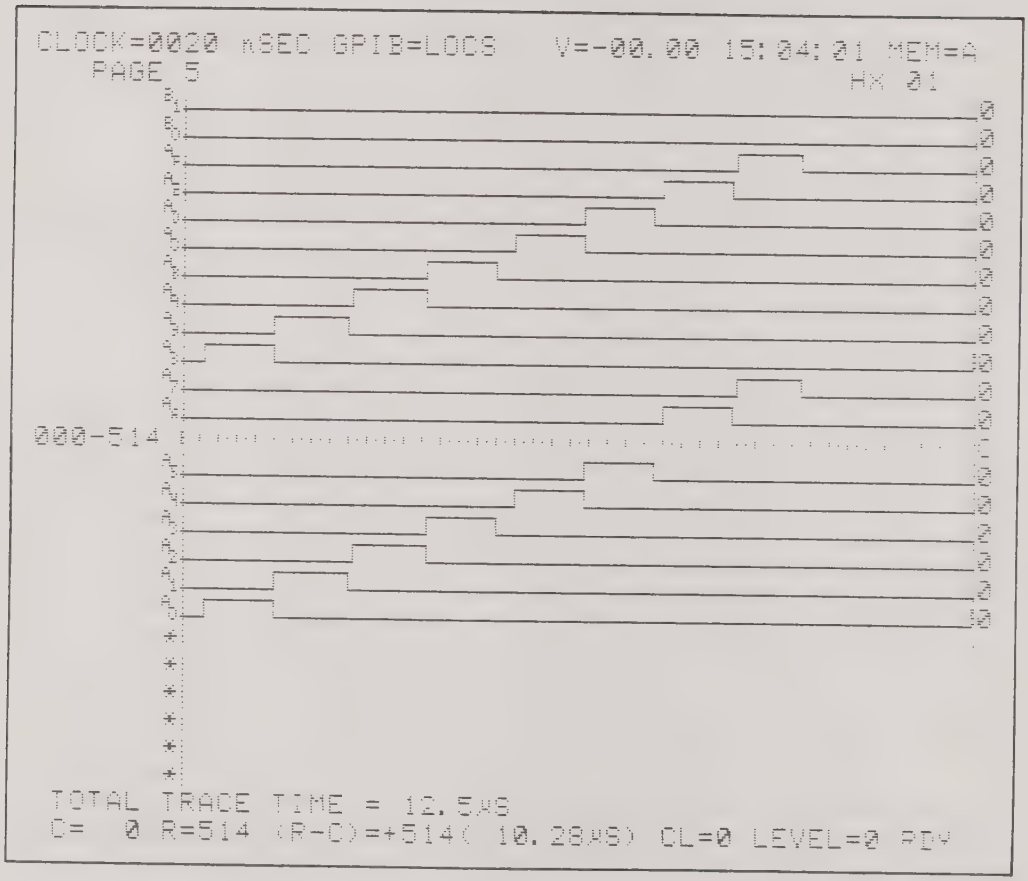

Figure 10-61. AF Through A8 Latched by AR↓ + AS↓.

10.2.5 TRACE CONTROL

The following are specific examples of the basic building blocks of trace control. There are some minor variations in some of the commands. (For example, TRACE IF DATA = T is often substituted for TRACE NEVER to better illustrate the recording process.) You may also notice some difference between a figure and what is displayed on your screen. This is due to remaining values from previous trace control routines. Specifically, if a command is NEVER or ALWAYS, then the value of its associated word recognizer is ignored, as if it were "don't care." Similarly, if DELAY is not used in any of a level's commands, then the specified delay value is ignored, as if it were "zero."

10.2.5.1 **Fill Memory with Samples from Anywhere in Data Stream**

SET UP: Unplug the A7 through A0 probe and connect the AF through A8 probe to PROBE TEST. See setup guide in Figure 10-62.

Display Clock Select screen.

Press [CLOCK SELECT], [Hx3 1 H], [▽ SET] twice, [▷] five times, [Hx6 2 I].

Display Input Mode screen.

Press [INPUT MODE], [△], [Hx3 1 H], [△] twice, [SAMPLE C S].

Display Data Format screen.

Press [DATA FORMAT], [Hx12 3 J], [▽ SET] twice, [ASCII A O A], [DEMUX F V HEX], [ASCII A O A], [LATCH E U OCTAL], [ASCII A O A], [GLITCH D T DECIMAL], [ASCII A O A], [SAMPLE C S],

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #51.1 OF ___ DATE _____

See back for notes (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
6	
D N 5	
A P 4	
T U 3	AFAB
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

LEVEL 0 (QUICK KEY, OF) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (OF)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY

S = X X

(2) JUMP TO 0 (OF) NEVER

J = X X

(2) ADVANCE NEVER

A = X X

(1) TRACE ALWAYS

T = X X

COMMENTS

515 SEQUENTIAL SAMPLES WILL BE RECORDED BEGINNING AT A RANDOM LOCATION.

LEVEL ___ (QUICK KEY, OF) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (OF)

(.....) STOP

S =

(...) JUMP TO ___ (OF)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

COMMENTS

LEVEL ___ (QUICK KEY, OF) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (OF)

(.....) STOP

S =

(.....) JUMP TO ___ (OF)

J =

(..) ADVANCE

A =

(.....) TRACE

T =

COMMENTS

LEVEL ___ (QUICK KEY, OF) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (OF)

(.....) STOP

S =

(. ..) JUMP TO ___ (OF)

J =

(. ..) ADVANCE

A =

( ) TRACE

T =

COMMENTS

Figure 10-62. Setup Guide: Fill Memory with Samples from Anywhere in Data Stream (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXT. SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - AO sequence
1	OCTAL Fixed octal format & CF - AO sequence
2	BINARY Fixed binary format & CF - AO sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF - AO SEQN Any radix fixed CF - AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 818 attached OR
5	DEVICE NOT AVAILABLE No RTE 818 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	- - - - NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	- - - - NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate. Section A - Section B - Section C - internal clock period

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate. Section A - Section B - Section C - Master external

2 EXTERNAL MULTI PHASED
Each section can be sampled at (each) external rate or Master external rate. Section A, Section B, Section C & Master can be different external repetitions

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate - internal clock period or 10ns. Section A, Section B and or Section C - Master external or internal clock period or 10ns

4 MIXED MULTI PHASED
Master must be external. Each section can be sampled at (each) external rate - the Master external rate - internal clock period or 10ns. Section A, Section B and or Section C - Master external or internal or 10ns

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C - internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (1) ARM MODE: AUTO

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-62. Setup Guide: Fill Memory with Samples from Anywhere in Data Stream (Sheet 2 of 2).

[▽] SET, [A] Q (ASCII, A), [B] R (BINARY, B), [A] Q (ASCII, A), [A] Q (ASCII, A), [A] Q (ASCII, A),

[9] P (EBCDIC, ECL), [A] Q (ASCII, A), [8] O (PAGE↑, TTL).

Display Trace Control screen.

Press [ ] (TRACE CONTROL), [▽] SET, [3] J (Hx12), [▽] SET, [*] SPACE (DON T CARE) twice.

The Trace Control screen should look like Figure 10-63.

RECORD: Press [ ] (ARM).

REVIEW: Display Timing screen.

Press [ ] (TIMING), [3] J (Hx12). You should be on page 4.

Observe how the pattern starts in a different location for every recording. This is because no unique starting or stopping location is specified for capturing the information; it happens randomly.

Stop.

Press [ ] (STOP).

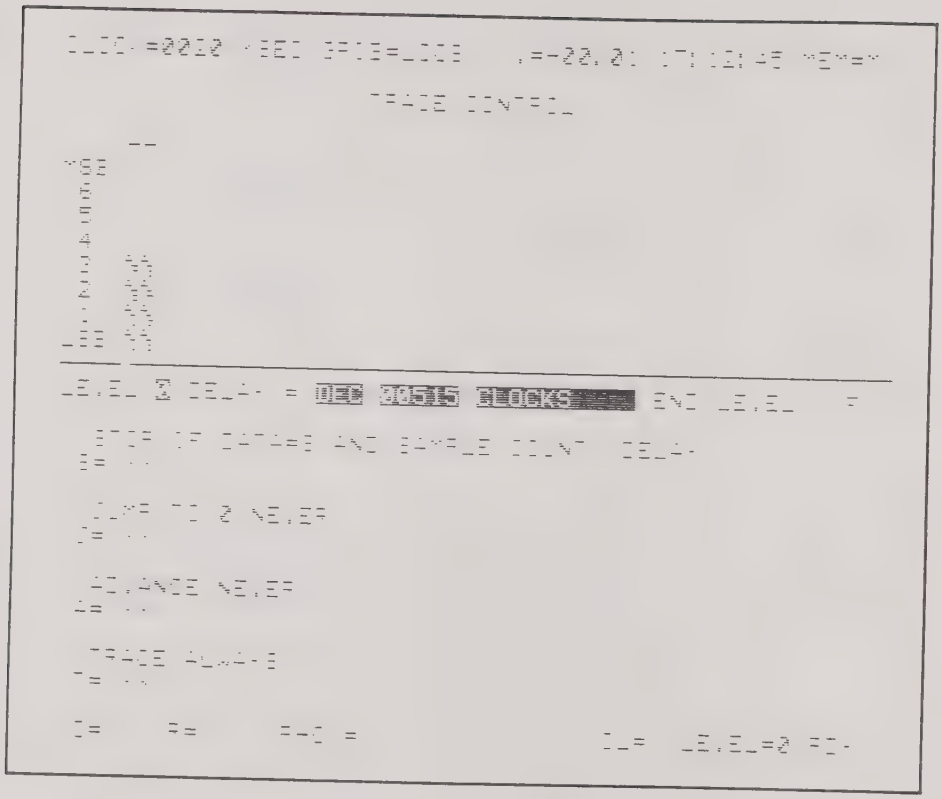

Figure 10-63. Fill Memory From Anywhere in the Data Stream.

10.2.5.2 Record What Happens Immediately After an Event

SET UP: Change the trace control program to be as in Figures 10-64 and 10-65.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▷] twice, [V24 5 L], [Hx3 1 H], [Hx3 1 H], [▽ SET], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Display Timing screen. Press [TIMING].

Notice that the pattern consistently starts in the same location.

Press [DATA] to see the same thing in the Data Domain display. Stop. Press [STOP].

This display should look like Figure 10-66. Note that the event of interest is the word 01 at location 000; it was captured by the trace control conditions on level 0, as indicated by CL = 0.

Press [▷] (see Figure 10-67).

Note that this and all subsequent words in memory were captured by trace control level 1.

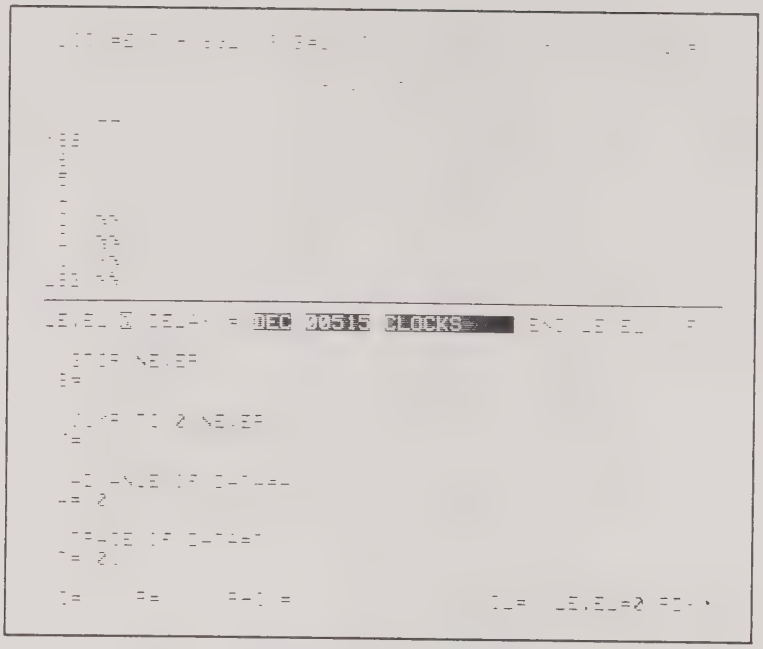

Figure 10-64. First Level, Record Immediately After Event 01.

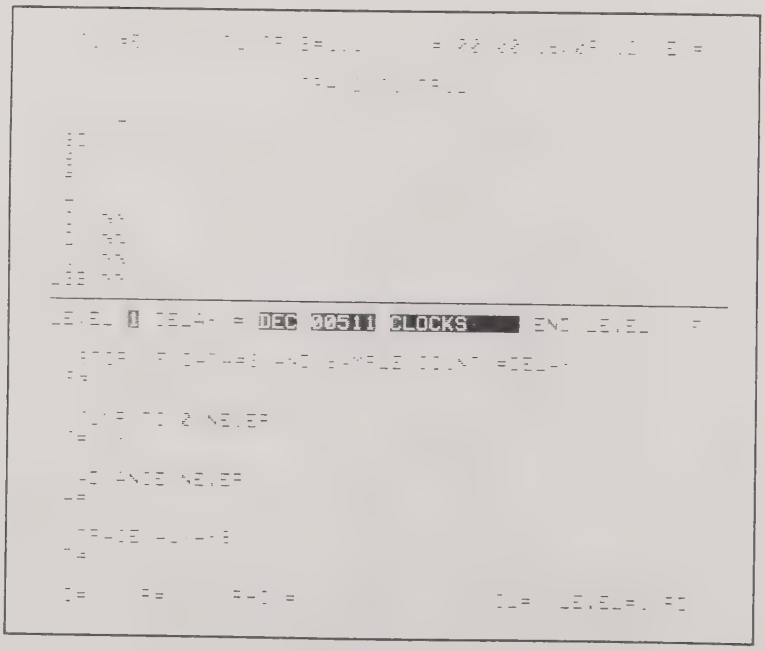

Figure 10-65. Second Level, Record Immediately After Event 01.

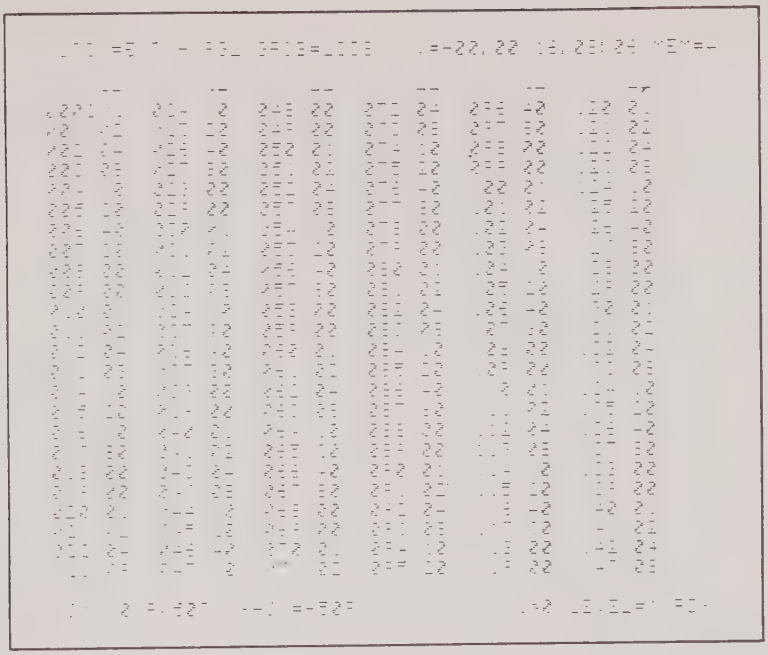

Figure 10-66. Event 01 Recorded by Trace Level 0.

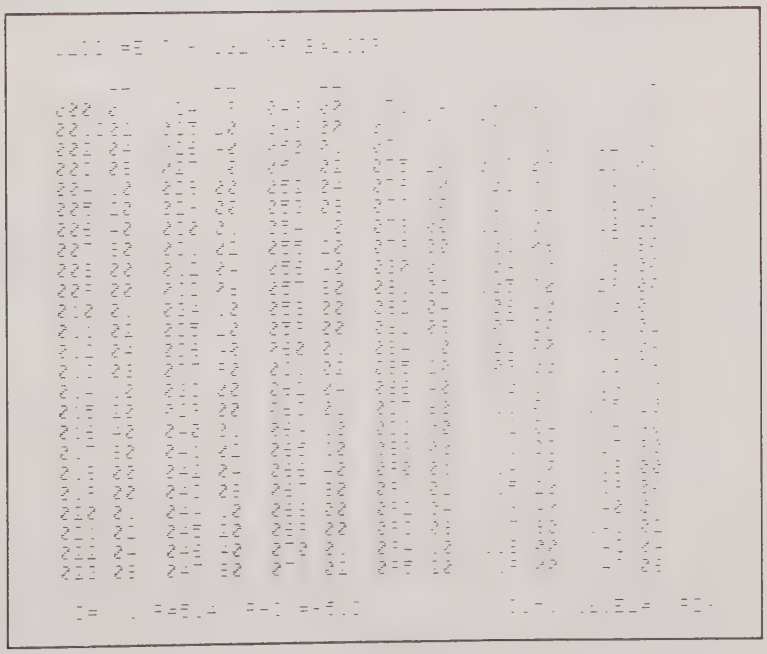

Figure 10-67. Words Recorded by Trace Level 1.

10.2.5.3 Record What Happens Immediately Before an Event

SET UP: Change the arm mode to manual.

Press [INPUT MODE], [△], [Hx1 0 G].

Change trace control.

Press [TRACE CONTROL], [▽ SET], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Show the Data display. Press [DATA].

Note that CL = F and that the data are all zeros.

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [Hx1 0 G], [DATA].

Press [▷] until CL = 0 (see Figure 10-68).

This is the first traced sample. Tracing continued until 01 occurred and then stopped. Since the Probe Test pattern generator output is continuous and your press of [ARM] is asynchronous with it, tracing can start at any point in the cycle. However, since the pattern repeats every ten sample clocks, a maximum of nine words can occur before the S = 01 condition is met. To see how the first word sampled can vary, press [ARM] again and then [◁ SET], or [▷].

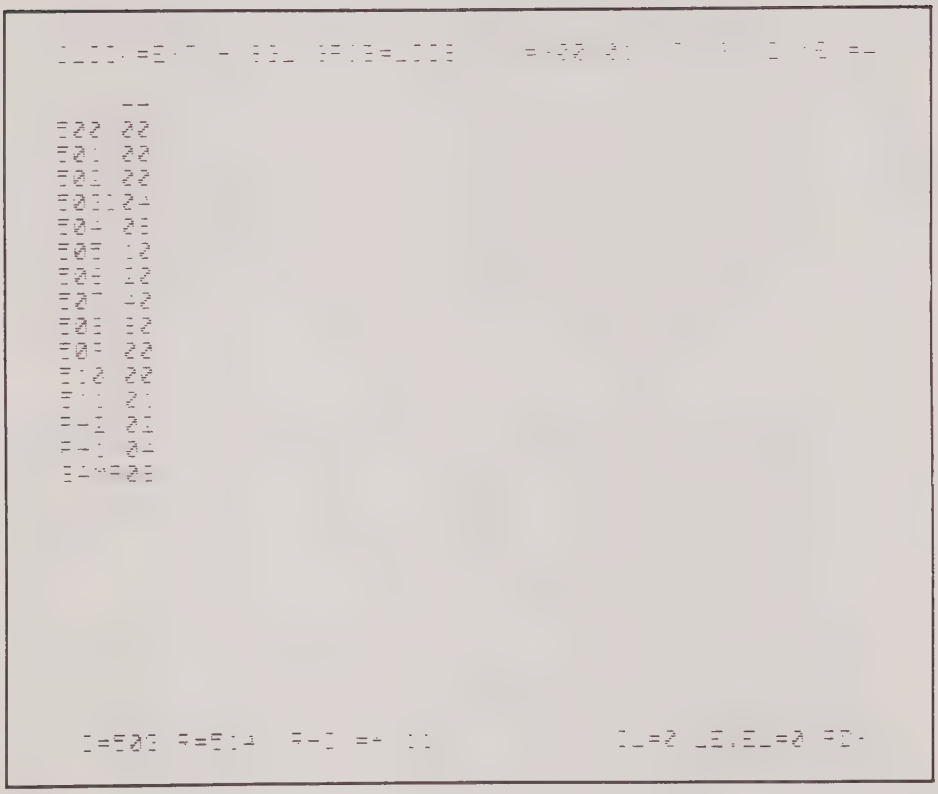

Figure 10-68. First Traced Sample.

This finds the first word captured on level 0 (indicated by CL = 0). Note that location 511 always holds the word 01. Repeat this process several times.

Press ▷ until C is at location P-2 (see Figure 10-69).

Note that CL = ?. These last three locations (also referred to as 512, 513, and 514) are the pipeline and sample register contents -- words not yet evaluated by the trace control circuitry.

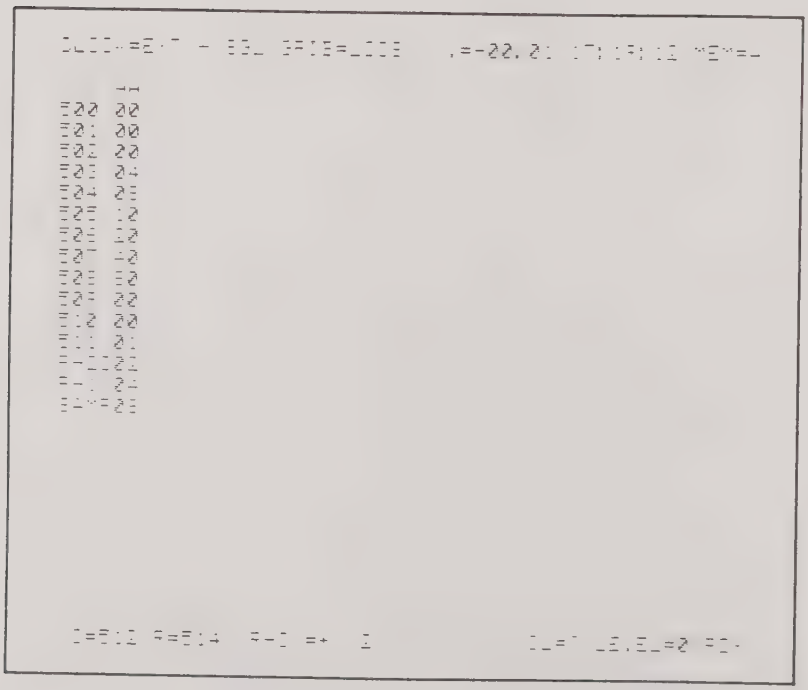

Figure 10-69. Last Three Displayed Words Sampled.

10.2.5.4 **Record What Happens Around an Event**

SET UP: The following will put an event of interest in the middle of memory. Specifically, to put word 01 in sample location 246, the stop of tracing must be delayed by 265(511 - 246) sample clocks. Change the trace control program.

Press [TRACE CONTROL], [▽ SET], [▽ SET] twice, [Hx1 0 G], [▽ SET] three times, [Hx3 1 H], [▷] twice, [Hx6 2 I], [V12 6 M], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx6 2 I], [Hx12 3 J], [V12 6 M], [DATA].

Press [▷] until C is at location 246.

The display will look similar to Figure 10-70. The event of interest, 01, has been placed at the specified mid-memory location 246. Note that 01 was recorded there by trace level 0. The following 265 words were recorded by trace level 1. (Again, because of Probe Test's repetitive pattern, only up to nine words could have been recorded on level 0 before 01 occurred.)

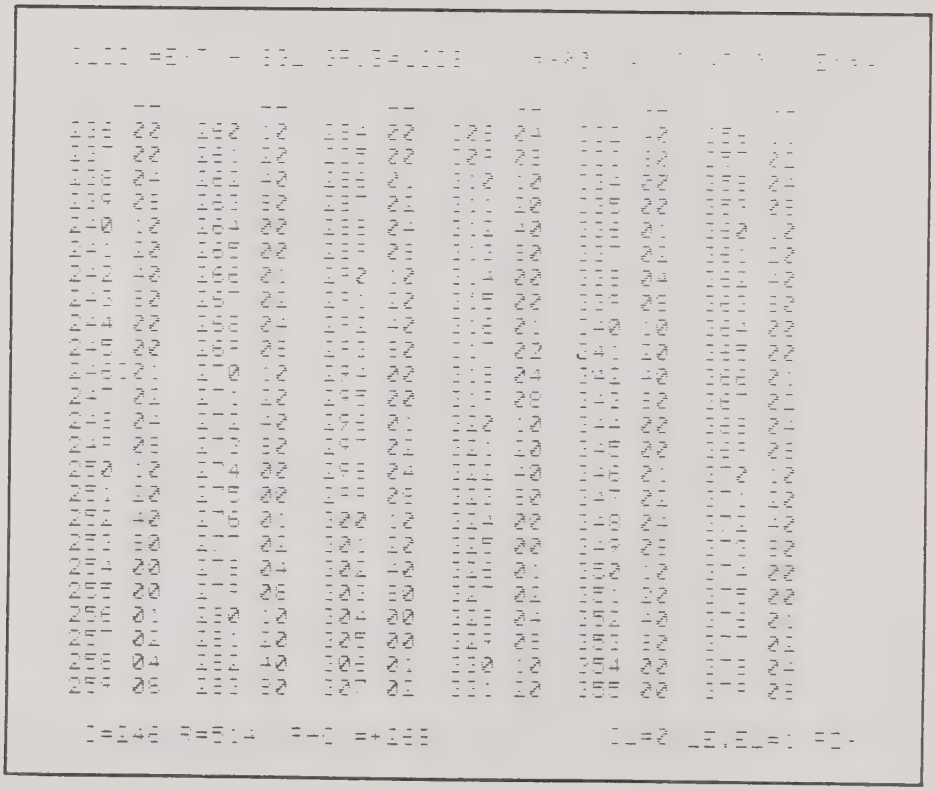

Figure 10-70. Event Placed at Location 246.

10.2.5.5 **Record What Happens Long After an Event**

SET UP: Use the setup guide of Figure 10-71. This will capture a memory full of information long after an event, as well as the event itself, yet without the intervening information.

Press [TRACE CONTROL], [▽ SET] five times, [Hx1 0 G], [▽ SET],
[Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▷] twice,
[V24 5 L], [Hx3 1 H], [V24 5 L], [▽ SET], [▽ SET] twice,
[V24 5 L], [▽ SET] twice [Hx6 2 I], [▽ SET], [Hx6 2 I],
[▷] twice, [V24 5 L], [Hx3 1 H], [Hx1 0 G], [▽ SET],
[V24 5 L].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [DATA].

The display should look like Figure 10-72. Recording the words in locations 002 to 511 was delayed from recording the word at location 001 by 515 sample clocks. The intervening words were not recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 51.1D OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX:		H H
	MSB	
	6	
D N	5	
A P	4	
T U	3	AFAB
A T	2	AEAA
S	1	ADA9
	LSB	ACA8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count < Delay
4	If DATA = D and Sample Count > Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count ≤ Delay
7	If DATA = D and Sample Count ≥ Delay
8	If DATA = D and Sample Count ≠ Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(0) TRACE IF DATA = A
T = 0 1

COMMENTS

ONLY 01 IS TRACED INTO MEMORY. AT ITS OCCURANCE, TRACE CONTROL ADVANCES TO LEVEL 1.

LEVEL 1 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = X X
(2) TRACE NEVER
T = X X

COMMENTS

NOTHING IS TRACED IN THIS LEVEL IT MERELY WAITS FOR 515 CLOCKS TO OCCUR BEFORE ADVANCING.

LEVEL 2 (O-F) DELAY = DEC (DEC/HEX) 510 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(5) STOP IF DATA = S AND SAMPLE COUNT = DELAY
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS

THE REST OF MEMORY IS FILLED WITH THE NEXT 510 SEQUENTIAL SAMPLES.

LEVEL ___ (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(____) STOP
S =
(____) JUMP TO ___ (O-F)
J =
(____) ADVANCE
A =
(____) TRACE
T =

COMMENTS

Figure 10-71. Setup Guide: Record What Happens Around an Event (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.2 D

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - A0 sequence
1	OCTAL Fixed octal format & CF - A0 sequence
2	BINARY Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF - A0 SEQN Any radix fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	— — — NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	— — — NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate. Section A - Section B - Section C - internal clock period.

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate. Section A - Section B - Section C - Master external.

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external rate or Master external rate. Section A - Section B - Section C & Master can be different external expressions.

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A - Section B and or Section C - Master external or internal clock period or 10ns.

4 MIXED MULTI PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A - Section B and or Section C - Master external or internal or 10ns.

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns. Section A - Section B and or Section C - internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (O) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP B	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP A	±	±	±	±	±	±	±	±	_	_	_	_	_	_	_	_

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-71. Setup Guide: Record What Happens Around an Event (Sheet 2 of 2).

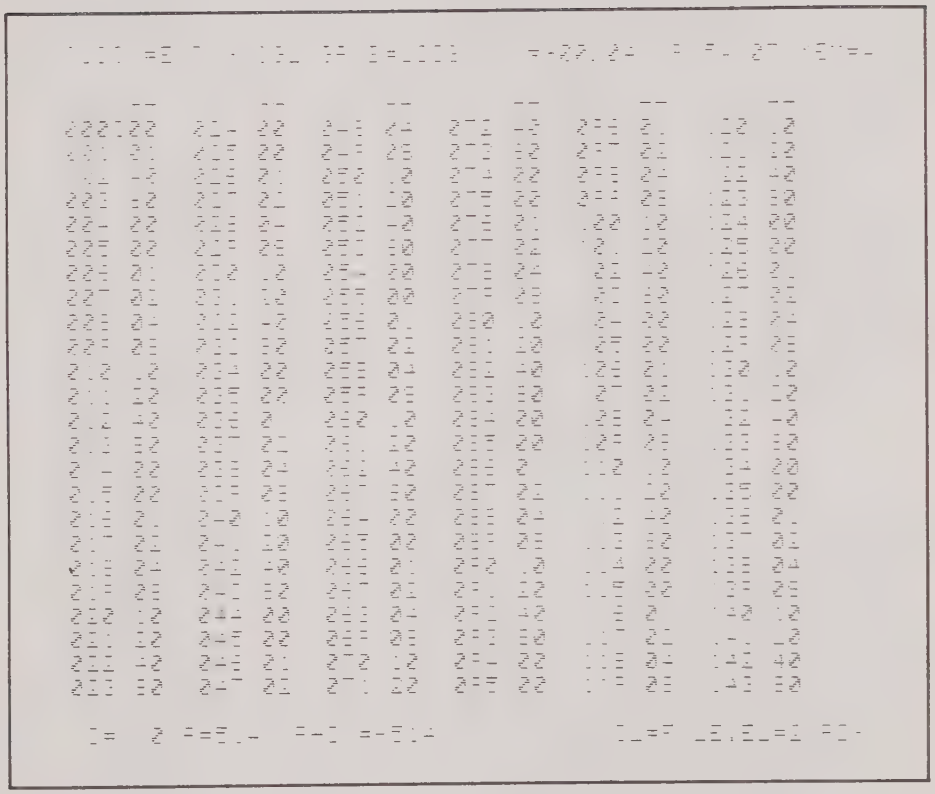

Figure 10-72. Recording of Selected Words.

Press [▷] . Note that CL = F changes to CL = 0; 01 was recorded by trace level 0. Press [▷] again.

Note that CL = 2; the next recorded sample was traced by level 2. Nothing was recorded during level 1. Although 515 samples (1 memoryful) flowed through the analyzer between trace control levels 0 and 2, none of them were stored in memory.

10.2.5.6 Capture a Segment of Samples: Record from Here to There

SET UP: Only a part of one cycle of the Probe Test pattern (the word sequence 01, 02, 04, 08, 10, 20, 40, 80) will be captured. See setup guide in Figure 10-73. Change the trace control program.

Press [TRACE CONTROL], [▽ SET] four times, [Hx1 0 G], [Hx3 1 H], [▽ SET] twice, [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▽ SET] three times, [Hx1 0 G], [▽ SET], [PAGE 8 O TTL], [Hx1 0 G], [▽ SET], [Hx3 1 H], [▽ SET], [Hx6 2 I], [▽ SET], [Hx3 1 H], [▽ SET] four times, [Hx6 2 I].

RECORD: Press [ARM] .

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.3 OF ___ DATE _____

QUICK KEY (3) See back for notes DATA FORMAT MIXED USER SEQN.

RADIX: H H

	MSB	
	I 6	
D	N 5	
A	P 4	
T	U 3	AF AB
A	T 2	AE AA
	S 1	AD A9
	LSB	AC A8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

[illegible]

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(0) TRACE IF DATA = T
T = 0 1

COMMENTS

TRACE CONTROL WAITS FOR 01 TO OCCUR, THEN TRACES IT AND ADVANCES.

LEVEL 1 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 8 0
(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED UP UNTIL 80 OCCURS, THEN TRACE CONTROL ADVANCES.

LEVEL 2 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(2) TRACE NEVER
T = X X

COMMENTS

NO MORE SAMPLES ARE TRACED AND THE RECORDING PROCESS STOPS, SINCE THE DESIRED SEGMENT HAS BEEN RECORDED.

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

QUICK KEY

(___) STOP
S =
(___) JUMP TO ___ (O-F)
J =
(___) ADVANCE
A =
(___) TRACE
T =

COMMENTS

Figure 10-73. Setup Guide: Capture a Segment of Samples: Record from Here to There (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.3

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE - PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - A0 sequence
1	OCTAL Fixed octal format & CF - A0 sequence
2	BINARY Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF - A0 SEQN Any radix fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE 818 attached OR
6	DEVICE NOT AVAILABLE No RTE 818 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	- - - NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	- - - NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock: are Section A - Section B - Section C - internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate Section A Section B Section C & Master external expressions
3	MIXED SINGLE PHASED Master must be external Each section can be sampled at the Master external rate internal clock period or 1/2ns Section A Section B and or Section C - Master external or internal clock period or 1/2ns
4	MIXED MULT PHASED Master must be external Each section can be sampled at own external rate and the Master external rate internal clock period or 1/2ns Section A Section B and or Section C Master external or internal clock period or 1/2ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock are 1/2ns Section A Section B and or Section C internal clock period or 1/2ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A ≤ B WITHIN LIMITS
5	AUTO STOP IF A ≥ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-73. Setup Guide: Capture a Segment of Samples: Record from Here to There (Sheet 2 of 2).

REVIEW: Press [SHIFT], [◁ SET], [5 L], [0 G], [3 J], [DATA], [▷].

The display should look like Figure 10-74. The first word of the pattern segment was captured by level 0 and the following nine by level 1.

Press [▷] to location 511 (see Figure 10-75).

The segment was captured on levels 0 and 1; recording stopped on level 2 (as indicated by LEVEL = 2 RDY).

Press [TIMING] and move the Control Cursor [◁ SET] to verify that only one pattern was recorded.

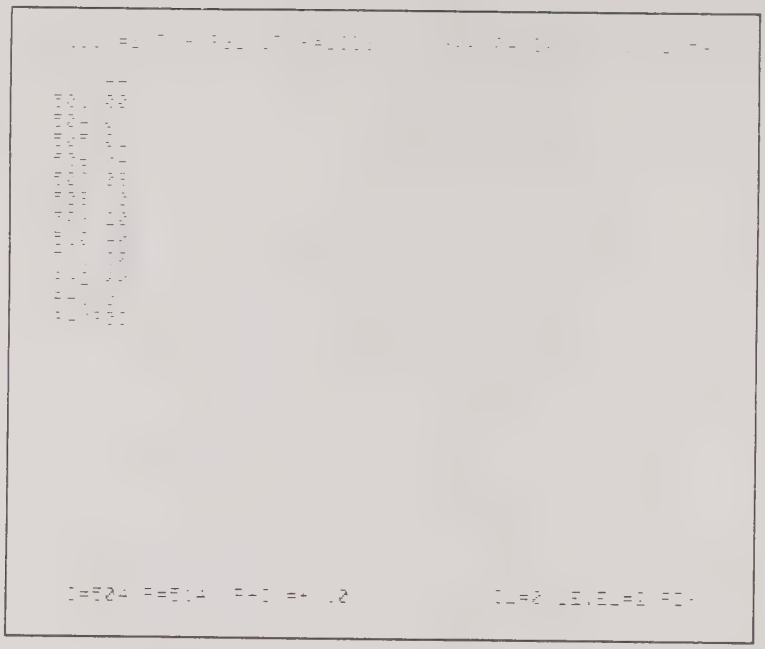

Figure 10-74. First Word (01) Recorded by Level 0.

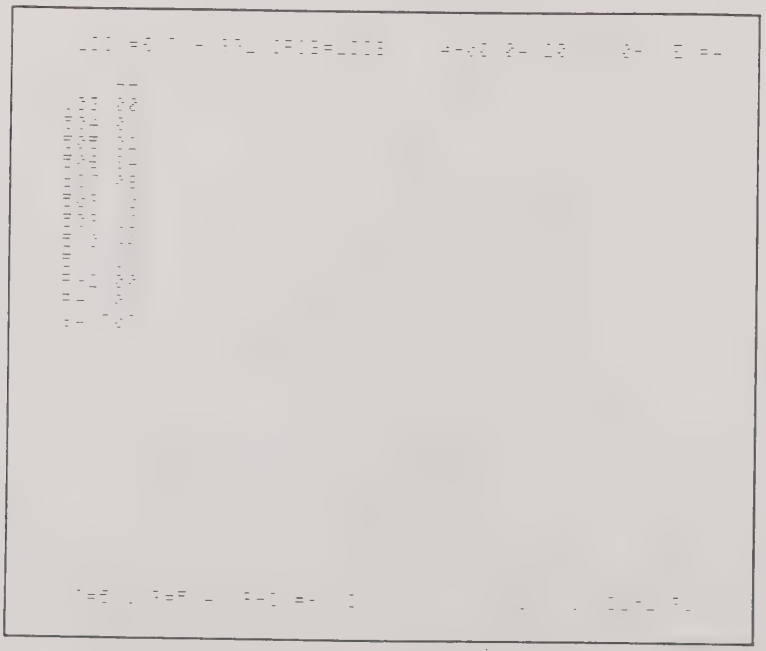

Figure 10-75. Words of Segment Recorded by Level 1.

10.2.5.7 Exclude Recording a Segment of Samples: Don't Record from Here to There

SET UP: To exclude capturing all the words between the first (01) and last (80) words of one cycle of the pattern, see setup guide in Figure 10-76.

Press [TRACE CONTROL], [▽ SET] five times, [Hx3 1 H], [▽ SET],
[Hx3 1 H], [▽ SET] five times, [Hx1 0 G], [▽ SET], [PAGE 8 O TTL],
[Hx1 0 G], [▽ SET], [Hx6 2 I], [▷] twice, [V24 5 L],
[Hx1 0 G], [Hx1 0 G], [▽ SET], [Hx12 3 J], [▽ SET] five
times, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [TIMING].

This display should look like Figure 10-77. The six pulses between the first and last pulse of the pattern were not recorded in memory, although they were sampled into the analyzer. Notice the six missing pulses in the first cycle. They correspond to the excluded data words 02, 04, 08, 10, 20, and 40. Move the Control Cursor to verify the trace level on which each word was recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.4 OF ___ DATE _____

See back for notes: (3) DATA FORMAT MIXED USER SEQN.

TRACE CONTROL NOTES

RADIX: H H

MSB	
6	
DATA 5	
4	
3	AF AB
2	AE AA
1	AD A9
LSB	AC A8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL

LEVEL 0 (QUICK KEY 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(1) TRACE ALWAYS
T = X X

COMMENTS: EVERYTHING IS TRACED UNTIL 01 OCCURS WHEN TRACE CONTROL THEN ADVANCES

LEVEL 1 (QUICK KEY 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 8 0
(0) TRACE IF DATA = T
T = 8 0

COMMENTS: THIS LEVEL WAITS FOR 80 TO OCCUR, TRACING NOTHING UNTIL IT DOES AND THEN ADVANCING.

LEVEL 2 (QUICK KEY 0-F) DELAY = DEC (DEC/HEX) 500 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS: FULL TRACING OF ALL SAMPLES RESUMES FOR 500 MORE CLOCKS.

LEVEL ___ (QUICK KEY 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

(____) STOP
S =
(____) JUMP TO ___ (0-F)
J =
(____) ADVANCE
A =
(____) TRACE
T =

COMMENTS

Figure 10-76. Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.4

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE no RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	-- NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	-- -- -- NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock: are Section A - Section B - Section C - Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external: are Section A - Section B - Section C - Master external
2	EXTERNAL MULT PHASED Each section can be sampled at own external: are or Master external rate: Section A - Section B - Section C, & Master: can be different external expressions
3	MIXED SINGLE PHASED Master must be external: Each section can be sampled at the Master external rate or internal clock period or 10ns: Section A - Section B and or Section C - Master external or internal clock period or 10ns
4	MIXED MULT PHASED Master must be external: Each section can be sampled at own external rate: the Master external rate: internal clock period or 10ns: Section A - Section B - and or Section C - Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock: are or 10ns: Section A - Section B - and or Section C - internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A > B
3	AUTO STOP IF A < B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP B	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	_	_	_	_	_	_	_	_

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-76. Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There (Sheet 2 of 2).

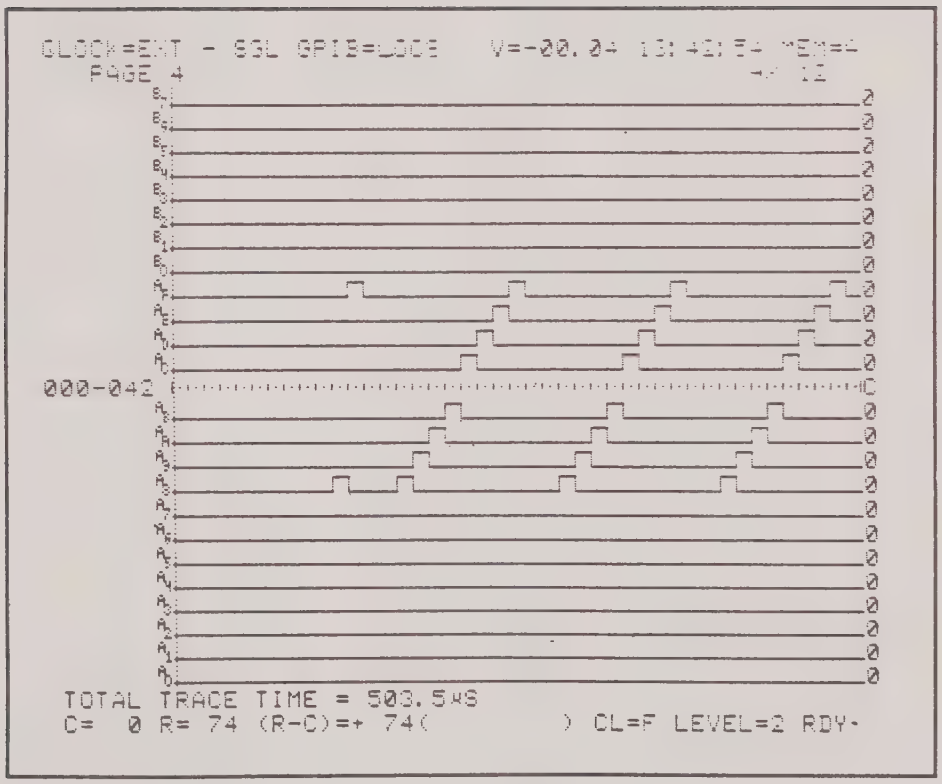

Figure 10-77. Six Pulses Sampled and Not Recorded.

10.2.5.8 Selectively Record Only One Kind of Sample for a Certain Number of Times

SET UP: To record only one memoryful of the word 01, change trace control.

Press [TRACE CONTROL], [▷] three times, [Hx3 1 H], [▽ SET], [V24 5 L], [▽ SET] three times, [Hx6 2 I], [▽ SET] twice, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx12 3 J], [V12 6 M], [DATA].

The display should look like Figure 10-78. Only 01s were recorded. P-2, P-1, and SAM show some of the other sampled words that flowed through the analyzer but did not meet the trace control TRACE conditions.

10.2.5.8 Follow a Path, Then Record

SET UP: Fill memory only after confirming that four words of the pattern occur in their proper sequence: 02, 08, 20, then 80. See setup guide in Figure 10-79.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [Hx6 2 I], [▽ SET], [Hx3 1 H], [▽ SET] four times, [Hx1 0 G], [PAGE 8 O], [▽ SET] twice, [Hx1 0 G], [PAGE 8 O],

```
CLOCK=EXT - SGL GPIB=LOCS    V=-00.04 14:07:07 MEM=4

    HH        HH        HH        HH        HH        HH
376C01    400 01    424 01    448 01    472 01    496 01
377 01    401 01    425 01    449 01    473 01    497 01
378 01    402 01    426 01    450 01    474 01    498 01
379 01    403 01    427 01    451 01    475 01    499 01
380 01    404 01    428 01    452 01    476 01    500 01
381 01    405 01    429 01    453 01    477 01    501 01
382 01    406 01    430 01    454 01    478 01    502 01
383 01    407 01    431 01    455 01    479 01    503 01
384 01    408 01    432 01    456 01    480 01    504 01
385 01    409 01    433 01    457 01    481 01    505 01
386 01    410 01    434 01    458 01    482 01    506 01
387 01    411 01    435 01    459 01    483 01    507 01
388 01    412 01    436 01    460 01    484 01    508 01
389 01    413 01    437 01    461 01    485 01    509 01
390 01    414 01    438 01    462 01    486 01    510 01
391 01    415 01    439 01    463 01    487 01    511 01
392 01    416 01    440 01    464 01    488 01    P-2 02
393 01    417 01    441 01    465 01    489 01    P-1 04
394 01    418 01    442 01    466 01    490 01    SAMR08
395 01    419 01    443 01    467 01    491 01
396 01    420 01    444 01    468 01    492 01
397 01    421 01    445 01    469 01    493 01
398 01    422 01    446 01    470 01    494 01
399 01    423 01    447 01    471 01    495 01

 C=376 R=514 (R-C)=+138(          ) CL=0 LEVEL=0 RDY
```

Figure 10-78. Word 01 Selected to be Recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.6 OF ___ DATE _____

QUICK KEY (3) See back for notes. DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AEAB
A T 2 AEAA
S 1 ADA1
LSB ACA8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

For each level
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
1	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count Delay
4	If DATA = D and Sample Count Delay
5	If DATA = D and Sample Count Delay
6	If DATA = D and Sample Count Delay
7	If DATA = D and Sample Count Delay
8	If DATA = D and Sample Count Delay

O = S, J, A or T which are assigned by command type

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 2
(0) TRACE IF DATA = T
T = 0 2

COMMENTS
WAIT FOR 02, TRACE IT AND ADVANCE.

LEVEL 1 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 8
(0) TRACE IF DATA = T
T = 0 8

COMMENTS
WAIT FOR 08, TRACE IT AND ADVANCE.

LEVEL 2 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 2 0
(0) TRACE IF DATA = T
T = 2 0

COMMENTS
WAIT FOR 20, TRACE IT AND ADVANCE.

LEVEL 3 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 8 0
(0) TRACE IF DATA = T
T = 8 0

COMMENTS
WAIT FOR 80, TRACE IT AND ADVANCE.

Figure 10-79. Setup Guide: Follow a Path, Then Record (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.6 (cont.) OF ___ DATE _____

See back for notes (3) DATA FORMAT MIXED USER SEQN.

RADIX: H_H

MSB
6
5
4
3 AEAB
2 AEAA
1 ADA9
LSB AGAB

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

QUICK KEY LEVEL 4 OF DELAY = DEC 500 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F OF

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY

S = X_X

(2) JUMP TO 0 OF NEVER

J = X_X

(2) ADVANCE NEVER

A = X_X

(1) TRACE ALWAYS

T = X_X

COMMENTS

TRACE ALL THE FOLLOWING 500 SAMPLES AND STOP.

QUICK KEY LEVEL ___ OF DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ OF

(.....) STOP _____

S = _____

(.....) JUMP TO ___ OF _____

J = _____

(.....) ADVANCE _____

A = _____

( ) TRACE _____

T = _____

COMMENTS

QUICK KEY LEVEL ___ OF DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ OF

(.....) STOP _____

S = _____

(.....) JUMP TO ___ OF _____

J = _____

(.....) ADVANCE _____

A = _____

(.....) TRACE _____

T = _____

COMMENTS

QUICK KEY LEVEL ___ OF DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ OF

( ) STOP _____

S = _____

(.....) JUMP TO ___ OF _____

J = _____

(.....) ADVANCE _____

A = _____

(.....) TRACE _____

T = _____

COMMENTS

Figure 10-79. Setup Guide: Follow a Path, Then Record (Sheet 2 of 2).

[▽ SET], [Hx6 2 I], [▽ SET], [Hx6 2 I], [▽ SET] twice,
[Hx1 0 G], [▽ SET], [Hx6 2 I], [Hx1 0 G], [▽ SET], [Hx1 0 G],
[▽ SET], [Hx6 2 I], [Hx1 0 G], [▽ SET], [Hx12 3 J],
[▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET],
[PAGE↑ 8 O TTL], [Hx1 0 G], [▽ SET], [PAGE↓ 4 K], [▷] twice,
[V24 5 L], [Hx1 0 G], [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [TIMING].

The display should look like Figure 10-80. The first four pulses had to occur in their proper sequence before the following pulses could be recorded.

Press [DATA], then press [▷] slowly ten times,

noting the cursor level of each word (see Figure 10-81). The words 02, 08, 20, and 80 were traced on levels 0, 1, 2, and 3, respectively, before the following data could be recorded by level 4.

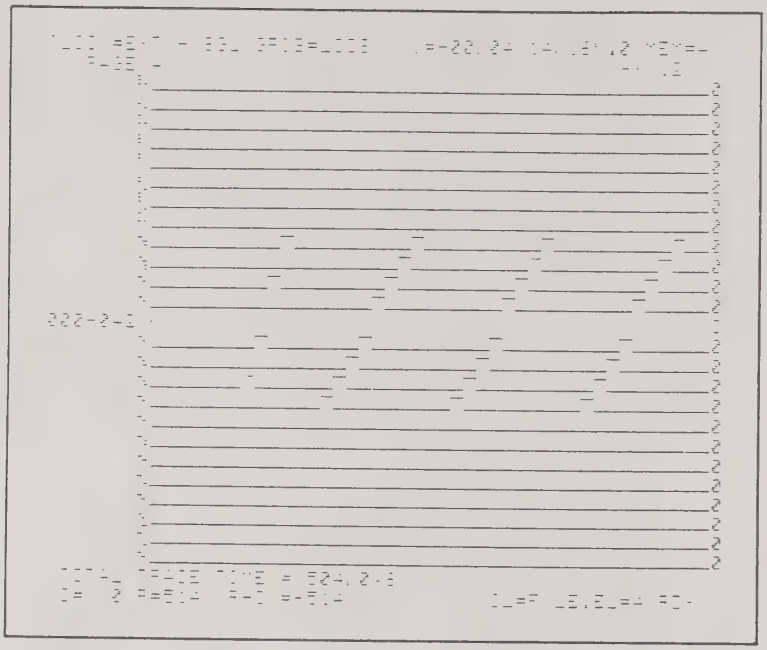

Figure 10-80. Four Pulses Sequence for Recording.

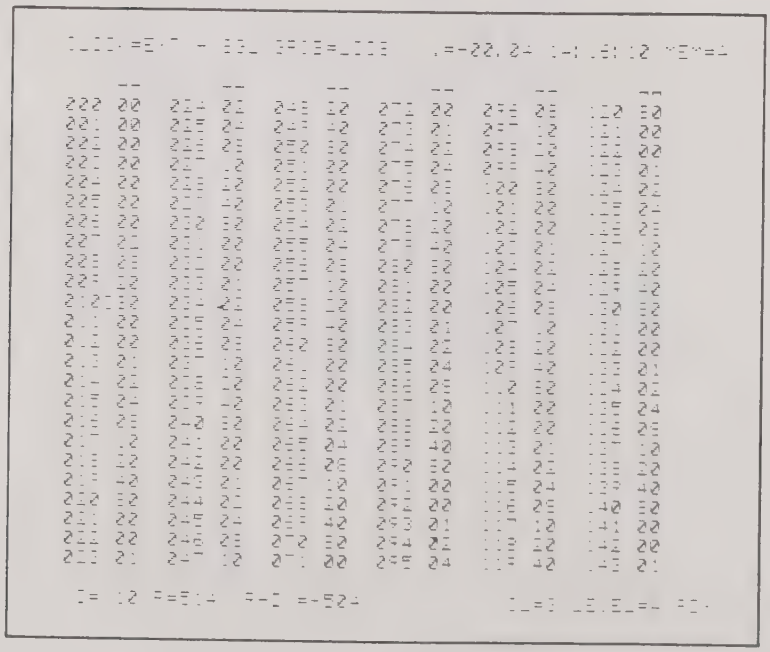

Figure 10-81. Trace on Four Levels Before Recording.

10.2.5.10 **Record, then Follow a Path**

SET UP: After capturing a memoryful of information, confirm that several subsequent words of the pattern occur in their proper sequence, i.e., 08, 20, then 80. See setup guide in Figure 10-82.

Press [TRACE CONTROL], [▷] twice, [V24 5 L], [Hx3 1 H], [V24 5 L], [▷], [Hx1 0 G], [▽ SET] three times, [Hx12 3 J], [▽ SET], [DON'T CARE * SPACE] twice, [▽ SET], [Hx3 1 H], [▽ SET], [Hx12 3 J], [▽ SET], [Hx1 0 G], [▽ SET], [PAGE 8 O TTL], [Hx1 0 G], [▽ SET] twice, [Hx6 2 I].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [PAGE 4 K], [EBCDIC 9 P ECL], [V12 6 M], [DATA].

Press [▷] slowly.

Note the cursor level at each location; this verifies the sequence of events that occurred after the main information was recorded (see Figure 10-83). After the information was recorded, subsequent words were checked to verify that the expected execution path occurred.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.7 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H_H

	MSB	
	6	
DATA	5	
	4	
	3	AE_AB
	2	AE_AA
	1	AD_A9
	LSB	AC_A8

RADIX CHOICES. (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition	
0	if DATA = D	
1	Always	
2	Never	
3	if DATA = D and Sample Count =	Delay
4	if DATA = D and Sample Count >	Delay
5	if DATA = D and Sample Count <	Delay
6	if DATA = D and Sample Count ≠	Delay
7	if DATA ≠ D and Sample Count =	Delay
8	if DATA ≠ D and Sample Count <	Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL 0 (0-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X_X
(2) JUMP TO 0 (0-F) NEVER
J = X_X
(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = X_X
(1) TRACE ALWAYS
T = X_X

COMMENTS: TRACE EVERYTHING FOR 515 SAMPLES THEN ADVANCE.

LEVEL 1 (0-F) DELAY = ___ (DEC/HEX, 0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X_X
(2) JUMP TO 0 (0-F) NEVER
J = X_X
(0) ADVANCE IF DATA = A
A = 0_8
(0) TRACE IF DATA = T
T = 0_8

COMMENTS: WAIT FOR 08, TRACE IT AND ADVANCE.

LEVEL 2 (0-F) DELAY = ___ (DEC/HEX, 0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X_X
(2) JUMP TO 0 (0-F) NEVER
J = X_X
(0) ADVANCE IF DATA = A
A = 2_0
(0) TRACE IF DATA = T
T = 2_0

COMMENTS: WAIT FOR 20, TRACE IT AND ADVANCE.

LEVEL 3 (0-F) DELAY = ___ (DEC/HEX, 0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(0) STOP IF DATA = S
S = 8_0
(2) JUMP TO 0 (0-F) NEVER
J = X_X
(2) ADVANCE NEVER
A = X_X
(0) TRACE IF DATA = T
T = 8_0

COMMENTS: WAIT FOR 80, TRACE IT AND STOP RECORDING

Figure 10-82. Setup Guide: Record, Then Follow a Path (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.7

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal formats & CF A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF-A0 SEQN Any radix fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 816 attached
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE ↓ ACTIVE FALLING EDGE
2	– – – NOT USED

QUICK KEY	CLOCK CHOICES
0	↑ POSITIVE TRUE ↓ NEGATIVE TRUE
2	– – – NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate Section A Section B Section C & Master or can be different external expressions
3	MIXED SINGLE PHASED Master must be external Each section can be sampled at the Master external rate internal clock period or 10ns Section A Section B and/or Section C - Master/ext external or internal clock period or 10ns
4	MIXED MULT PHASED Master must be external Each section can be sampled at own external rate the Master external rate internal clock period or 10ns Section A Section B and or Section C - Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns Section A Section B and or Section C internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ___ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
	NEGATIVE

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Figure 10-82. Setup Guide: Record, Then Follow a Path (Sheet 2 of 2).

```
CLOCK=EXT - SGL GPIB=LOCS    .=-00.04 20:41:36 MEM=-

     HH
496 08
497 10
498 20
499 40
500 80
501 00
502 00
503 01
504 02
505 04
506 08
507 10
508 20
509C08
510 20
511 30
P-2 00
P-1 00
SAMR01



 C=509 R=514 (R-C)=+  5(          ) CL=1 LE.EL=3 RDY
```

Figure 10-83. Verify Expected Execution Path.

10.2.5.11 **Check for Event 1 or Event 2**

SET UP: The place in the pattern cycle where the analyzer will begin sampling will vary with each recording. For example, if the first word sampled is 01, the next will be 02, the next 04, and so on; if the first word is 10, the next will be 20, the next 40, and so on. Therefore, one cannot predict whether 01 will appear before 10 or vice versa. The trace control program will end on level 1 if 10 occurs first and level 8 if 01 occurs first, thereby indicating exactly which happened when (see setup guide in Figure 10-84).

Press [TRACE CONTROL], [▽ SET] twice, [PAGE 8 O TTL], [▷], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx1 0 G], [▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET] twice, [Hx3 1 H], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 H], [▽ SET], [PAGE 8 O TTL], [▽ SET], [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Observe the trace level status field. It indicates which path was taken and therefore, which word occurred first. LEVEL = 1 RDY means 10 happened first. LEVEL = 8 RDY means 01 happened first.

Press [DATA] to verify.

Press [ARM] several times to see the varying end levels.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.8A OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
6	
D N 5	
A P 4	
T U 3	AE AB
A T 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level –
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition	
0	If DATA = D	
1	Always	
2	Never	
3	If DATA = D and Sample Count =	Delay
4	If DATA = D and Sample Count >	Delay
5	If DATA = D and Sample Count <	Delay
6	If DATA = D and Sample Count ≠	Delay
7	If DATA ≠ D and Sample Count =	Delay
8	If DATA ≠ D and Sample Count	Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(0) JUMP TO 8 (0-F) IF DATA = J
J = 0 1
(0) ADVANCE IF DATA = A
A = 1 0
(1) TRACE ALWAYS
T = X X

COMMENTS
TRACE EVERYTHING WHILE LOOKING FOR 10 OR 01. IF 01 OCCURS 1st, GO TO LEVEL 8. OTHERWISE GO TO LEVEL 1.

LEVEL 1 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
THIS LEVEL IS ONLY ENTERED IF 10 OCCURED BEFORE 01. IT TRACES ONE SAMPLE AND STOPS.

LEVEL 8 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
THIS LEVEL IS ONLY ENTERED IF 01 OCCURED BEFORE 10. IT TRACES ONE SAMPLE AND STOPS.

LEVEL ____ (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ____ (0-F)

(.....) STOP
S =
(.....) JUMP TO ____ (0-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

Figure 10-84. Setup Guide: Check for Event 1 or Event 2 (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.8A

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF - A0 sequence
1	OCTAL — Fixed octal format & CF - A0 sequence
2	BINARY — Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN — Any radix any sequence
4	MIXED CF - A0 SEQN — Any radix fixed CF - A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACT.VE FALLING EDGE
2	— — — NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	— — — NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate
Section A - Section B - Section C - internal clock period

EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate
Section A - Section B - Section C - Master external

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master external can be different external expressions

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C - Master external or internal clock period or 10ns

4 MIXED MULT. PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C - Master external or internal or 10ns

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C - Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-84. Setup Guide: Check for Event 1 or Event 2 (Sheet 2 of 2).

10.2.5.12 **Take the Same Path Regardless of Which Event Occurred**

SET UP: As in paragraph 10.2.5.11, either 10 or 01 may be sampled first. Regardless, trace control goes to level 1 and stops. See setup guide in Figure 10-85.

Press [TRACE CONTROL], [▽ SET] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [Hx12 3 J], [DATA], [▷] seven times.

Your display should look like either Figure 10-86 or 10-87.

Press [ARM] repeatedly and observe the word in location 510. It may be 01 or 10, but tracing always stops at level 1.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.88 OF ___ DATE _____

QUICK KEY (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB 6 5 4 3 2 1 LSB

DATA: AEAB AEAA ADA9 ACAB

RADIX CHOICES (B) BINARY (O) OCTAL, (H) HEX, (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

LEVEL 0 DELAY = ___ ___ ___ END LEVEL F

QUICK KEY (2) STOP NEVER

S = X X

(0) JUMP TO 1 IF DATA = J

J = 0 1

(0) ADVANCE IF DATA = A

A = 1 0

(1) TRACE ALWAYS

T = X X

COMMENTS

EVERYTHING IS TRACED WHILE LOOKING FOR EVENT 01 OR 10 TO OCCUR. REGARDLESS OF WHICH HAPPENS 1st, GO TO LEVEL 1.

LEVEL 1 DELAY = ___ ___ ___ END LEVEL F

QUICK KEY (1) STOP ALWAYS

S = X X

(2) JUMP TO 0 NEVER

J = X X

(2) ADVANCE NEVER

A = X X

(1) TRACE ALWAYS

T = X X

COMMENTS

TRACE ONE SAMPLE AND STOP.

LEVEL ___ DELAY = ___ ___ ___ END LEVEL ___

QUICK KEY (.....) STOP

S =

(.....) JUMP TO ___

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

COMMENTS

LEVEL ___ DELAY = ___ ___ ___ END LEVEL ___

QUICK KEY (.....) STOP

S =

(.....) JUMP TO ___

J =

(.....) ADVANCE

A =

( ) TRACE

T =

COMMENTS

Figure 10-85. Setup Guide: Take the Same Path Regardless of Which Event Occurred (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.8B

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C =
- INT: ☐ SAME AS MASTER; ☐ 10 NANOSECONDS
- EXT: ☐ SAME AS MASTER; ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B =
- INT: ☐ SAME AS MASTER; ☐ 10 NANOSECONDS
- EXT: ☐ SAME AS MASTER; ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A =
- INT: ☐ SAME AS MASTER; ☐ 10 NANOSECONDS
- EXT: ■ SAME AS MASTER; ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF AO sequence
1	OCTAL Fixed octal format & CF AO sequence
2	BINARY Fixed binary format & CF AO sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF AO SEQN Any radix fixed CF AO sequence
5	DEVICE MNEMONICS Fixed disassembled uP code format only if RTE 816 attached
6	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	– NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
1	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	– NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A – Section B – Section C – Internal clock period
	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A – Section B – Section C – Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master can be internal external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external, internal clock period or 0ns. Section A, Section B and or Section C – Master external or internal clock period or 0ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate. The Master external rate, internal clock period or 0ns. Section A, Section B and or Section C Master external or internal or 0ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 0ns. Section A, Section B and or Section C internal clock period or 0ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A ≠ B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A ≠ B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

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Figure 10-85. Setup Guide: Take the Same Path Regardless of Which Event Occurred (Sheet 2 of 2).

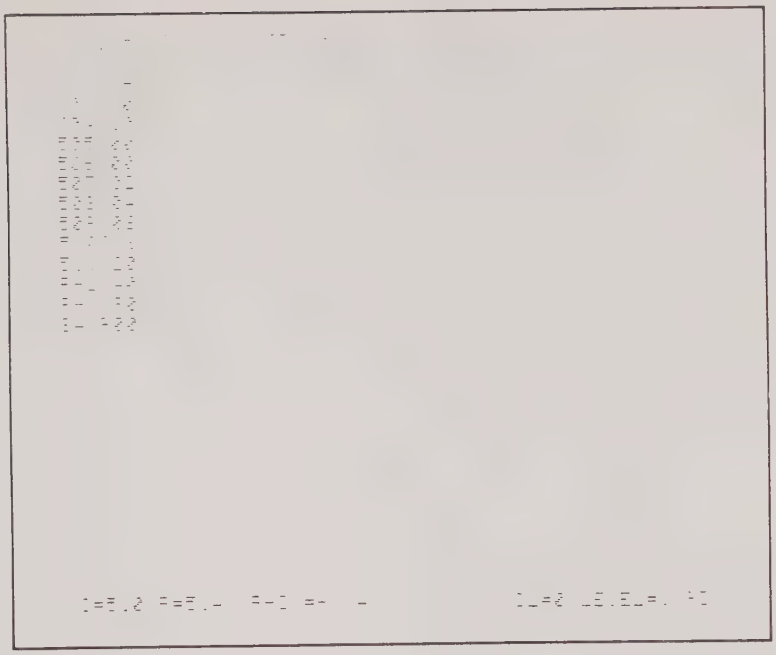

Figure 10-86. Sometimes 10 will occur on level 0.

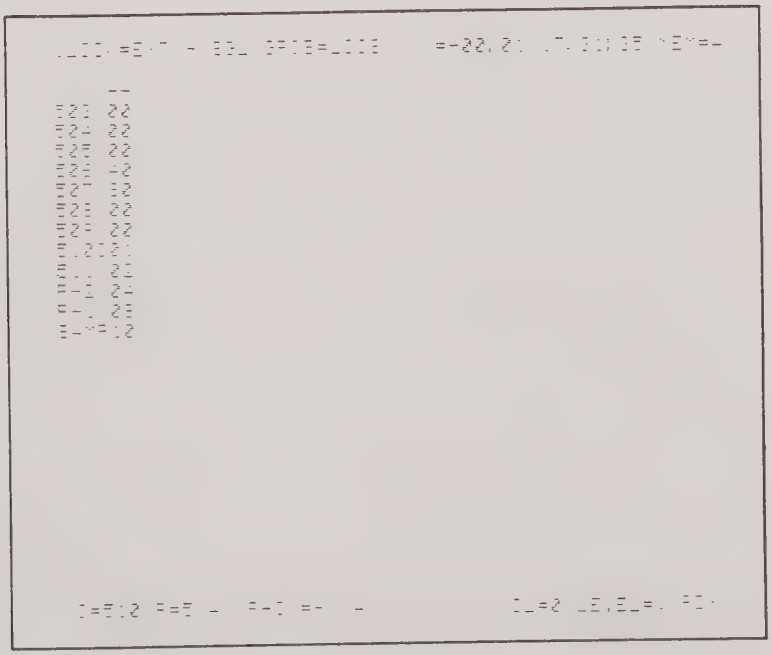

Figure 10-87. Sometimes 01 will occur on level 0.

10.2.5.13 **Check for Correct Timing Between Two Events**

SET UP: According to the Probe Test pattern there should be exactly four samples, or "ticks" of the master sample clock, between words 01 and 10. See setup guide in Figure 10-88 to verify this time interval.

Press [TRACE CONTROL], [▽ SET] twice, [▷], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [Hx3 1 H], [▽ SET] twice, [Hx3 1 H], [▷] twice, [Hx12 3 J], [▽ SET], [Hx6 2 I], [▽ SET], [PAGE 8 O], [▷], [V6 7 N], [▽ SET], [Hx3 1 H], [TTL Hx1 0 G], [▽ SET], [Hx12 3 J], [▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET] twice, [Hx6 2 I], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Note that in the status field, tracing stopped at level 2 (2 RDY), indicating the time interval was correct (four or more sample clock pulses apart). There is no way to vary the actual time between the pulses; to simulate an incorrect time interval, change the delay on level 1 to four clocks.

Press [TRACE CONTROL], [Hx3 1 H], [▷] twice, [PAGE 4 K], [ARM].

Now notice that tracing stopped on level 8 because 10 came true at SAMPLE COUNT = 4 CLOCKS and therefore satisfied the JUMP condition of level 1.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.9 OF ___ DATE _____

See back for notes (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB		
	6	
D	N 5	
A	P 4	
T	U 3	AFAB
A	T 2	AEAA
	S 1	ADA9
LSB		ACA8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

For each line
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four main commands in each line can come up on any one of 8 binary
Any 4 Any commands in a group

(DATA D
Always
Never
(DATA D and Sample Count Delay
(DATA D and Sample Count Delay
(DATA D and Sample Count Delay
(DATA = D and Sample Count Delay
(DATA < D and Sample Count Delay
(DATA > D and Sample Count Delay

Bits 5, 4, 3, 2, 1 are which bits assigned to ... up

TRACE CONTROL

LEVEL 0 (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

QUICK KEY

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE EVERYTHING WHILE LOOKING FOR 01. ADVANCE WHEN IT IS FOUND.

LEVEL 1 (0-F) DELAY = DEC 3 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

QUICK KEY

(2) STOP NEVER
S = X X

(7) JUMP TO 8 (0-F) IF DATA = J AND SAMPLE COUNT < = DELAY
J = 1 0

(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = 1 0

(1) TRACE ALWAYS
T = X X

COMMENTS

EVENT 10 SHOULD OCCUR EXACTLY 4 CLOCKS AFTER ENTERING LEVEL 1 AND TRACE CONTROL THEREFORE ADVANCES TO LEVEL 2.

LEVEL 2 (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

QUICK KEY

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

IF THE TIME BETWEEN 01 AND 10 WAS CORRECT, TRACING ADVANCES TO HERE AND STOPS.

LEVEL 8 (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

QUICK KEY

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

IF THE TIME BETWEEN 01 AND 10 WAS INCORRECT TRACE CONTROL JUMPS TO HERE AND STOPS.

Figure 10-88. Setup Guide: Check Correct Timing Between Two Events (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.9

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled uP code format, only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	— — — NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	— — — NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A = Section B = Section C = internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C = Master external or internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C = Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C = internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-88. Setup Guide: Check Correct Timing Between Two Events (Sheet 2 of 2).

10.2.5.14 **Continuously Monitor for Correct Operation**

a. Word 02

SET UP: To repeatedly check that word 02 occurs immediately after word 01, see setup guide in Figure 10-89.

Press [TRACE CONTROL], [▽ SET], [2 Hx6 I], [▽ SET] twice, [0 Hx1 G], [▽ SET] twice, [0 Hx1 G], [▽ SET], [0 Hx1 G], [1 Hx3 H], [▽ SET], [1 Hx3 H], [▽ SET] twice, [0 Hx1 G], [▷], [0 Hx1 G], [▽ SET], [0 Hx1 G], [2 Hx6 I], [▽ SET], [0 Hx1 G], [▽ SET], [* DON T CARE SPACE] twice.

RECORD: Press [ARM].

REVIEW: Watch the trace level status field; it should alternate between 0 BUSY and 1 BUSY (the changing of the 0 and 1 may be difficult to detect). If and when an error occurs, it will go to 2 RDY. When it does,

Press [SHIFT], [◁ SET], [5 V24 L], [0 Hx1 G], [0 Hx1 G], [DATA].

See Figure 10-90 for an example. In Figure 10-90 the word 02 should have occurred after word 01. Since it did not, tracing was halted. (The exact erroneous word will vary for each machine and recording, as well as the amount of elapsed time before an error occurs.)

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.10(1) OF ___ DATE _____

See back for notes! (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
6	
DATA 5	
4	
3	AF AB
2	AE AA
1	AD A9
LSB	AC A8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII (I) (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

LEVEL 0 (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS: WAIT FOR 01 - TRACE IT AND ADVANCE.

LEVEL 1 (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X

(0) JUMP TO 0 (0-F) IF DATA = J
J = X X

(0) ADVANCE IF DATA = A
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS: EVENT 02 SHOULD OCCUR IMMEDIATELY UPON ENTERING LEVEL 1. IF SO, JUMP BACK. IF NOT, ADVANCE. TRACE THE EVENT THAT DOES OCCUR.

LEVEL 2 (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (0-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS: TRACE CONTROL COMES HERE AND STOPS ONLY IF 02 DID NOT OCCUR RIGHT AFTER 01.

LEVEL ___ (0-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)

( ) STOP
S =

( ) JUMP TO ___ (0-F)
J =

( ) ADVANCE
A =

( ) TRACE
T =

COMMENTS

Figure 10-89. Setup Guide:Continuously Monitor for Correct Operation (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.10 (1)

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1.) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - A0 sequence
1	OCTAL Fixed octal format & CF - A0 sequence
2	BINARY Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF - A0 SEQN Any radix fixed CF - A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate Section A Section B Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external Each section can be sampled at the Master external rate Internal clock period or 1 One Section A Section B and/or Section C - Master (external) or Internal clock period or 1 One
4	MIXED MULTI PHASED Master must be external Each section can be sampled at own external rate the Master external rate Internal clock period or 1 One Section A Section B and/or Section C - Master (external) or Internal or 1 One
5	INTERNAL EXTENDED Each section can be sampled at the Internal clock rate or 1 One Section A Section B and/or Section C - Internal clock period or 1 One

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0.) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP B	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP A	±	±	±	±	±	±	±	±	_	_	_	_	_	_	_	_

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-89. Setup Guide:Continuously Monitor for Correct Operation (Sheet 2 of 2).

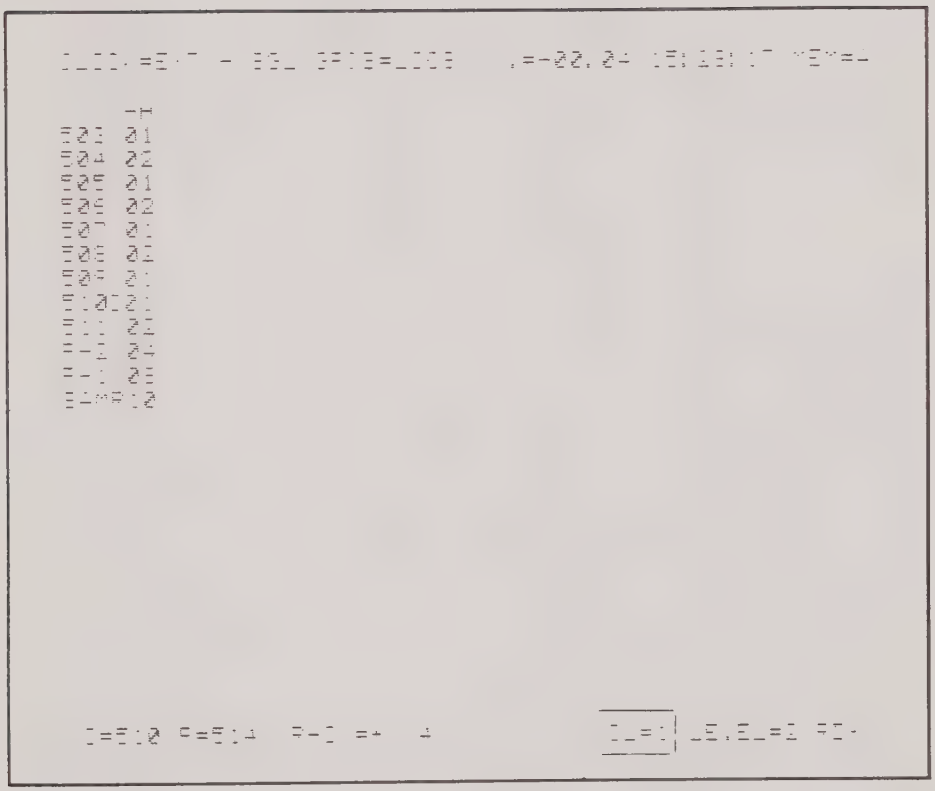

Figure 10-90. Tracing Halted.

b. Word 80

SET UP: To repeatedly check that word 80 occurs within the proper time interval (seven clocks) from the occurrence of 01, see setup guide in Figure 10-91.

Press [TRACE CONTROL], [Hx3 1 H], [▷] twice, [V6 7 N], [▽ SET] twice, [Hx1 0 G], [▷], [V6 7 N], [▽ SET], [PAGE 8 O TTL], [Hx1 0 G], [▽ SET], [Hx12 3 J].

RECORD: Press [ARM].

REVIEW: Watch the trace level status field. Again, it should toggle between 0 BUSY and 1 BUSY. If and when an error occurs, it will go to 2 RDY.

Press [DATA] to see the cause of the error, as in Figure 10-92. Because an extra sample (40) occurred between 01 and 80, the time interval between them was in error and tracing stopped.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.10 (2) OF ___ DATE _____

See back for notes (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB 6 5 4 3 2 1 LSB

AFAB
AEAA
ADA9
ACA8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

LEVEL 0 (QUICK KEY, O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(0) TRACE IF DATA = T
T = 0 1

COMMENTS
WAIT FOR 01, TRACE IT AND ADVANCE WHEN IT OCCURS.

LEVEL 1 (QUICK KEY, O-F) DELAY = DEC 7 (DEC/HEX) ___ (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(7) JUMP TO 0 (O-F) IF DATA = J AND SAMPLE COUNT < = DELAY
J = 8 0
(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
EVENT 80 SHOULD OCCUR EXACTLY 7 CLOCKS AFTER EVENT 01. IF SO, JUMP BACK. IF NOT, ADVANCE, TRACE EVERYTHING THAT HAPPENS BETWEEN 01 AND 80.

LEVEL 2 (QUICK KEY, O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
IF THIS LEVEL IS REACHED, A TIMING ERROR OCCURED.

STOP.

LEVEL ___ (QUICK KEY, O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =
(.....) JUMP TO ___ (O-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

Figure 10-91. Setup Guide: Repeatedly Check Word 80 (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.10(2)

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - A0 sequence
1	OCTAL Fixed octal format & CF - A0 sequence
2	BINARY Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN Any rate any sequence
4	MIXED CF A0 SEQN Any rate fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 818 attached OR
5	DEVICE NOT AVAILABLE No RTE 818 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE ↓ ACTIVE FALLING EDGE
2	– – – – NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE ↓ NEGATIVE TRUE
2	– – – – NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - Internal clock EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B and/or Section C - Master external or internal clock period or 10ns
4	MIXED MULT PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B and/or Section C - Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C - internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
	NEGATIVE

DWS24-12.5183

Figure 10-91. Setup Guide: Repeatedly Check Word 80 (Sheet 2 of 2).

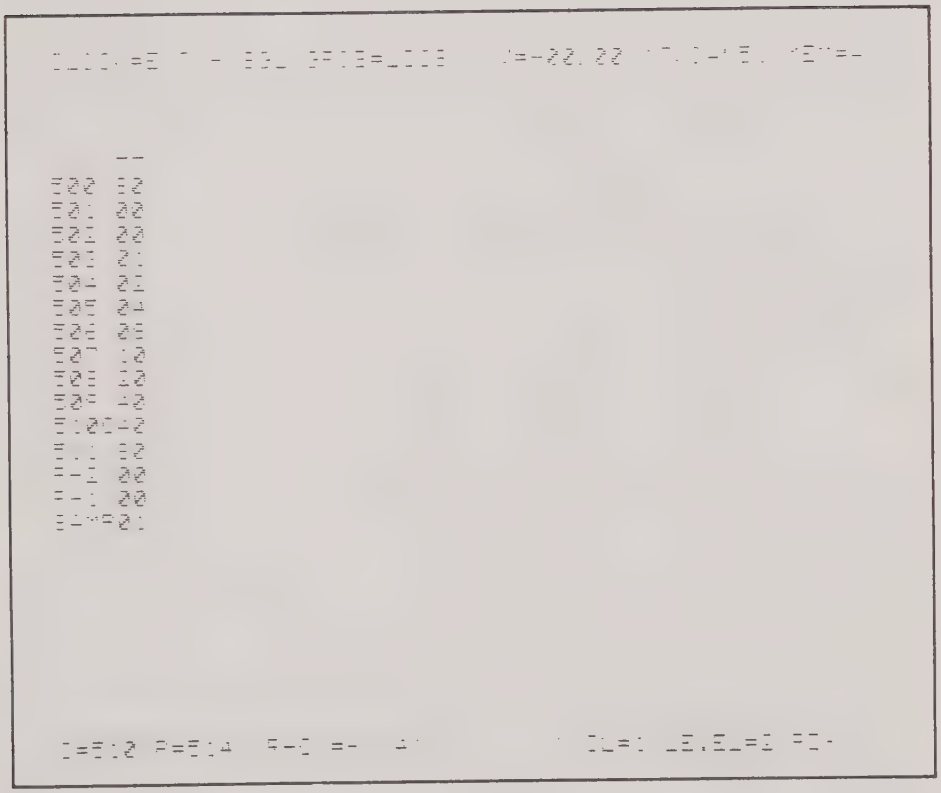

Figure 10-92. Time Interval Error, Tracing Stopped.

10.2.6 ADVANCED TRACE CONTROL

Combining and varying the basic building blocks let you create more complex and powerful trace control programs. The following examples will illustrate some of the more advanced trace control capabilities.

10.2.6.1 **Continuously Check Execution Path and Timing**

SET UP: To check that certain words occur in their expected sequence as well as within their expected time interval, see setup guide in Figure 10-93.

Press [TRACE CONTROL], [Hx3 1 H], [▷] twice, [Hx3 1 H] twice,
[▽ SET] twice, [▷], [Hx6 2 I], [▽ SET], [V24 5 L],
[▽ SET], [Hx1 0 G], [Hx6 2 I], [▽ SET], [V24 5 L], [▽ SET],
[Hx1 0 G], [Hx6 2 I], [▽ SET], [Hx6 2 I], [▷] twice,
[Hx6 2 I], [Hx3 1 H], [▽ SET], [Hx6 2 I], [▽ SET] twice,
[V24 5 L], [▽ SET], [Hx1 0 G], [PAGE 4 K], [▽ SET], [V24 5 L],
[▽ SET], [Hx1 0 G], [PAGE 4 K], [▽ SET], [Hx12 3 J], [▷]
twice, [Hx3 1 H], [▽ SET], [Hx6 2 I], [▽ SET] twice, [V24 5 L],
[▽ SET], [Hx1 0 G], [PAGE 8 TTL], [▽ SET], [V24 5 L], [▽ SET],
[Hx1 0 G], [PAGE 8 TTL], [▽ SET], [PAGE 4 K], [▷] twice,
[Hx3 1 H], [▽ SET], [Hx6 2 I], [▽ SET], [▷], [V24 5 L],

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.2.1 OF ___ DATE _____

QUICK KEY (See back for notes) ( ) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB

DATA 6

DATA 5

DATA 4

DATA 3 AF AB

DATA 2 AE AA

DATA 1 AD A9

LSB AC A8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(2) STOP NEVER

S = X X

(2) JUMP TO ___ (O-F) NEVER

J = X X

(0) ADVANCE IF DATA = A

A = 0 1

(0) TRACE IF DATA = T

T = 0 1

COMMENTS

BEGIN AT KNOWN STARTING POINT.

LEVEL 1 (O-F) DELAY = DEC (DEC/HEX) 11 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(2) STOP NEVER

S = X X

(2) JUMP TO 0 (O-F) NEVER

J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY

A = 0 2

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY

T = 0 2

COMMENTS

02 SHOULD OCCUR 1 CYCLE AND 1 WORD LATER.

LEVEL 2 (O-F) DELAY = DEC (DEC/HEX) 21 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(2) STOP NEVER

S = X X

(2) JUMP TO 0 (O-F) NEVER

J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY

A = 0 4

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY

T = 0 4

COMMENTS

04 SHOULD OCCUR 2 CYCLES AND 1 WORD LATER.

LEVEL 3 (O-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY

(2) STOP NEVER

S = X X

(2) JUMP TO 0 (O-F) NEVER

J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY

A = 0 8

(5) TRACE IF DATA = A AND SAMPLE COUNT = DELAY

T = 0 8

COMMENTS

08 IS NEXT IMMEDIATE WORD.

Figure 10-93. Setup Guide: Continuously Check Execution Path and Timing (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.2 (CONTINUED) OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AFAB
A T 2 AEAA
S 1 ADA9
LSB ACAB

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count = Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count = Delay
7	If DATA = D and Sample Count = Delay
8	If DATA = D and Sample Count = Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

QUICK KEY LEVEL 4 (O-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(5) JUMP TO 0 (O-F) IF DATA = J AND SAMPLE COUNT = DELAY
J = 1 0
(5) ADVANCE IF DATA = J AND SAMPLE COUNT = DELAY
A = X X
(0) TRACE IF DATA = T
T = 1 0

COMMENTS

BOTH JUMP AND ADVANCE ARE TRUE SIMULTANEOUSLY, BUT JUMP HAPPENS 1st, SO IT CONTINUOUSLY LOOPS BETWEEN LINK 0, 1, 2, 3, 4.

QUICK KEY LEVEL 5 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS

THIS LEVEL SHOULD NEVER BE REACHED.

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =
(.....) JUMP TO ___ (O-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =
(.....) JUMP TO ___ (O-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

Figure 10-93. Setup Guide: Continuously Check Execution Path and Timing (Sheet 2 of 2).

[▽] SET, [1] H, [0] G, [▽] SET, [5] L, [▽] SET

twice, [0] G, [▽] SET, [1] H, [0] G.

RECORD: Press [ARM].

REVIEW: Watch the trace level status field continuously sequence through LEVEL = 0, 1, 2, 3, 4 BUSY as the conditions on each level are satisfied and the commands executed.

Note

If an error occurs in the generation or clocking of the Probe Test pattern, the trace program will get hung up (as indicated by a steady LEVEL = n BUSY) because the expected word on that level did not happen when it should have.

Press [M→A].

The recording will most likely stop on level 2 since more time is spent in that level than the others.

Press [SHIFT], [◁] SET, [5] L, [0] G, [0] G, [DATA].

Your display should look like Figure 10-94. The trace program repeatedly captures only one word on each of five levels until manually stopped.

```
CLOCK=EXT - SGL SFIB=LOCS    v=-00.04 15:15:24 MEM=A


     HH
500C01
501 02
502 04
503 08
504 10
505 01
506 02
507 04
508 08
509 10
510 01
511 02
P-2 00
P-1 01
SAMR02


C=500 R=514 (R-C)=+ 14(         ) CL=0 LEVEL=2 RDY
```

Figure 10-94. Capture One Word on Each Level until Stopped.

Press [▷] slowly and

notice that 01 is captured by level 0; one cycle (ten sample clocks) and one sample later 02 is captured by level 1; two cycles and one sample later 04 is captured by level 2; one sample later 08 is captured by level 3; one sample later 10 is captured by level 4; then the whole process repeats. Figure 10-95 shows the exact words that were traced by this program out of all the words that were sampled. Note that of all the samples being evaluated by trace control, only certain samples will be transferred into memory.

10.2.6.2 **Trace Independently of the Execution Path**

SET UP: Change the trace control setup on level 2.

Press [TRACE CONTROL], [Hx6 2 I], [▽ SET] five times, [Hx1 0 G],

[▽ SET], [PAGE↑ 8 O TTL], [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [M→A], [SHIFT], [◁ SET], [PAGE↓ 4 K], [EBCDIC 9 P ECL],

[Hx3 1 H], [DATA].

Your display will look similar to Figure 10-96. Taking the same execution path as before, different samples are selected to be recorded.

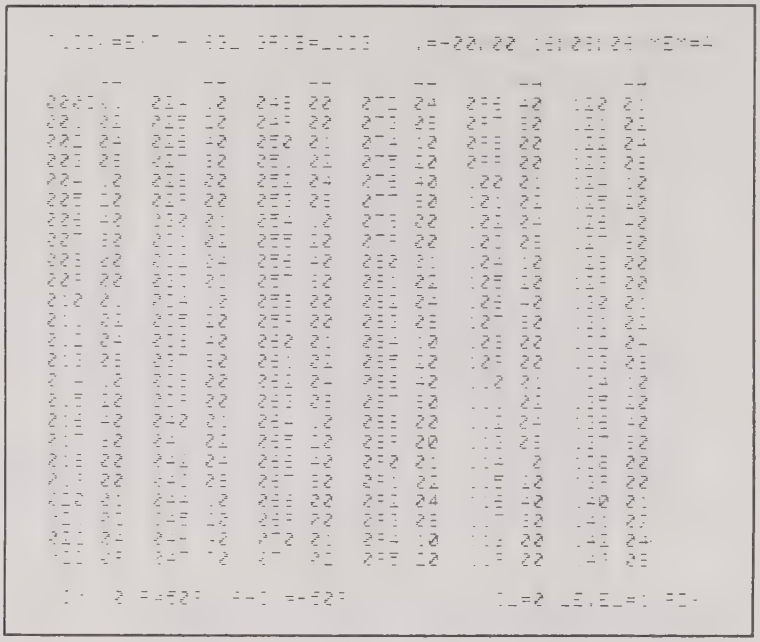

Figure 10-95. Transfer Certain Samples into Memory.

Figure 10-96. Changing Sample Selection.

Press [▷] until CL = 2.

Level 2 still checks for and advances on the second occurrence of 04, but it now traces the two occurrences of 80 that happen while waiting for ADVANCE to come true (see Figure 10-97). While waiting for the level 2 ADVANCE condition to come true, two occurrences of 80 are traced. The TRACE command and its T word recognizer do not have to be the same as any of the other commands and their word recognizers. The words you choose to record don't have to be the same as the words that define the execution path to be followed.

10.2.6.3 **End Level Breakpoint**

SET UP: Change the trace control program end level to 3.

Press [TRACE CONTROL], [◁] SET, [Hx12 3] ↵.

Press [▷], then [CHOICE NEXT] repeatedly to verify that the end level you set applies to all 16 levels.

RECORD: Press [ARM].

REVIEW: Press [DATA], and use [▷] to move the Control Cursor to location 511 (Figure 10-98). Note that though the last sample traced occurred in level 3, end level 3 forces an advance to level 4 and stops the recording there.

Note that the last word was traced by level 3 (CL = 3) and the recording stopped on level 4 (LEVEL = 4 RDY), although none of the level 4 commands were performed. Setting end level to n (where n is a level used in the current program) causes trace control to advance to level

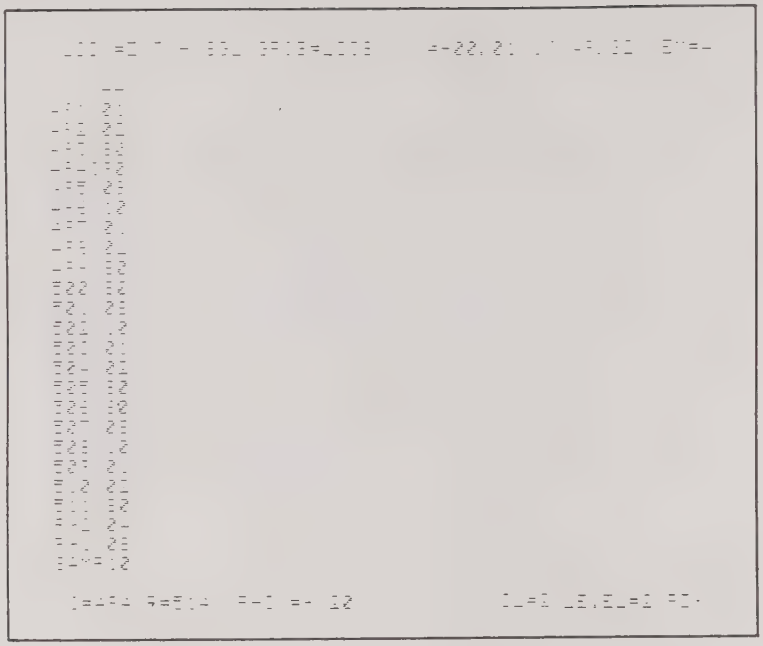

Figure 10-97. Record While Waiting.

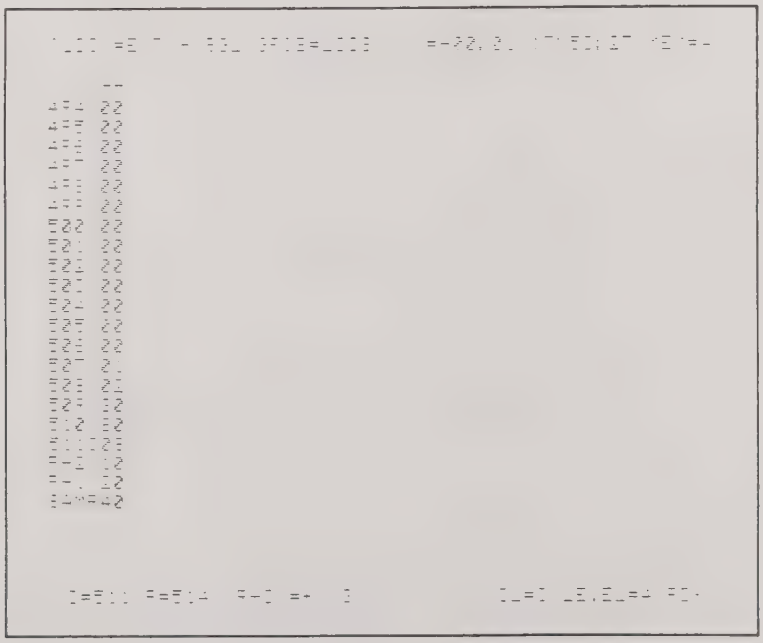

Figure 10-98. End Level 3 Forces.

n + 1, regardless of the commands on level n, and stop on level n + 1 without performing any of the commands on n + 1. In this way, end level can be used as a breakpoint to check out segments of your trace control program.

10.2.6.4 **Segments, Patterns, and Total Trace Time**

SET UP: See setup guide in Figure 10-99.

Press [TRACE CONTROL], [Hx3 1 H], [▷] twice, [V12 6 M], [V24 5 L],
[Hx1 0 G], [Hx1 0 G], [Hx1 0 G], [▷], [Hx3 1 H], [▷],
[DEMUX F V], [▷], [Hx6 2 I], [▷] twice, [Hx3 1 H],
[HEX Hx1 0 G], [Hx3 1 H], [▽ SET] five times, [Hx6 2 I], [▽ SET],
[Hx12 3 J], [▽ SET], [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Notice that the trace level status word remains at 1 BUSY for a moment before going to 3 RDY.

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [V24 5 L],
[Hx3 1 H], [▷] six times.

Your display should look like Figure 10-100.

Press [TIMING] and note the total trace time of 2 microseconds. This is because trace control was only enabled to record one word on levels 0, 1, and 2. Change trace control to trace every occurrence of the level 2 A pattern.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.24 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
6	
D N 5	
A P 4	
T U 3	AFA8
A T 2	AEAA
S 1	ADA9
LSB	ACA0

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX. (A) ASCII. or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA ≠ D and Sample Count = Delay
5	If DATA = D and Sample Count ≠ Delay
6	If DATA ≠ D and Sample Count ≠ Delay
7	If DATA = D and Sample Count ≠ Delay
8	If DATA ≠ D and Sample Count = Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (QUICK KEY; 0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(0) TRACE IF DATA = T
T = 0 1

COMMENTS

WAIT FOR 01, TRACE IT AND ADVANCE WHEN IT OCCURS.

LEVEL 1 (QUICK KEY; 0-F) DELAY = DEC 65000 (DEC/HEX) A (0-65 K) PATTERNS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 2
(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 2

COMMENTS

WAIT FOR THE 65000 TH OCCURANCE OF EVENT 02. TRACE ONLY THAT LAST OCCURANCE AND THEN ADVANCE.

LEVEL 2 (QUICK KEY; 0-F) DELAY = DEC (DEC/HEX) 101 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 4
(2) TRACE NEVER
T = 0 4

COMMENTS

DON'T TRACE ANYTHING WHILE CHECKING FOR EVENT 04 WHICH SHOULD OCCUR EXACTLY 101 CLOCKS AFTER LEAVING THE LAST LEVEL.

LEVEL 3 (QUICK KEY; 0-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 8
(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 8

COMMENTS

CHECK THAT EVENT 08 OCCURS IMMEDIATELY UPON ENTERING THIS LEVEL. IF IT DOES, TRACE IT. STOP RECORDING, THE ADVANCE COMMAND SHOULD NOT BE EXECUTED WHEN IT COMES TRUE AS STOP TAKES PRIORITY.

Figure 10-99. Setup Guide: Segments, Patterns, and Total Trace Time (Sheet 1 of 2).

K101-D SET UP GUIDE 5.2.4

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF A0 SEQN Any radix fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 818 attached OR
5	DEVICE NOT AVAILABLE No RTE 818 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master external
2	EXTERNAL MULTI-PHASED Each section can be sampled at own external rate or Master external rate Section A - Section B - Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external Each section can be sampled at the Master external rate Internal clock period or 10ns Section A - Section B and or Section C - Master external or Internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external Each section can be sampled at own external rate the Master external rate Internal clock period or 10ns Section A - Section B and or Section C - Master external or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns Section A - Section B and or Section C - Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

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Figure 10-99. Setup Guide: Segments, Patterns, and Total Trace Time (Sheet 2 of 2).

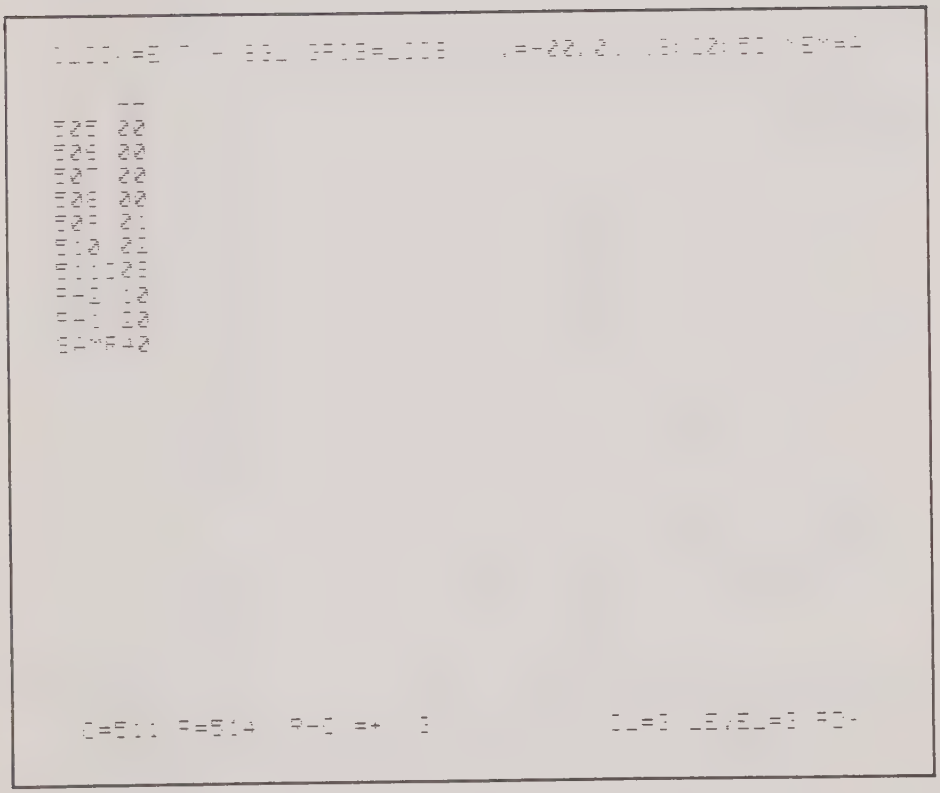

Figure 10-100. Only Three Words are Traced into Memory.

Press [TRACE CONTROL], [Hx3 1 H], [◁▷ SET] five times, [Hx1 0 G].

Press [ARM], [TIMING].

Note that the total trace time is now (typically) 65.26 milliseconds.

10.2.7 RECORD

10.2.7.1 **Manual Arm**

SET UP: See setup guide in Figure 10-101.

Press [TRACE CONTROL], [◁▷ SET], [Hx12 3 J], [◁▷ SET], [Hx1 0 G], [Hx3 1 H], [◁▷ SET] twice, [Hx6 2 I], [◁▷ SET] twice, [Hx3 1 H], [INPUT MODE], [△] twice, [▷], [PAGE↑ 8 O TTL].

RECORD: Press [ARM].

The instrument makes a single recording for each manual press of [ARM]. This allows you to take all the time you need to review and analyze each recording.

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [TIMING], [Hx12 3 J] (and [PAGE↓ 4 K] or [PAGE↑ 8 O TTL] as necessary to be on Page 4).

Your display should look like Figure 10-102 which is a timing display of a Probe Test recording. Manual recording allows unlimited time to review and analyze a display.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 6.1 OF ___ DATE _____

QUICK KEY See back for notes! (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
6
D N 5
A P 4
T U 3 AFAB
A T 2 AEAA
S 1 ADA9
LSB ACA8

RADIX CHOICES (B) BINARY (O) OCTAL (H) HEX (A) ASCII or (E) EBCDIC

TRACE CONTROL NOTES

For each level –
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any given time conditions

Quick Key	Command condition		
0	≠ DATA	0	
1	Always		
2	Never		
3	≠ DATA	0 and Sample Count	Delay
4	= DATA	0 and Sample Count	Delay
5	≠ DATA	0 and Sample Count	Delay
6	= DATA	0 and Sample Count	Delay
7	≠ DATA	0 and Sample Count	Delay
8	= DATA	0 and Sample Count	Delay

0 – S J A or T which are assigned by command code

TRACE CONTROL

LEVEL 0 (0-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1
(2) JUMP TO 0 (0-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS
FILL MEMORY AND STOP THE NEXT TIME 0.1 OCCURS.

LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)
( ) STOP
S =
( ) JUMP TO ___ (0-F)
J =
( ) ADVANCE
A =
( ) TRACE
T =

COMMENTS

LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)
( ) STOP
S =
( ) JUMP TO ___ (0-F)
J =
( ) ADVANCE
A =
( ) TRACE
T =

COMMENTS

LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F)
( ) STOP
S =
( ) JUMP TO ___ (0-F)
J =
( ) ADVANCE
A =
( ) TRACE
T =

COMMENTS

Figure 10-101. Setup Guide: Manual Arm (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # 6.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (.1.) MODE = EXT. SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↑	↑	↑	↑	↑	↑	↑	↑	–	–	–	–	–	–	–	–

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF AO sequence
1	OCTAL Fixed octal format & CF AO sequence
2	BINARY Fixed binary format & CF AO sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF AO SEQN Any radix fixed CF AO sequence
5	DEVICE MNEMONICS Fixed disassembled uP code format only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	— — — NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	— — — NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A - Section B - Section C - Internal clock period
	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master external
1	EXTERNAL MULTI PHASED Each section can be sampled at own external rate Master external rate - Section A - Section B - Section C & Master can be fed from external expressions
2	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate. Internal clock period or 10ns. Section A - Section B and or Section C - Master external or internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate. The Master external rate. Internal clock period or 10ns. Section A - Section B and or Section C Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A - Section B and or Section C Internal clock period or 10ns

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
	AUTO
	AUTO STOP IF A = B
	AUTO STOP IF A ≠ B
8	AUTO STOP IF A - B WITHIN LIMITS
9	AUTO STOP IF A ≠ B WITHIN LIMITS

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
	NEGATIVE

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Figure 10-101. Setup Guide: Manual Arm (Sheet 2 of 2).

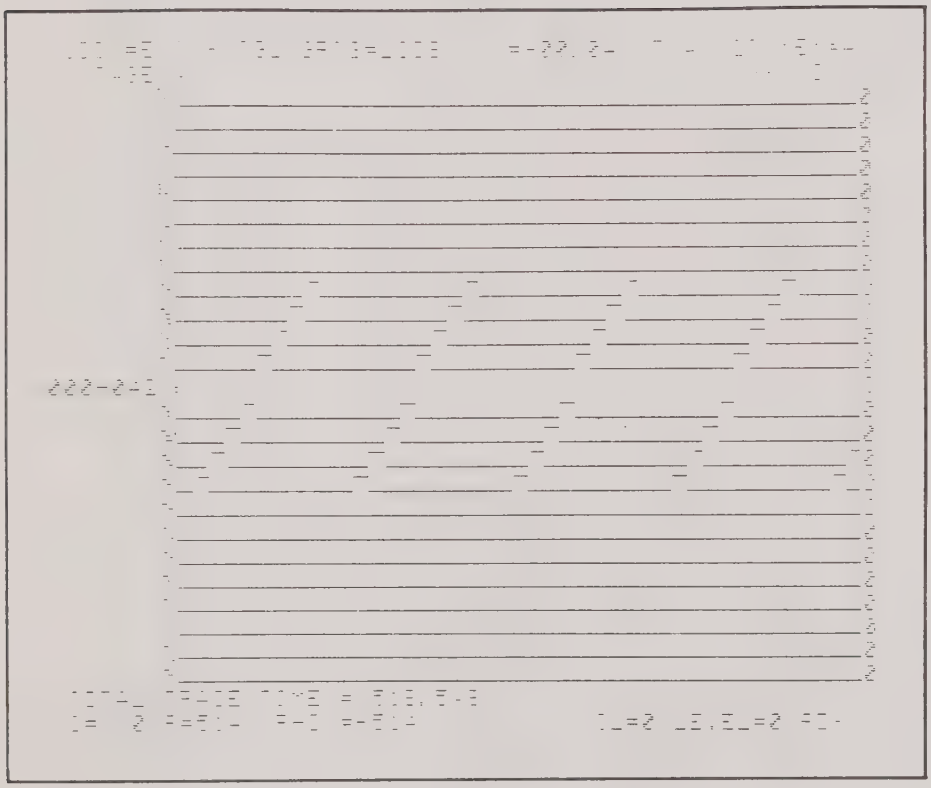


Figure 10-102. Probe Test Timing Display.

10.2.7.2 **Auto Arm**

SET UP: To avoid repeatedly pressing [ARM] by hand when you need to make multiple recordings, change the arm mode to Auto.

Press [INPUT MODE] , [△] , [Hx3 1 H] .

RECORD: Press [ARM] .

Watch the trace control level and status words. LEVEL = alternates between * and 0. The current trace level and number of the current recording are indicated in the bottom status field. A cumulative count of completed recordings is displayed in the upper right of the Input Mode screen (see Figure 10-103). While this automatic rearming and recording process is going on you can press any DISPLAY or SPECIFY key at any time.

Note

It is possible to change a setup parameter of Specify screen during auto recordings. However, to ensure that the change is accepted, press [STOP] , make the change, then press [ARM] .

Press [DATA] , [TIMING] , [GRAPH] .

Observe several recording cycles in each display mode. Press the other DISPLAY keys to see their effect.

This process can continue indefinitely as long as the trace control conditions of each recording are satisfied. If an expected STOP, JUMP, or ADVANCE command condition

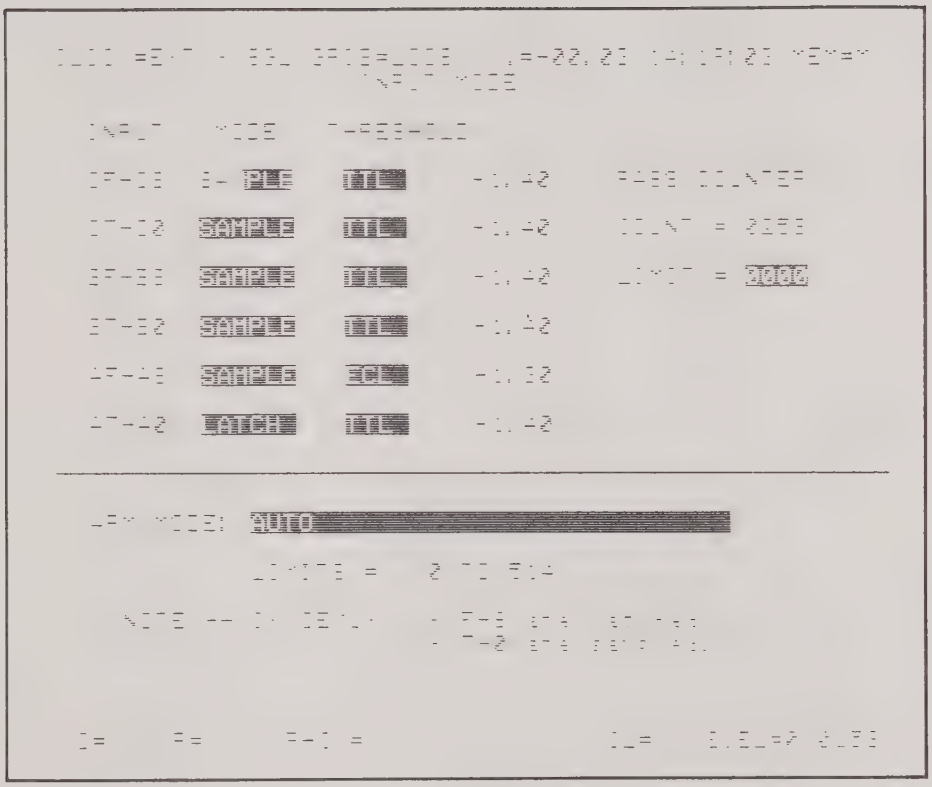


Figure 10-103. Status Field Display.

is not met, the process stops. The level message displays the number of the "stuck" trace level and the count stays at the count of the current hung up recording. If and when the condition comes true, the auto arming and count resume where they left off. Similarly, loss of an external clock input causes a halt. To simulate such an error, unplug the probe from the test socket. Note that the trace status says F CLK? because the expected external sample clock is absent. Plug the probe back in. The recordings and count will resume.

To completely halt the process you must press [STOP] or [M→A]. Press [STOP].

REVIEW: Notice that the trace status word has gone to RDY. The total number of recordings you made can be seen by pressing **INPUT MODE** (see Figure 10-104). The trace status word RDY indicates the completion of an auto arming recording cycle. The total number of recordings made is held until a new arm cycle is begun. If you press **ARM** again, the count initializes to zero and the process begins again.

10.2.7.3 **Limiting the Count**

SET UP: Set a limit of 100 cycles.

Press [INPUT MODE], [▷] twice, ^{1}H, [0]G twice.

Setting a limit on the pass counter stops automatic recordings when that limit is reached. If all 100 recordings are successful (i.e., do not fail or get hung up) then you can be reasonably confident your system will not fail more than 1 time out of 100. Confidence that

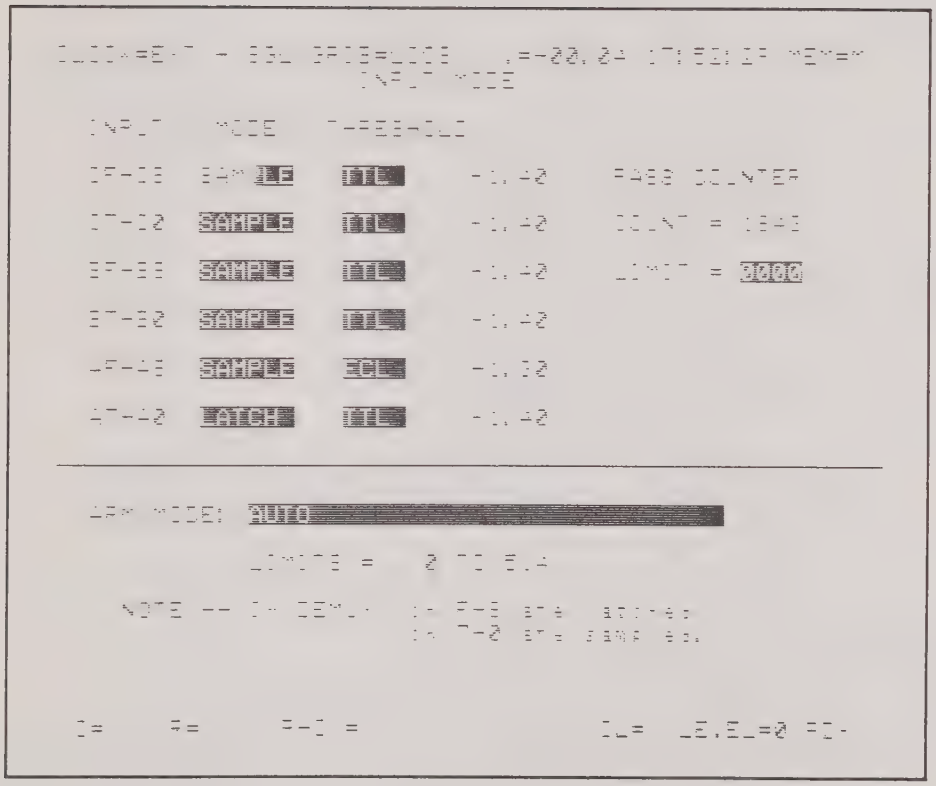


Figure 10-104. Completion of Auto Arming Recording Cycle.

your system is truly operational and debugged comes from obtaining successful test results over numerous recordings.

RECORD: Press [ARM] and observe the count.

It continues until 100 recordings have been made and then stops (see Figure 10-104a and 10-104b) as long as each test is successful. Remove the count limit.

Press [INPUT MODE], [▷], twice, [0] G .

10.2.7.4 **Stop if A ≠ B**

SET UP: Press [INPUT MODE], [△], [3] J .

To load memory B with a known "good" recording, press [A→B] .

RECORD: Press [ARM] .

New recordings are continually compared to the contents of B in search of any unknown or intermittent errors. This process is sometimes referred to as "baby-sitting." Observe the count. To create an "error" or difference between the current and stored recording, edit the B memory.

Press [DATA], [B], [EDIT], [▽] SET, [1] H , [EDIT] .

The process stops since A and B are now unequal.

REVIEW: Press [COMPARE A/B] .

The display should look like Figure 10-105. Any difference between the current and reference recording will stop the automatic arming process. To see the number of recordings and comparisons made before the "error" occurred,

press [INPUT MODE] .

ALTERNATE SET UP: An alternate method of comparing recordings is to change Clock Select display to the following:

MODE = INTERNAL

INTERNAL CLOCK PERIOD = 40 NANOSECONDS

Press [CLOCK SELECT] , [Hx1 0 G] , [▽ SET] , [PAGE 4 K] , [Hx1 0 G] .

RECORD: Press [ARM] .

The instrument will make one recording and stop. Press [A→B] to load memory B.

Press [ARM] again.

Even though the trace control routine is identical, samples are now being taken asynchronously. It is therefore unlikely that every sample will be taken at exactly the same place in the pattern as in the previous recording. Therefore, auto arming will probably stop after only one recording.

```
CLOCK=EXT - SGL GRIB=LOCS    .=-00.03 16:21:19 MEM=3

     --       --       --       --       --       --
000C00   024 08   048 80   072 02   096 20   120 00
001=11   025 10   049 00   073 04   097 40   121 01
002 02   026 20   050 00   074 08   098 80   122 02
003 04   027 40   051 01   075 10   099 00   123 04
004 08   028 80   052 02   076 20   100 00   124 08
005 10   029 00   053 04   077 40   101 01   125 10
006 20   030 00   054 08   078 80   102 02   126 20
007 40   031 01   055 10   079 00   103 04   127 40
008 80   032 02   056 20   080 00   104 08   128 80
009 00   033 04   057 40   081 01   105 10   129 00
010 00   034 08   058 80   082 02   106 20   130 00
011 01   035 10   059 00   083 04   107 40   131 01
012 02   036 20   060 00   084 08   108 80   132 02
013 04   037 40   061 01   085 10   109 00   133 04
014 08   038 80   062 02   086 20   110 00   134 08
015 10   039 00   063 04   087 40   111 01   135 10
016 20   040 00   064 08   088 80   112 02   136 20
017 40   041 01   065 10   089 00   113 04   137 40
018 80   042 02   066 20   090 00   114 08   138 80
019 00   043 04   067 40   091 01   115 10   139 00
020 00   044 08   068 80   092 02   116 20   140 00
021 01   045 10   069 00   093 04   117 40   141 01
022 02   046 20   070 00   094 08   118 80   142 02
023 04   047 40   071 01   095 10   119 00   143 04
    TOTAL # =  1     FIRST # =  1     LAST # =  1
 C=  0 R=514 (R-C)=+514(          ) CL=0 LEVEL=0 RDY
```

Figure 10-105. Automatic Arming Process Stopped.

REVIEW: Press [DATA] to see the specific differences.

There may be a few differences (see Figure 10-106) or many (see Figure 10-107). Figure 10-106 shows that even similarly traced asynchronous recordings usually differ due to the one sample uncertainty of plus or minus one. Figure 10-107 shows that similarly traced asynchronous recordings may differ significantly depending on the specified sample rate and trace condition.

Press [ARM] several times.

10.2.7.5 **Auto Stop if A = B**

SET UP: To check for a specific suspected error, or to check if and when a system will perform as specifically desired, change the arm mode to look for equality.

Press [INPUT MODE], [△], [Hx6 2'].

RECORD: Press [ARM].

Watch the count. Because of the asynchronous sampling, each new recording will most likely be different from the stored recording. However, the odds are good that eventually an exact match will occur and therefore halt the process. In Figure 10-108 267 asynchronous recordings were taken and compared before a match occurred.

REVIEW: When rearming stops, press [DATA].

Note that the memory contents are identical. In Figure 10-109 every sample of the 267th recording is identical to the previously stored recording.

```
LLIOK=0040 ·BEC GPIE=LIOE    A=-00.0I 18:18:51 MEM=A

     HH        HH        HH        HH        HH        HH
000C00  024 01  048 02  072 04  096 08  120 10
001 00  025 01  049 02  073 04  097 08  121 10
002 00  026 01  050 02  074 04  098 08  122 10
003 00  027 01  051 02  075 04  099 08  123 10
004 00  028 01  052 02  076 04  100 08  124 10
005 00  029 01  053 02  077 04  101 08  125 10
006 00  030 01  054 02  078 04  102 08  126 10
007 00  031 01  055 02  079 04  103 08  127 10
008 00  032 01  056 02  080 04  104 08  128 10
009 00  033 00  057 02  081 04  105 08  129 10
010 00  034 02  058 00  082 04  106 08  130 10
011 01  035 02  059 00  083 00  107 08  131 10
012 01  036 02  060 04  084 08  108 00  132 10
013 01  037 02  061 04  085 08  109 00  133*10
014 01  038 02  062 04  086 08  110 00  134 20
015 01  039 02  063 04  087 08  111 10  135 20
016 01  040 02  064 04  088 08  112 10  136 20
017 01  041 02  065 04  089 08  113 10  137 20
018 01  042 02  066 04  090 08  114 10  138 20
019 01  043 02  067 04  091 08  115 10  139 20
020 01  044 02  068 04  092 08  116 10  140 20
021 01  045 02  069 04  093 08  117 10  141 20
022 01  046 02  070 04  094 08  118 10  142 20
023 01  047 02  071 04  095 08  119 10  143 20
    TT-TL * =  I     T-T-T * =I00     T-T-T * =I00
 I=  0 P=514  P-I =+514  20.5643  CL=0 LEVEL=0 PD+
```

Figure 10-106. Asynchronous Recordings Differences.

```
LLIO*=0040 ·BEC GPIE=LIOE    A=-00.0I 18:18:05 MEM=A

     --        --        --        --        HH        HH
000I01  024*02  048*04  072*08  096*10  120*20
001*01  025*02  049*04  073*08  097*10  121*20
002*01  026*02  050*04  074*08  098*10  122*20
003*01  027*02  051*04  075*08  099*10  123*20
004*01  028*02  052*04  076*08  100*10  124*20
005*01  029*02  053*04  077*08  101*10  125*20
006*01  030*02  054*04  078*08  102*10  126*20
007*01  031*02  055*04  079*08  103*10  127*20
008*01  032*02  056*04  080*08  104*10  128*20
009*01  033*02  057*04  081*08  105*10  129*20
010*01  034 02  058*04  082*08  106*10  130*20
011 01  035 02  059*04  083*08  107*10  131*20
012 01  036 02  060 04  084 08  108*10  132*20
013*02  037*02  061 04  085 08  109*10  133*20
014*02  038*02  062*04  086*08  110*20  134*00
015*02  039*02  063*04  087*08  111 10  135*00
016*02  040*04  064*08  088*08  112 10  136 20
017*02  041*04  065*08  089*20  113*20  137*00
018*02  042*04  066*08  090*20  114*20  138*00
019*02  043*04  067*08  091*10  115*20  139*00
020*02  044*04  068*08  092*10  116*20  140*40
021*02  045*04  069*08  093*10  117*20  141*40
022*02  046*04  070*08  094*10  118*20  142*40
023*02  047*04  071*08  095*10  119*20  143*40
    T-T-T * =429     T-T-T * =  2     T-T-T * =514
 I=  2 P=514  P-I =+514  20.5643  CL=0 LE.EL=0 PD+
```

Figure 10-107. Effect of Specified Sample Rate and Trace Condition.

```
[illegible]=2242  [illegible]=[illegible]  =-22 2-  [illegible]

  [illegible]   [illegible]   [illegible]

  [illegible]  SAMPLE  TTL   -1.42   [illegible]
  [illegible]  SAMPLE  TTL   -1.42   [illegible] = [illegible]
  [illegible]  SAMPLE  TTL   -1.42   [illegible] = 0000
  [illegible]  SAMPLE  TTL   -1.42
  [illegible]  SAMPLE  ECL   -1.12
  [illegible]  LATCH   TTL   -1.42

  [illegible]: AUTO STOP IF A=B

          [illegible] =   2 [illegible]

    NOTE -- [illegible]

  I=    R=     R-I =                    DL=  [illegible]=2 [illegible]
```

Figure 10-108. 267 Recordings Compared Before Match.

```
[illegible]=2242  [illegible]=[illegible]   .=-22.2-  [illegible]

     --        --        --        --        --        --
2221 22  214 21  245 21  271 24  276 25  122 12
221 22  215 21  245 21  271 24  277 25  121 12
221 22  216 21  252 21  274 24  273 25  111 12
221 22  217 21  251 21  275 24  277 25  111 12
224 22  218 21  252 21  276 24  122 25  114 12
225 22  219 21  251 21  277 24  121 25  115 12
226 22  220 21  254 21  278 24  121 25  116 12
227 22  221 21  255 21  279 24  121 25  117 12
228 22  222 21  256 21  232 24  124 25  118 12
229 22  223 21  257 21  231 24  125 25  119 12
210 22  224 21  258 22  261 22  125 25  130 12
211 21  225 21  259 22  211 25  127 22  131 12
212 21  226 21  262 24  234 25  125 22  132 12
213 21  227 21  261 24  255 25  125 22  133 12
214 21  228 21  261 24  253 25  112 22  134 12
215 21  229 21  267 24  257 25  111 12  135 12
216 21  242 21  264 24  253 25  111 12  136 12
217 21  241 21  255 24  255 25  112 12  137 12
218 21  242 22  266 24  250 25  114 12  138 12
219 21  243 22  267 24  291 25  115 12  139 12
220 21  244 22  268 24  292 25  116 12  140 12
221 21  245 22  269 24  293 25  117 12  141 12
222 21  246 22  270 24  294 25  118 12  142 12
223 21  247 22  271 24  295 25  119 12  143 12
    [illegible] * =  2     [illegible] * =  0     [illegible] * =  2
 I=  2 R=[illegible]  R-I =-[illegible]  [illegible]  [illegible]=2 [illegible]=2 [illegible]
```

Figure 10-109. Identical Recordings.

10.2.7.6 **Auto Stop if A ≠ B Within Limits**

SET UP: Once the problem area has been narrowed down, it often isn't necessary to compare the entire recording, only portions of it. To do this, change the arm mode.

Press [INPUT MODE], [△], [V24 5 L], then go back to synchronous clocking.

Press [CLOCK SELECT], [Hx3 1 H].

RECORD: Press [ARM], [A→B], [ARM] to load memory B and initiate the auto arming.

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], twice to set the cursors to frame the area of comparison.

Press [INPUT MODE] to check the cursors' locations (see Figure 10-110).

Press [DATA], [B], [▷], [EDIT], [DEMUX F V HEX], [EDIT].

Rearming does not stop because the inequality is outside the area defined by the cursors (see Figure 10-111).

Press [EDIT], [▽ SET] twice, [Hx3 1 H], [EDIT].

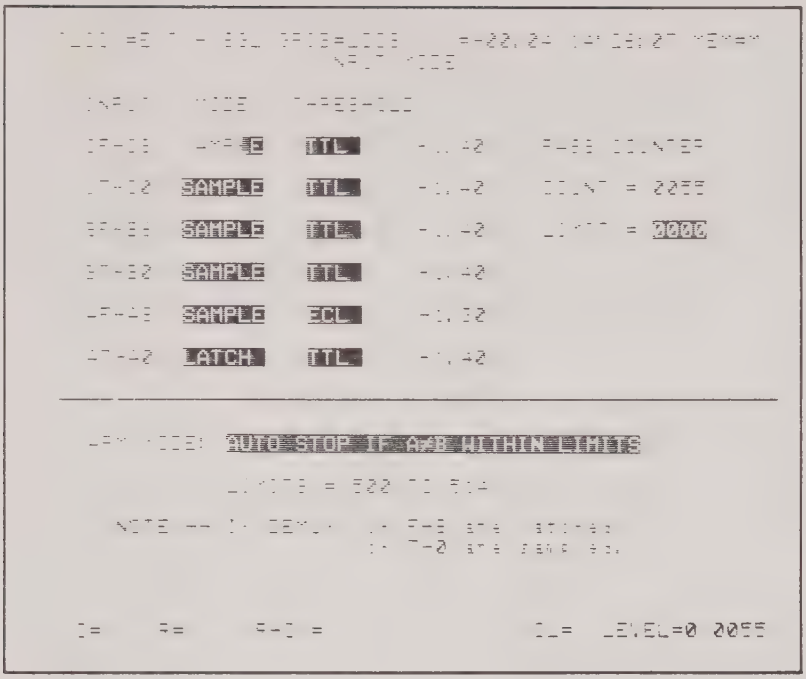


Figure 10-110. Comparison Between Location 500 and 514.

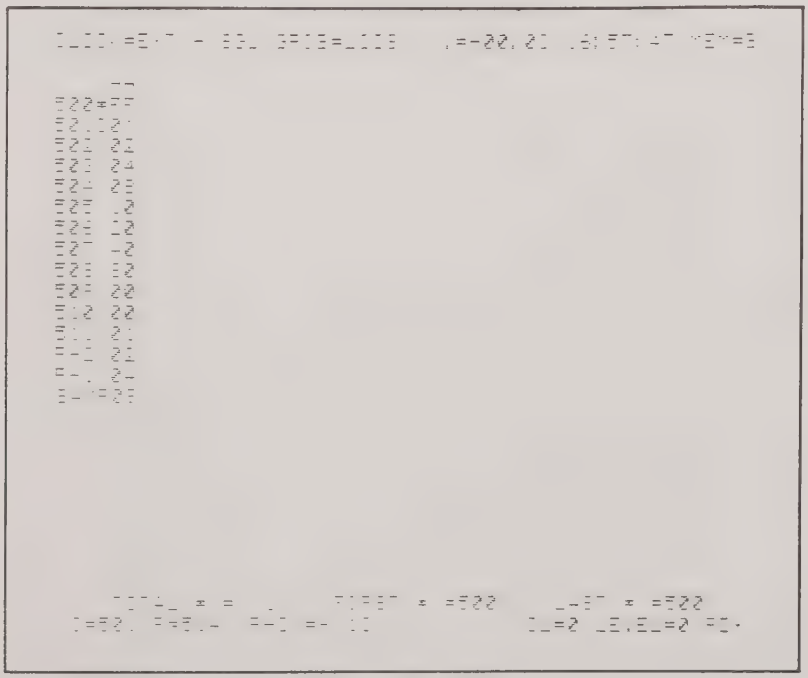


Figure 10-111. Inequality Outside Window.

The auto stop condition is now satisfied as the change is within the cursor limits.

REVIEW: The display should look like Figure 10-112 which shows that an inequality within the limited comparison window stops auto arming.

10.2.7.7 **Auto Stop if A = B Within Limits**

SET UP: A check for equality similarly may be focused on a smaller area of the recording. Change the arm mode.

Press [INPUT MODE], [△], [PAGE ↑ 4 K], [DATA], [B].

RECORD: Press [ARM] to start the recording process.

Since the memories were made unequal in the previous exercise, the rearming could continue indefinitely.

Press [EDIT], [◁+ ▽ SET], [Hx1 0 G], [EDIT].

Recording will stop.

REVIEW: Between the Control Cursor and the Reference Cursor, memories A and B are now identical (see Figure 10-113), which satisfied the auto stop condition. Figure 10-113 shows that arming stops when the samples in the windowed area become the same.

Figure 10-112. Inequality Within Window.

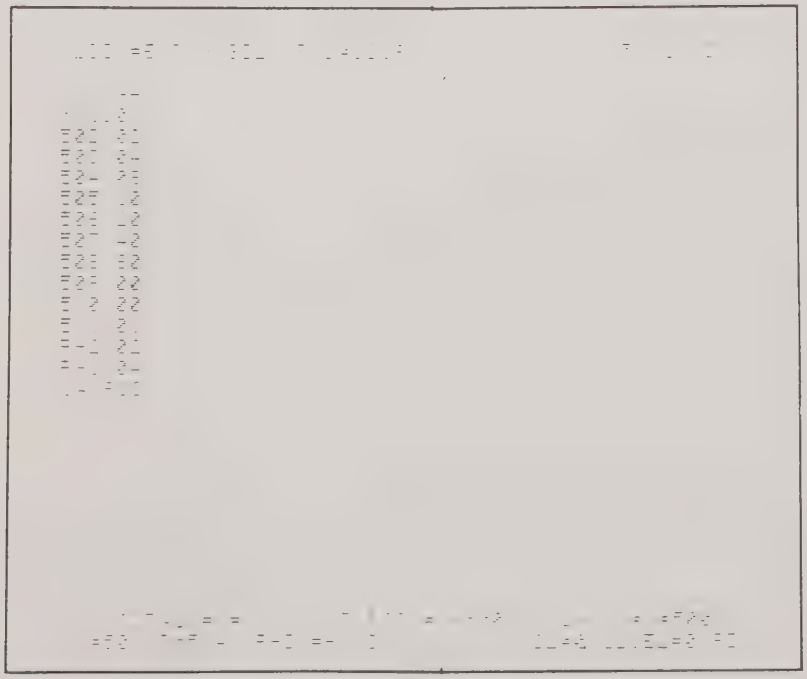


Figure 10-113. Samples in Window Same Arming Stops.

10.3 POWER UP TEST

As soon as the power is turned on, the K101-D will beep and start executing an automatic diagnostic routine of six tests. As each test is completed, the next test is automatically run. When all tests are successfully completed, the analyzer beeps again and displays the Clock Select setup screen.

If an error is detected in any of the tests, the name of the failed test is displayed and further testing halted. To run the rest of the power up tests, or to attempt to operate the instrument despite the error, press **NEXT** to continue. When the last test (successful or not) is completed, the Clock Select setup screen is displayed. At this point, since an error has been detected, you should run the appropriate Self-Test diagnostic routine (see paragraph 10.4, Self Test). Table 10-2 lists the power up error messages and the action you should take to respond to these messages. The following paragraphs briefly describe the six power up tests.

10.3.1 K101-D ROM TEST

A total of 16 EPROMs are individually tested against known check sums. The failure display uses an 8 x 2 grid to indicate the physical location of the bad ROM on the K101-D MPU PC board (see Figure 10-114). Any failure can cause incorrect operation of the unit.

10.3.2 K101-D RAM TEST

A total of sixteen 64K RAMs are tested and any failures are displayed in a grid indicating the faulty RAM location on the K101-D MPU PC board (see Figure 10-115). Any failure can cause incorrect operation of the unit.

Table 10-2. Power Up Test Error Messages

Error Message	Appropriate Response
1. ROM: see Figure 10-114	Advise Gould repair facility
2. RAM: see Figure 10-115	Advise Gould repair facility
3. Power supply: see Figure 10-116	Run indicated Self-Test and advise Gould repair
4. CMOS RAM checks in error	See paragraph 10.3.4. Advise Gould repair facility if error does not clear
5. USART: see Figure 10-117	
6. Stuck key	See paragraph 10.3.6. Advise Gould repair facility as to which key is stuck

```
ROM CHECKSUM ERROR:

   MAP OF ROMS ON MPU BOARD (G=GOOD, X=BAD)

   COL→    1    2
   ROW↓
      A    G    G
      B    G    G
      C    G    G
      D    G    G
      E    G    G
      F    G    G
      G    G    G
      H    G    X

PRESS "NEXT" TO CONTINUE
```

Figure 10-114. ROM Test Grid.

```
MPU MEMORY FAILURE:

   MAP OF RAMS ON MPU BOARD (G=GOOD, X=BAD)

   COL→    3    4    5    6
   ROW↓
      A         X         G
      B         G         G
      C         G         G
      D         G         G
      E         G         G
      F         G         G
      G         G         G
      H         G         G

PRESS "NEXT" TO CONTINUE
```

Figure 10-115. RAM Test Grid.

10.3.3 POWER SUPPLY TEST

Each of the power supply's voltage outputs is tested on a pass/fail basis. If any supply is out of tolerance, the testing stops and a message is displayed indicating which power supply failed (see Figure 10-116). Power supply tolerances are discussed in paragraph 10.4. A failure may or may not cause improper operation of the unit, depending on the nature of the failure.

10.3.4 CMOS RAM TEST

The stored data are tested against a check sum also stored in the CMOS RAM. (This is not the same as the CMOS RAM Self-Test.) A failure causes an error message (CMOS RAM CHECKSUM ERROR) to be displayed. An error indicates that the unit will not properly recall the recording setup parameters previously stored, nor correctly save new ones.

The appearance of the error message does not necessarily mean a component has failed. The source could be an intermittent, "soft" error. The following procedure will clear such a soft error:

Press [CHOICE NEXT]. Wait for Clock Select to be displayed.

Press [SHIFT], [RECALL], and [SAVE].

This loads the default setups from ROM into the CMOS RAM. If the original error was not caused by a component failure, the CMOS RAM CHECKSUM ERROR should not appear on the next power up and the CMOS memory should operate correctly. You can test this by changing any parameter from its default value, pressing **SAVE**, then **RECALL**, and seeing if the changed parameter is still there as it should be.

10.3.5 USART ERRORS

The status of the communication I/O USART is checked for failures. USART failures may cause incorrect operation of the unit. See Figure 10-117 for USART error messages.

10.3.6 KEYBOARD TEST

Each one of the keys on the front panel keyboard is tested for a NOT PRESSED condition. If a pressed key is observed, the unit displays an error message: STUCK KEY. Press one key at a time; keys that are not stuck cause the unit to beep when pressed. Stuck keys must be repaired in order to continue operation of the unit.

10.4 **SELF-TEST**

Self-Test is selected by pressing **SHIFT**, then **SELF TEST**. The screen will display a menu of the various tests that can be run (see Figure 10-118). To run a specific test, move the cursor up or down (field up or field down) to the desired test then press **NEXT**. Depending on the test, the unit either starts an actual test or displays a more detailed submenu. To run a specific submenu test, again move the cursor to the desired test and press **NEXT**. To exit a submenu and return to the main menu, press **PREV**. To exit Self-Test altogether, press **PREV** while in the main Self-Test menu.

A confidence test generally runs all the specific tests listed beneath it. At the completion of a confidence test, the display says only whether the tests passed or failed; no detailed failure information is given. At the completion of the confidence tests (there is no screen indication showing that a test is being run while it is executing) END OF TEST and test PASSED, or FAILED are displayed. Have patience. Some tests (such as trace control) take several minutes to complete. Also, failures will extend the testing time.

```
POWER SUPPLY FAILURE =  +05.0
```

Figure 10-116. Power Supply Error Messages.

```
232 USART ERROR -- PRESS NEXT TO CONTINUE.  STAT= FF
```

Figure 10-117. USART Error Messages.

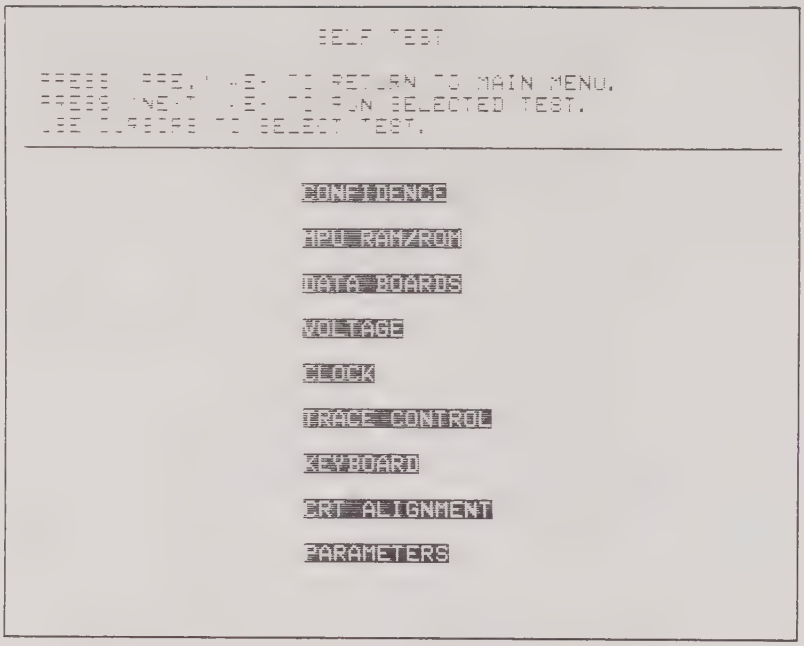


Figure 10-118. Main Menu When First Entering Self-Test.

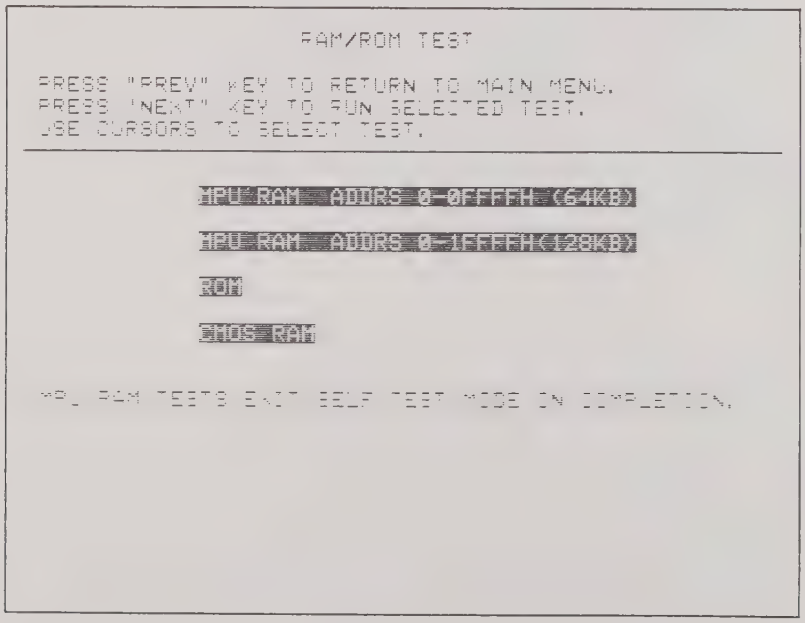


Figure 10-119. MPU RAM/ROM Test Submenu.

Running the specific diagnostic tests individually results in an error summary listing of the type and number of failures as well as specific failure information. The format of this detailed error information is specified in the Parameters screen (discussed later in this section).

10.4.1 CONFIDENCE TEST

Runs all tests in the main menu except for Keyboard, CRT alignment, and Parameters.

10.4.2 K101-D MPU RAM/ROM

When this test is selected, the submenu appears as shown in Figure 10-119.

10.4.2.1 **MPU RAM (64K)**

This test checks the first half of the memory RAM on the MPU board. Failures are displayed on a grid showing faulty RAM locations on the MPU board. This test is also run during power up testing. Failures may or may not affect system operation. Failures can be listed by each bad memory location when using the scroll selection of the Parameter screen. Note that upon completion of this test, Self-Test mode is automatically exited.

10.4.2.2 **MPU RAM (128K)**

This test checks all of memory RAM on the MPU board. It operates identically to the MPU RAM (64K) test.

10.4.2.3 **ROM**

This test verifies the check sum of all 16 EPROMs on the MPU board. Any failures are displayed on a grid, to show the location of the faulty ROM. This test is also run during power up testing.

10.4.2.4 **CMOS RAM**

This test checks the ability of the CMOS RAMs to store new data. Failures are listed as specified by the Parameter screen. A failure indicates the unit will fail the CMOS RAM test (of the power up tests), and that the unit will power up with unwanted recording setups. Refer to paragraph 10.3.4 for instructions to clear CMOS RAM errors.

10.4.3 DATA BOARDS

When this test is selected, the submenu shown in Figure 10-120 is displayed.

10.4.3.1 **Confidence**

This test runs all three data board tests.

10.4.3.2 **Data Board A**

When this test is selected, the submenu shown in Figure 10-121 is displayed.

10.4.3.3 **Confidence Test**

Runs all of the tests on the specific data board.

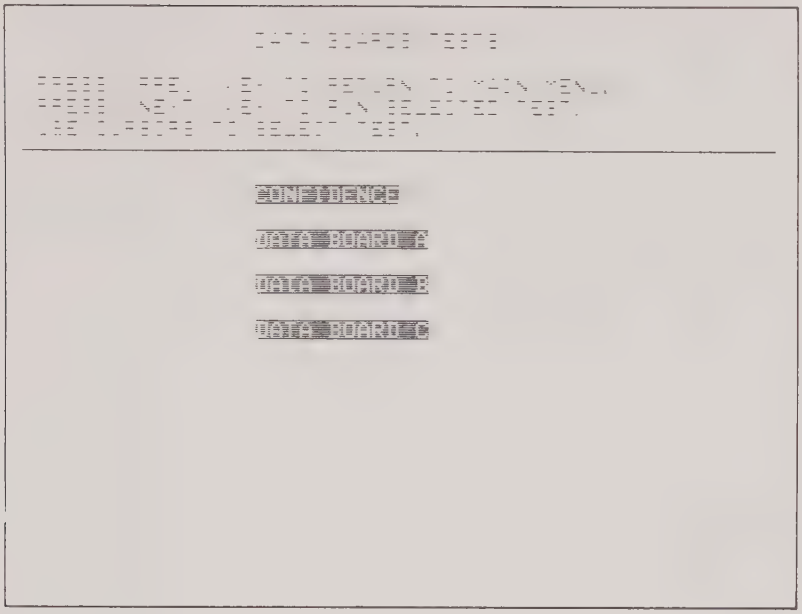
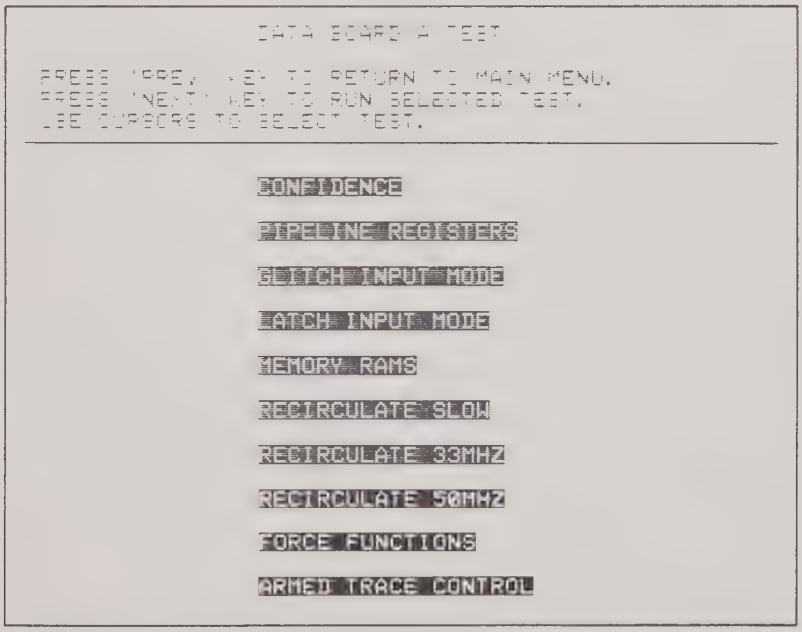


Figure 10-120. Data Board Tests Submenus.



Note: The Menus for boards B and C are identical.

Figure 10-121. Data Board A Submenu.

10.4.3.4 **Pipeline Registers**

This test checks the pipeline register circuitry on the data board. A failure indicates which of that section's 16 inputs will not record properly. Failures are displayed to show the data expected and data actually recorded in hex words.

10.4.3.5 **Glitch Input Mode**

This test checks the ability of all the inputs to detect glitches while in the glitch mode. Failures are displayed to show hex data words that indicate which inputs are not detecting properly. If this is the only test that failed, the only operation that should be affected is that of glitch capture.

10.4.3.6 **Latch Input Mode**

All of the latch inputs are tested for proper operation. For failures, readings similar to those for other data board tests are displayed. Typically, if the unit fails this test, an input is not sampled.

10.4.3.7 **Memory RAMs**

This test checks the ability of the high-speed memory RAMs to store information. Note that if there are failures in the previous data board test, the memory RAMs appear to be bad but may not be. Failures are displayed in hex as in previous tests. Typically, if the memory RAMs fail, recorded information is incorrect.

10.4.3.8 **Recirculate Slow**

This is a slow-speed test of the capability of the data board to feed information out of the memory RAM and then back into RAM. A failure in

this process may not be apparent when making a normal recording unless certain functions are performed with the logic analyzer. Failures are displayed in hex.

10.4.3.9 **Recirculate 33 MHz**

This is the same test as Recirculate Slow, except the test runs at 33 MHz.

10.4.3.10 **Recirculate 50 MHz**

This is the same test as Recirculate Slow, except the test runs at 50 MHz.

10.4.3.11 **Force Functions**

This test checks the recording control of the data board. If failures are observed, more than one channel may be inoperative. (Test mnemonics require a technical description from the factory.)

10.4.3.12 **Armed Trace Control**

This test checks trace control functions within the data board for errors. (Error descriptions require further technical information from the factory.) Failures may or may not cause improper operation of the unit, depending upon the failure and nature of the trace control functions being performed.

10.4.3.13 **Confidence**

This test runs all tests except for DVM and Calibrate. Note that the probes must be connected before running this test.

10.4.3.14 **ADC Calibration**

This test checks the voltage measurement circuits by measuring the +10.00 V reference. An error here may indicate the DVM circuitry is faulty or out of calibration. A DVM fault can cause incorrect failures to be displayed on any voltage test. Another cause could be the +10.00 V reference being out of tolerance. Refer to paragraph 10.4.3.22 for information on the reference supply.

10.4.3.15 **Power Supply Test**

This test checks that each power supply is within set tolerances. Refer to paragraph 10.4.3.21 for power supply tolerances. Each failed power supply is displayed. The tested power supplies are the +15, -15, -10, -5.2, and -2 V battery and the +10 V reference supply.

10.4.3.16 **Threshold Source**

There are four different threshold selections available. The circuitry that generates the four voltages (TTL, ECL, VAR A, VAR B) is tested for accuracy. Any failures displayed indicate that the threshold voltage is not accurate on any probes that are trying to use that threshold.

10.4.3.17 **Threshold Selection**

This test verifies that each probe can be operated on TTL, ECL, VAR A, or VAR B. A failure is displayed if any threshold selector does not put out the correct voltage. This test may fail if there was a failure in the Threshold Source test.

10.4.3.18 **Probe Loading**

This test verifies the accuracy of the load the input probe has on the threshold voltage. If there is no connection to a probe, the voltage measures too high and is indicated as a failure. Also, if the probe is bad, it may short the voltage such that it measures too low, and so indicates a failure. The probes must be connected to run this test.

10.4.3.19 **Variable A/B**

This test checks the linearity of the variable threshold voltages. This test measures linearity at the output going to the input probe. A failure indicates the variable voltages are bad or out of tolerance. Recordings are not affected, unless the threshold that failed is selected. The probes must be connected before running this test.

10.4.3.20 **DVM**

This test requires the installation of DVM cables to the input probe connector. Without jumpers, this test will fail. Install a jumper from the +DVM input to pin 14 of the A8 section input probe connector (lower right hand pin). Install a jumper from the -DVM (ground) to pin 14 of the A0 section input probe connector. The jumpers connect the threshold voltages to the DVM inputs. The external DVM circuitry is tested for accuracy and linearity. If there are threshold failures, the DVM test may fail. Specific voltage measurement failures are displayed.

10.4.3.21 **Calibrate**

This test displays the voltages actually measured and the acceptable tolerances. The display is continually updated every few seconds. Power supply voltages can be adjusted by monitoring this display, but it is recommended that you adjust power supplies by the calibration

procedure. The display that is observed while in the Calibrate mode is shown in Figure 10-122.

The following is a list of the various power supply voltages and the associated circuitry to which they provide power:

a. ±15 V -- Display and threshold circuitry
b. ±10 V -- Threshold voltage generation circuitry
c. -5.2 V -- ECL circuitry within the unit
d. +5 V -- TTL circuitry within the unit
e. -2 V -- Many ECL pull-down resistors
f. Battery -- CMOS RAMs

10.4.4 VOLTAGE TEST

When this test is selected, the submenu shown in Figure 10-123 is displayed.

10.4.5 CLOCK

When this test is selected, the submenu shown in Figure 10-124 is displayed.

10.4.5.1 **Confidence**

This test runs both the Clock Frequency and the Level Memory tests.

10.4.5.2 **Clock Frequency**

This test checks the various internal clock frequencies on which the unit operates. The multiplier frequencies and actual measurements are displayed if a failure is noted.

CALIBRATE

SUPPLY NOMINAL	ACCEPTABLE MINIMUM	ACCEPTABLE MAXIMUM	MEASURED AVERAGE	MEASURED P-P
+15.00 V	+14.40	+15.60	+15.02	+0.03
-15.00 V	-15.60	-14.40	-15.03	+0.05
-10.00 V	-10.10	-9.90	-9.99	+0.00
-5.04 V	+4.94	+5.24	+5.02	+0.01
-5.23 V	-5.48	-5.08	-5.10	+0.09
-1.03 V	-1.15	-1.00	-1.09	+0.04
V BATT	-2.34	-4.00	+3.06	+0.00
INT REF	-0.02	+0.02	-0.00	+0.00
-10V REF	+9.96	+10.04	+10.00	+0.00

USE "PREV" TO RETURN TO MENU

Figure 10-122. Typical Calibrate Display.

VOLTAGE TESTS

PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.

CONFIDENCE

ADC CALIBRATION

POWER SUPPLY

THRESHOLD SOURCE

THRESHOLD SELECTOR

PROBE LOADING

VAR A/B

DVM

CALIBRATE

PROBES MUST BE INSTALLED FOR CONFIDENCE TEST AND
FOR PROBE LOADING AND VAR A/B TESTS.
DVM TEST FIXTURE IS REQUIRED FOR DVM TEST.

Figure 10-123. Voltage Test Submenu.

```
                    CLOCK BOARD TESTS

PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.
------------------------------------------------------------

                    CONFIDENCE

                    CLOCK FREQUENCY

                    LEVEL MEMORY
```

Figure 10-124. Clock Test Submenu.

10.4.5.3 **Level Memory**

This test checks the ability of the level memory RAMs to store the level at which trace control samples were recorded. Failures are displayed by memory location. A failure here indicates the memory will not be accurate.

10.4.6 TRACE CONTROL

When this test is selected, the submenu shown in Figure 10-125 is displayed.

10.4.6.1 **Trace Confidence**

This test runs all of the tests in the menu.

10.4.6.2 **Force Conditions**

This test checks the ability of the unit to perform basic trace control functions. A failure indicates the unit may not perform trace control functions, depending upon the failure.

```
                    TRACE CONTROL TESTS

PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.
------------------------------------------------------------

                    TRACE CONFIDENCE TEST

                    FORCE CONDITIONS

                    ADVANCE AND JUMP

                    WORD DETECTION RAMS

                    DELAY CONTROL RAM

                    DELAY RAMS

                    DELAY COUNTERS

                    WORD SELECTION

                    WORD SELECTION RAMS
```

Figure 10-125. Trace Control Test Submenu.

10.4.6.3 **Advance and Jump**

This test checks the ability of the unit to ADVANCE and JUMP to the various levels of trace control. A failure indicates the unit may not record properly, depending upon the failure and the functions the logic analyzer is trying to perform.

10.4.6.4 **Word Detection RAMs**

This test checks the RAMs' capability to store data that control the word detection circuitry. A failure indicates the unit may not recognize the S, J, A, and T word recognizers used in the trace control commands. This test takes several minutes to run.

10.4.6.5 **Delay Control RAM**

This test checks the RAMs' capability to store data that control the delay control circuitry. A failure indicates the unit will not perform delay functions, depending on the failure.

10.4.6.6 **Delay RAMs**

This test checks the ability of the RAMs to store data that control the amount of delay in tracing functions. A failure indicates the unit may not delay by the proper amount of clocks or events, depending on the failure.

10.4.6.7 **Delay Counters**

This test checks the ability of the unit to count the correct number of clocks or events. A failure indicates the unit may not delay by the proper amount when tracing, depending upon the failure.

10.4.6.8 **Word Selection**

This test checks the ability of the unit to recognize each S, J, A, and T word. A failure indicates the word selection circuitry may not tell the word detection RAMs when a condition is satisfied.

10.4.6.9 **Word Selection RAMs**

This test checks the ability of the RAMs to store data that control the word selection circuitry. A failure indicates the unit may not recognize S, J, A, and T words in the trace control commands.

10.4.7 KEYBOARD

When this test is selected, the keyboard test routine is automatically entered and a display appears as in Figure 10-126. The unit is prompting you to press **DATA.** After you press **DATA**, the display changes and prompts you to press **GRAPH.** To complete the test (and exit the test routine) you must press each key in the proper sequence as prompted by the display (by columms, left to right, going up from bottom row to top row). A BAD KEY error message appears if a key is pressed out of sequence or if the key immediately preceeding the one just pressed is actually bad. (In other words, an actual bad key is not indicated until the next key is pressed.) All 56 keys must be pressed before you can exit the test: there is no way to abort the test.

10.4.8 CRT ALIGNMENT

CRT alignment simply provides a test grid on the CRT in order to adjust it for proper visual linearity (see Figure 10-127).

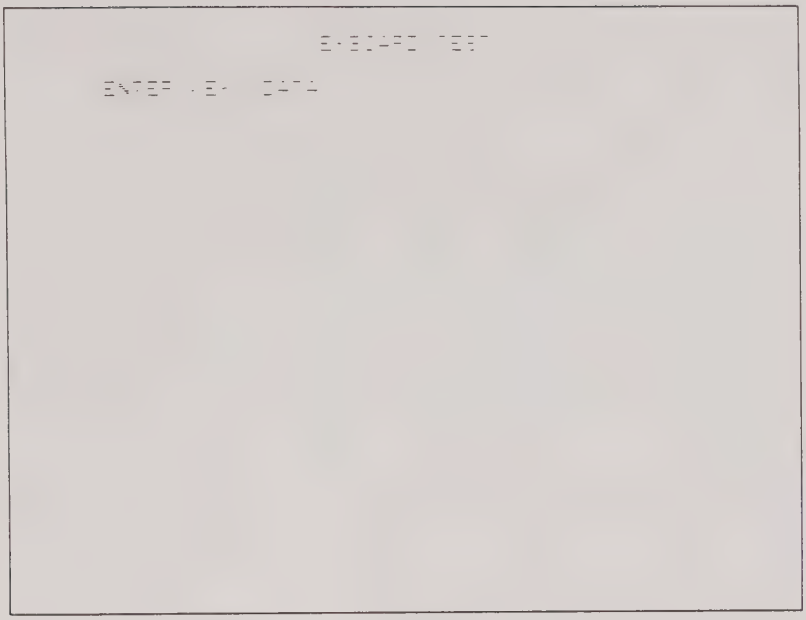


Figure 10-126. First Keyboard Test Display.

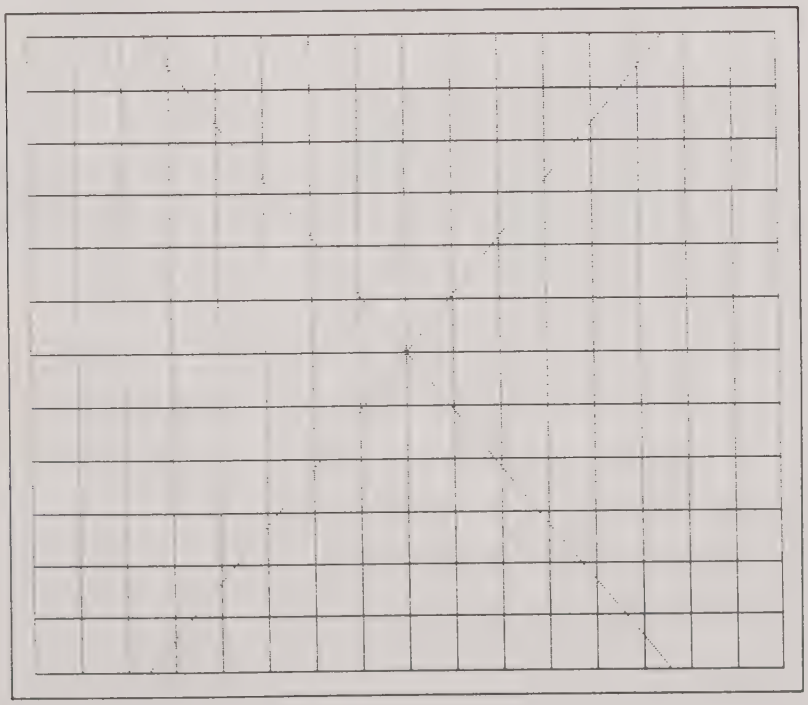


Figure 10-127. Alignment Test Grid.

10.4.9 PARAMETERS

The submenu that is shown when parameters is selected is shown in Figure 10-128. Parameters enhances all of the Self-Test diagnostics. The lower section of the display provides a cumulative total of errors detected during the Self-Test diagnostics. (The totals are reset to zero upon entering Self-Test.) The first field allows you to choose three types of error display modes, which are selectable by the **NEXT** key. The selections are as follows:

a. **Page.** If a failure occurs in a chosen diagnostic test, the unit displays one page (display) of errors only.

b. **Scroll.** If a failure occurs, the display scrolls through the entire list of errors.

c. **No Print.** No errors are displayed even if a failure occurs.

LOOP ON TEST may be selected as YES or NO. If YES is selected the unit continuously performs one Self-Test after another. Once it is looping, the only way to exit Self-Test is to turn off the unit. This allows the instrument to be checked for correct performance over extended use. NO stops after one Self-Test cycle.

```
                    PARAMETERS

  ERROR MODE = PAGE          LOOP IN TEST = NO

---------------------------------------------------------

                    ERROR SUMMARY

ROM                 00000    CLOCK FREQUENCY    00000
CMOS RAM            00000    LEVEL MEMORY       00000
DATA BOARD A        00000    PORTS CONDITIONS   00000
DATA BOARD B        00000    ADVANCE/JUMP       00000
DATA BOARD C        00000    WORD DETECTION     00000
ADC CALIBRATION     00000    DELAY CONTROL      00000
POWER SUPPLIES      00000    DELAY RAMS         00000
THRESH SOURCE       00000    DELAY COUNTERS     00000
THRESH SELECTORS    00000    WORD DETECTION     00000
PROBE LOADING       00000    WORD SELECT RAMS   00000
VAR A/B             00000    KEYBOARD           00000
```

Figure 10-128. Parameters Display Screen.

K101 and K102 Calibration Procedure

Rev. A1
6/16/82

Recommended Test Equipment

Item	MFG	Model No.
3 1/2 Digit DMM	Tektronix	DM501
Oscilloscope	Tektronix	485 or 475A
Frequency Counter	Hewlett-Packard	5316A
0-25 V Power Supply	Hewlett-Packard	6215A
K-101 DVM Leads	Biomation	0114-0057
K-101 Probe Set	Biomation	0114-0254
K-101 Extender Card	Biomation	0950-0135
20 pin .3" IC Clip	Any	Standard
3 mini-clips	Any	Standard
4.7k ohm 1/4w,5%resistor	Any	Standard

I. Display Calibration

To check the unit for proper raster scan display alignment, power-up the unit, depress the "shift" key, then the "selftest" key and move the cursor up 2 times. Then depress the "Next" key. The unit should now be in the CRT alignment mode. The adjustments below are available on the Data Display Board, refer to Figure IA for location of adjustments.

1. Adjust R20 for height
2. Adjust R21 for vertical hold
3. Adjust L1 for width
4. Adjust L2 for horizontal linearity
5. Adjust R29 for focus
6. Adjust R32 for brightness
7. Adjust R47 for vertical linearity

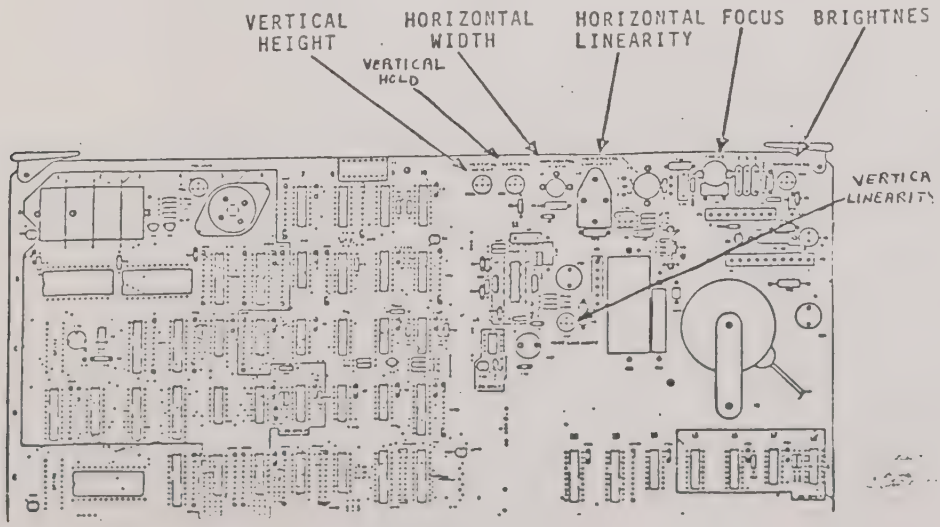


Figure 1A

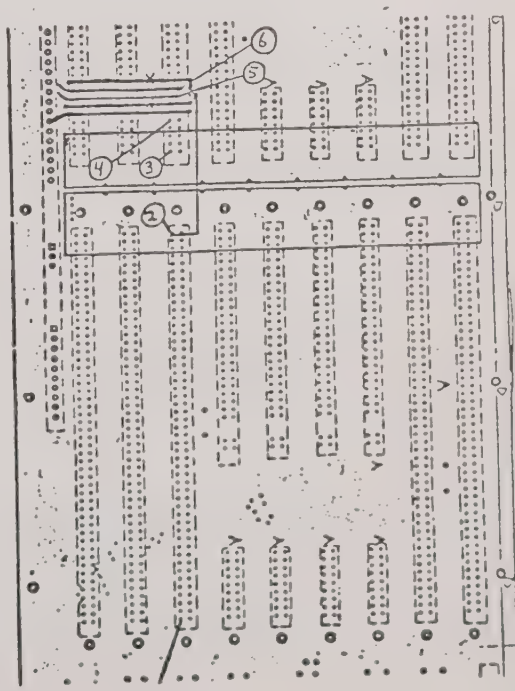
NOTE: The unit must be allowed to warm up for at least 10 minutes prior to calibration.

II Power Supply Voltage Adjustment

All input probes should be installed in the unit prior to adjustment. The soft start power supply has each pots purpose labeled. For pot replacement on the old style power supply refer to figure 2A. For measurement test points refer to figure 2B.

1. Remove the bottom cover from the unit and stand the unit on its rear feet.
2. Measure and adjust the -5.2 v. supply to -5.290 volts ± 5 mv.
3. Measure and adjust the +5.0 v. supply to +5.060 volts ± 5 mv.
4. Measure and adjust the -15.0 v. supply to -15.010 volts ± 5 mv.
5. Measure and adjust the +15.0 v. supply to +15.010 volts ± 5 mv.
6. Measure and adjust the -2.0 v. supply to -2.090 volts ± 5 mv.
7. Recheck all voltage measurements. Note that the -5.2 v. supply is the reference for all of the other supplys.

Figure 2B. Front of unit



Test Points

1. +5 v.
2. Gnd
3. -5.2 v.
4. -2.0 v.
5. +15 v.
6. - 15 v.

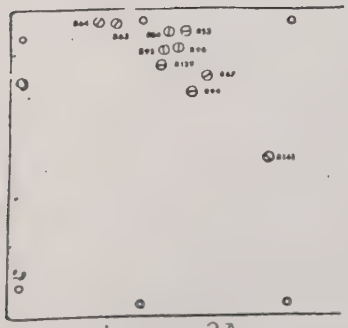


Figure 2A

R64 (-15 V ADJUST)
R63 (+15 V ADJUST)
R54 (+15 V OVERCURRENT)
R53 (-15 V OVERCURRENT)
R95 (-5.2V OVERCURRENT)
R96 (-2 V OVERCURRENT)
R129(-2 V ADJUST)
R87 (-5.2V ADJUST)
R94 (+5 V OVERCURRENT)
R141(+5 V ADJUST)

III Power Supply Current Limit Adjustment

The current limits have been set at the factory and should not require calibration. Prior to adjusting the current limits, the voltage settings in Step 2 should be checked and adjusted if necessary. Refer to Figure 2A for pot placement on the Old Style power supply or labeling on the supply for the soft start type power supply. Note that the +15 and -15 volt supplys may not draw enough current to allow the supply to go into current limit. Do not adjust the current limit on the ± 15.

1. Install a complete set of input probes into the unit.

2. Turn on the unit. Adjust the -5.2 v. supply's current limit down (counterclockwise) slowly until the supply shuts down (current limit).

3. Adjust the -5.2 v. supply's current limit pot up approximately 1/2 turn (clockwise).

4. Turn the unit off then back on. Verify the power supply does not go into current limit.

5. Repeat steps 2 through 4 for the +5 volt power supply.

6. Repeat steps 2 through 4 for the -2.0 volt power supply.

7. Recheck all voltage settings. Refer to Section 2.

IV Threshold Voltage Adjustments.

Remove all input probes from the unit. This procedure utilizes a 4.7 k ohm resistor as a load for adjustment of the thresholds. Install a 4.7k ohm resistor between pins 2 and 14 of the AO section input probe connector on the front panel. All voltages will be measured across the resistor. For adjustment, install the resistor in the AO probe connector, refer to Figure 4A for threshold adjustment pot placement.

1. Turn on the unit. Depress the "shift" then "recall" keys. This will put the unit into a default condition for basic recording.

2. Depress the "input mode" key.

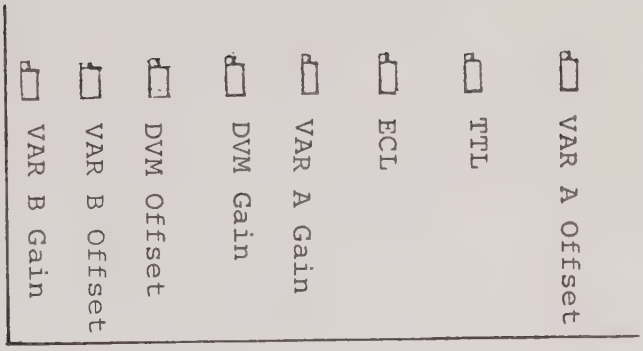
3. Move the cursor up once and hit the "next" key unitl the arm mode reads "auto".

4. Depress the " arm " key. The unit should now be continually taking new recordings, and will automatically update the threshold voltages to the new settings.

5. Change the threshold selection for all probes to "VAR A".

Front of Unit

Figure 4A



6. Set the Var A voltage to 9.98 volts plus or minus.

7. Change the polarity from plus to minus while measuring across the resistor. The voltage should measure 9.98 volts ±25 mv., in both polarity's. Set the voltage to 0.00 volts. It should measure 0.000 volts ±5 mv. Adjust the Var A gain and offset accordingly to meet spec.

8. Repeat steps 5 through 7 for " Var B".

9. Set the threshold selection on all probes to TTL and adjust the voltage to -1.400 volts ± 3 millivolts.

10. Set the threshold selection on all probes to ECL and adjust the voltage to +1.300 volts ± 3 millivolts.

11. Moving the lead resistor to each probe connector, measure the voltages for the correct spec. as in steps 6 through 10.

V. DVM Circuit Calibration

1. Turn on the unit, it should come up in the clock select mode.

2. Input +20.00 volts D.C. ± 5 mv into the DVM inputs on the front panel, noting the voltage reading at the top of the display.

3. Reverse the polarity of the input voltage. Note the reading at the top of the display. Adjust the DVM gain and offset accordingly until the DVM reads 20.00 volts ± .01 in both polarity's and 0.00 with no voltage input.

4. Depress the "shift" then "selftest" keys. Move the cursor down to the voltage test and depress the "next" key. Move the cursor up once and depress the "next" key. The unit should now be in the voltage calibrate mode.

5. Observe all of the voltages in the calibrate mode. Although the voltage tolerances indicated in the calibrate mode are wider, it is necessary that the readings are within the following ranges: (see top of next page)

Voltage	Minimum Acceptable	Maximum Acceptable
+15	+14.90	+15.10
-15	-15.10	-14.90
-10.00 reference	-10.04	- 9.96
+5	+ 5.02	+ 5.08
-5.2	- 5.31	- 5.25
-2.	- 2.12	- 2.07
+10.00 reference	+ 9.97	+10.03

6. DVM test. This test requires DVM cables to be connected. The DVM "input" on the front panel must be connected to the A8-F section input probe connector pin number 14. The DVM "GND" on the front panel must be connected to the A0-7 section input probe connector pin number 14.

   Move the cursor to the DVM test and depress the "next" key. The display should say "end of test"; listing no errors.

7. Run all of the voltage self tests without input probes installed, and all tests should pass except the probe loading test. Install all of the input probes and run the voltage self tests. All of the tests should pass.

VI. High Speed Clock Calibration

1. Turn power off, remove the clock board, and place on an extender. Turn power back on.

2. Refer to figure 6A (Clock Board) for location of parts and test points.

3. Connect the frequency counter to IC 12C, Pin 12, using pin 6 of the same device for ground.

4. Adjust variable capacitor C8 to obtain a frequency reading of 100 mhz $\pm$ 0.1 mhz.

5. Disconnect the frequency counter, and replace it with an oscilloscope probe, using the same signal and ground pins. Use the shortest possible ground lead on the probe.

6. Adjust R19 until the 100 mhz clock waveform is as symmetrical as possible, and centered on an ECL threshold of -1.3 v.

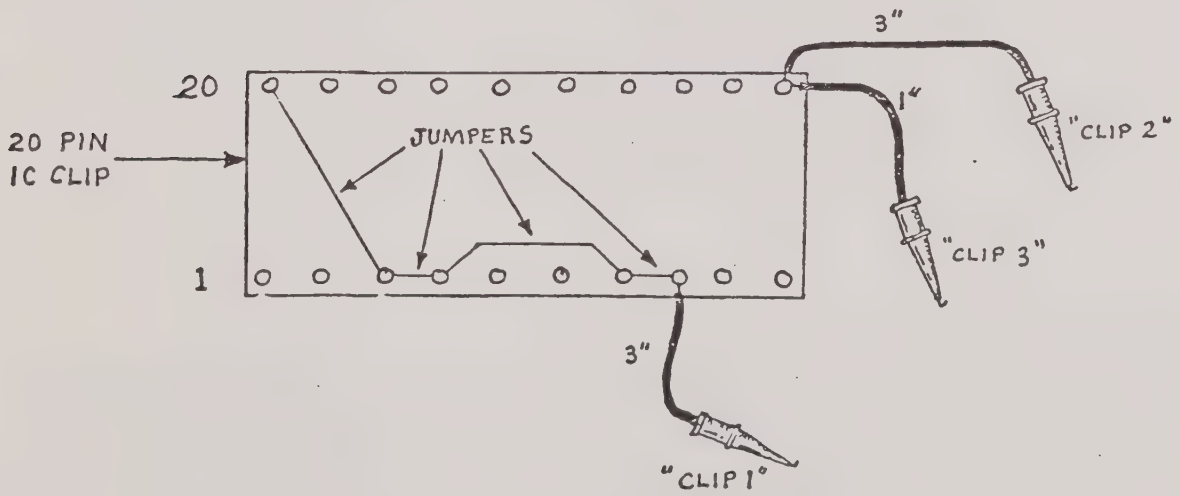
VII Real-Time Clock Calibration

1. Refer to figure 7A of the display board for part locations and test points.

2. Turn power off, place data display board on an extender, and apply power to the unit.

   Note: It is not necessary to re-connect the video cables, only the flyback high-voltage lead!

3. Using the IC clip and the mini clips, construct a test jig according to the drawing below



4. Carefully place the clip on IC, 4D-being sure to watch for proper orientation.

5. Connect "clipl" to IC 3D pin 8, connect "clip 2" to IC 3D pin 11, and "clip 3" to pin 10 of the IC clip.

6. The clock is now in the test mode.

7. Connect the frequency counter to IC 2D pin 9, and place the counter in the "period" mode.

8. Adjust variable capacitor C10 for a period reading of 976.5625 us, ±.0019 us.

9. This allows an initial accuracy of approximately ±5 seconds per month.

Figure 6A

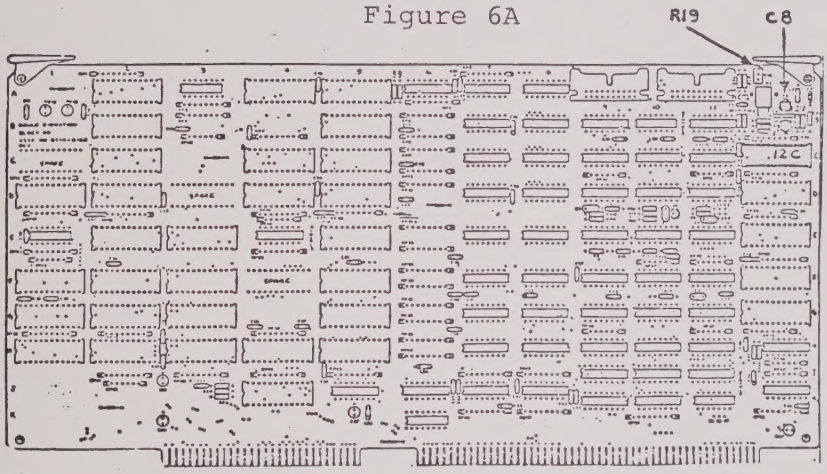
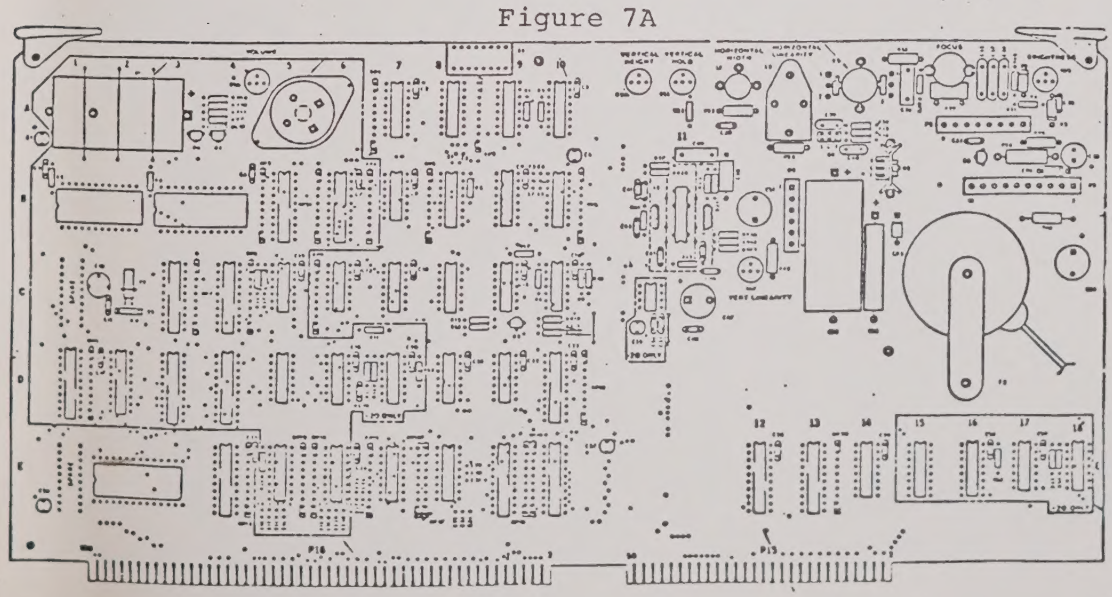


Figure 7A



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